A Dynamically High-Impedance Charge-Pump-Based LDO With Digital-LDO-Like Properties Achieving a Sub-4-fs FoM

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***Abstract*— This article presents an event-driven charge-pump-based low-dropout (LDO) regulator with an ac-coupled high-impedance (ACHZ) feedback loop. By using the ACHZ loop and continuous-time dead-zone detection, the proposed LDO responds in less than a clock cycle during load transients, achieving the response and settling times of 6.9 and 65 ns, respectively, all at a 4.9-μA quiescent current for a sub-4-fs FoM. The output ripple is measured to have a stable amplitude and is <15 mV over the LDO's 105 000× stable load range (1 μA–105 mA). In addition to all these features, the proposed LDO also retains the advantages of normal digital LDOs: process portability and the ability to operate at a low supply voltage.**

***Index Terms*— Analog assisted (AA), digital LDO, low-dropout (LDO) regulator, power management, voltage regulator.**

I. Introduction

SCALED CMOS systems on chip (SoCs) are trending in the direction of having many functional cores, where each core has its own power domain in order to be run at an optimal energy–performance tradeoff point. Since it is difficult to integrate high-power-density switching dc–dc converters directly into the SoC fabric, most solutions rely on one or more external power management ICs (PMICs) to bring the supply down to a scaled-CMOS-friendly voltage (e.g., $\leq$1 V), after which multiple on-chip linear low-dropout (LDO) regulators individually scale down and regulate the voltage of each core according to the dynamic application demands.

Conventionally, LDOs are designed in an analog manner, where an error amplifier is used in a compensated feedback loop to regulate the output voltage through a single power transistor. However, such analog LDOs have difficulty in operating well at low voltages due to the limited transistor overdrive. In addition, stabilizing analog feedback loops while achieving high performance can take a significant amount of time and effort, leading to long re-design times when specifications or process technologies change.

For these reasons, there has been significant recent interest in digital LDOs, which replace the analog amplifier with one or more comparators that digitally control an array of power transistors [1]–[4]. Since there are no analog amplifiers, low-voltage operation can be more easily achieved, and the most digital nature can enable more rapid process portability.

Despite these advantages, digital LDOs tend to have worse performance in terms of response time, settling time, ripple, regulation range, and power supply rejection (PSR) than a well-designed analog LDO [5]–[7]. Fundamentally, digital LDOs that rely on a clock for operation cannot, in the worst case, response to sudden full-scale load changes quicker than within a single clock cycle. In practice, shift-register (SR)-based N-bit digital LDOs require many clock cycles [1], while N-bit binary-search digital LDOs require up to N clock cycles [8], both of which may be too slow for the increasingly stringent demands of modern digital loads. While increasing the clock frequency can improve the response time, it directly leads to higher quiescent power and, without careful compensation, can result in stability issues. Changing from clocked to continuous-time comparators can help digital LDOs respond more quickly while retaining the favorable digital LDO properties of low-voltage operation and easier process portability [9], [10], yet they typically require energy-expensive multi-bit quantizers and have non-negligible delay through complex control logic.

To further improve the response time of digital LDOs, recent work has suggested using analog circuits to "assist" the digital circuits [11], [12]. Such approaches retain the benefits of digital LDOs yet offer direct performance advantages in terms of response time. In general, they operate by coupling the output voltage to the gate of the power transistors through a high-pass RC network, which enables the provision of nearly instantaneous compensation current during load transients. However, the compensation effect is seriously degraded when the load current is small in [11], while [12] cannot respond to voltage overshoot during load transient and has a limited input/output voltage range. Besides, such approaches do not yet address the ripple and regulation range.

To help improve the ripple, regulation range, and PSR of digital LDOs, other recent solutions have suggested combining digital LDOs with analog LDOs operating in parallel to create hybrid LDOs that inherit the performance benefits of both approaches [13]–[17]. However, such solutions may not be appropriate in the applications in which digital LDOs are advantageous: applications that operate at low input voltages (since analog amplifiers are still needed) or in applications that require rapid process portability (since the analog feedback

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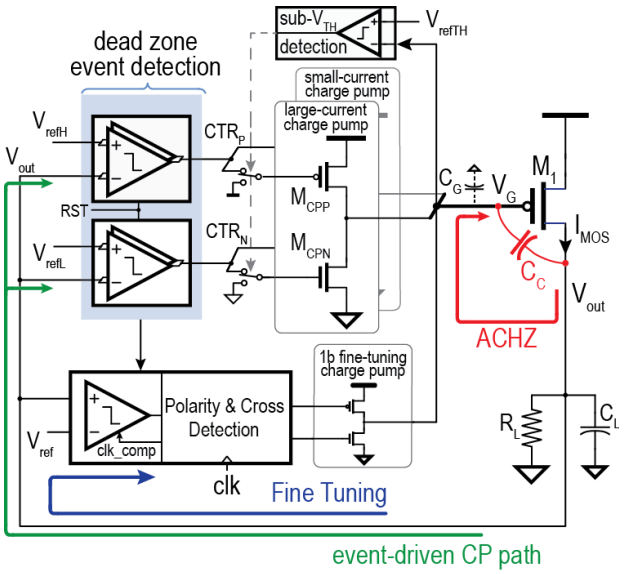


Fig. 1. Proposed charge-pump-based LDO with ACHZ loop.

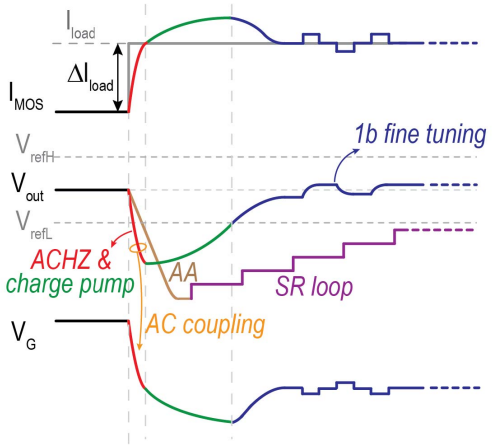


Fig. 2. Transient response waveform of the proposed LDO.

loops can be difficult to stabilize without a large design time/effort). Thus, while such approaches may yield excellent performance across numerous specifications, especially in regard to PSR (which is not normally addressed in digital LDOs and in fact may be quite poor—though this is often acceptable for digital loads), their comparison points should really be to hybrid or analog LDOs, not digital LDOs, in which case the utility of the hybrid approach is less clear.

This article presents the design of an LDO that mostly operates in an analog manner yet is specifically designed to retain the advantages of digital LDOs: namely, low-voltage operation and easy process portability, all with favorable response time, quiescent current, ripple, and dynamic range [18]. To enable low-voltage and process scalable operation, the design, shown in Fig. 1, forgoes the use of an amplifier and instead biases the voltage of a single power transistor via a charge pump (CP), which is controlled by two dead-zone comparators. A direct ac-coupled high-impedance (ACHZ) feedback loop is further used to dynamically increase response time and help stabilize the system, while a small-current charge pump is then used to improve regulation accuracy in the design. It should be noted that the proposed design does not improve PSR in any way over conventional digital LDOs.

This article is organized as follows. Section II describes the architecture and operation principle of the proposed LDO. Section III discusses the speed, ripple, and dynamic range advantages of the proposed LDO over the conventional architectures, while Section IV analyzes the system stability and design tradeoffs between settling speed and stability. Section V presents the circuit implementations and the design considerations, and Section VI presents the measurement results and the respective analyses.

II. Architecture and Working Principle

The architecture of the proposed LDO is shown in Fig. 1. In contrast to conventional digital LDOs that utilize arrays of PMOS power transistors, the proposed design utilizes a single PMOS power transistor, M_1, driven by a pair of charge pumps, which in turn are driven by a pair of time-interleaved dynamic-inverter-based continuous-time comparators setting upper and lower regulations bounds ($V_{\mathrm{ref}H}$ and $V_{\mathrm{ref}L}$) of a regulation dead zone. Capacitor C_C is set across the power transistor M_1 to form the ACHZ loop. In addition to the pair of continuous-time comparators that set the regulation dead zone, an auxiliary clocked comparator is used to compare the output voltage with V_{ref}, usually set to be in the middle of the dead zone, to detect whether the output voltage is above or below the desired reference voltage and improve regulation accuracy through an auxiliary 1-bit fine-tuning charge pump.

The working principle of the LDO is as follows. When V_{out} is within the dead zone between the bounds during steady state, the main charge pumps are disabled (ignore the fine-tuning charge pump for now), and their output, V_G, is high any residual charge stored on C_C and parasitic capacitance C_G determines the power transistor's gate voltage and, thus, the current supplied by the LDO. The ACHZ loop is formed by directly ac coupling V_{out} to V_G via V_G via capacitor C_C. Since this node is high impedance in this state (when the charge pumps are OFF), any droop experienced at V_{out} during a load transient will directly couple to V_G with coupling efficiency set $C_C/(C_C + C_G)$. This serves to directly lower the gate voltage of M_1, thereby providing near-instantaneous compensation current through the power transistors (i.e., I_{MOS}), which helps to significantly shorten the response time, as illustrated by the red section of curves in Fig. 2.

Though it helps to significantly improve the response time, the ACHZ loop may not be able to provide all of the necessary compensation current to return the LDO's output all the way back to the middle of the dead zone under all circumstances. This is where the charge pumps come in. When V_{out} falls below $V_{\mathrm{ref}L}$, as also shown in Fig. 2, in Fig. 2, the lower continuous-time comparator is triggered, which turns on $M_{chargepumpN}$ for continuous-time integration. This then further discharges V_G, thereby further increasing the current through the power transistor, I_{MOS}, to help V_{out} settle back to within the dead zone. After V_{out} settles to $V_{\mathrm{ref}L}$, the lower bound detection comparator's output is flipped

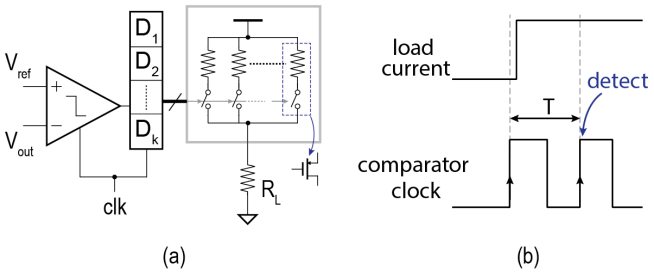


Fig. 3. (a) Conventional SR digital LDO architecture. (b) SR digital LDO detection delay.

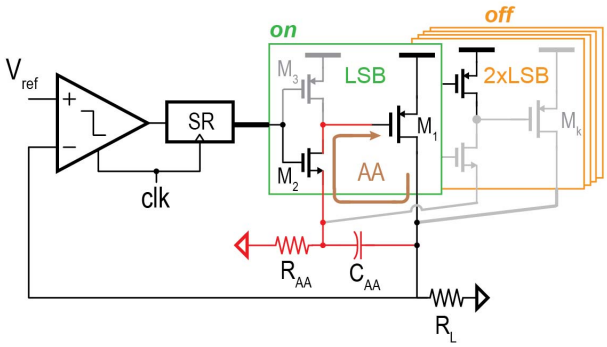


Fig. 4. AA loop when only the LSB power transistor is ON.

again, which turns off transistor M_{CPN} in the charge pump, and thus, the main charge pump is shut down. Interestingly, during this phase, V_{out} will settle in the dead zone with the help of the ACHZ loop—the details of this will be discussed in detail in Section IV.

Ideally, the ACHZ loop should provide instantaneous compensation current when load transients occur, and the charge pump path should begin operating as soon as V_{out} drops out of the dead zone. Thus, ideally, both paths should operate together, with some possible time overlap. However, when the edge rate of the load is faster than the propagation delay of the charge pump loop, it is possible that the ACHZ loop will provide most of the compensation current to reduce output droop, while the charge pump path is mainly responsible for voltage recovery and settling. On the other hand, if the edge time is relatively long, then both the two paths contribute current to reduce the voltage drop.

Since the gain of the power transistor changes rather dramatically once the device enters the subthreshold region, loop stability can be affected at high values of V_G. To compensate for this, a subthreshold detection block is used that, upon the detection of a subthreshold gate voltage, disconnects the large-current charge pump from the CP path and only use the small-current charge pump. The stability of this approach will be discussed in more detail in Section IV.

To improve the accuracy of V_{out}, an auxiliary small-size charge pump path is used for fine-tuning. After V_{out} settles back and re-enters the dead zone, the main charge pump is turned off and the auxiliary 1-bit fine-tuning charge pump path is activated. A clocked comparator compares V_{out} with V_{ref}, and the result is used to regulate V_{out} by 1 LSB per cycle toward V_{ref}. Once V_{out} crosses V_{ref}, this auxiliary fine-tuning charge pump path is turned off to avoid limit cycling. If small perturbations in the output voltages are present, the fine-tuning charge pump can be left on so that the dead-zone detector will not be frequently triggered. Due to the small-size transistors in the fine-tuning charge pump, the impedance at node G is larger than 4 MΩ, and together with the low-latency event-driven charge pump path, the load transient voltage droop difference is less than 3 mV compared to the non-continuous mode.

III. Performance Analysis

This section will describe the speed, ripple, and dynamic range performance of the proposed LDO and contrast it to prior-art digital LDO designs.

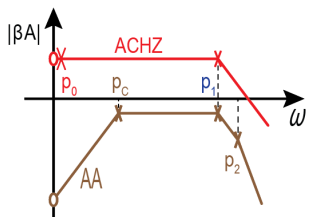
A. Speed

Both the detection and the response speed of conventional SR digital LDOs are limited by the clock frequency. For the representative conventional SR-based digital LDO shown in Fig. 3(a), the comparator can only perform the comparison at the edges of the clock, and thus, if a load transient happens right after the edge of the clock as shown in Fig. 3(b), the digital LDO requires essentially an entire clock cycle to detect the load transient and then another cycle to respond. After detection, at least several clock cycles are required in conventional SR-based digital LDOs to settle back, as shown in Fig. 2. Increasing the clock frequency would increase the detection and response speed, and however, this directly trades off with increased quiescent power consumption. Moreover, increased frequency may also degrade the phase margin of the system, potentially rendering it unstable as described briefly in Section IV and by the analysis in [8].

On the other hand, the proposed ACHZ loop responds nearly instantaneously to sudden load current steps, and thus, the proposed LDO can respond in less than a clock cycle, importantly without any increase in clock frequency or quiescent power. Since the ACHZ loop may not provide all necessary compensation current, the charge pump path is also designed to respond quicker than a single clock cycle thanks to the continuous-time comparator (which are designed for low quiescent power as described in Section V), the output of which is used to perform a fast continuous-time integration, as shown in Fig. 2.

The proposed ACHZ loop is thematically similar to the analog-assisted (AA) loop in [11], which can also provide nearly instantaneous compensation current when there is an output voltage droop and coupled through the RC feedback network shown in Fig. 4. However, the amount of compensation current in the AA technique is seriously degraded when the load current is small. For example, in Fig. 4, when the load current is small and thus only a single LSB power transistor is ON, the coupling only affects the LSB and thus only supplies a small amount of compensation current.

There is also a difficult tradeoff between the value of the resistance in the feedback loop, R_{AA}, the coupling efficiency, and settling speed. To have a high coupling efficiency, a large time constant in the high-pass RC network is preferred, which means a large value of R_{AA} and C_{AA}. For a given time constant, a large value of R_{AA} and a small value of C_{AA}



	Expression	Loop
p_0	$1/(R_{HZ}C_C)$	ACHZ
p_1	$1/[(R_{M1} // R_{load}) \times C_C]$	AA & ACHZ
p_2	$1/(R_{M2}C_G)$	AA
p_C	$1/(R_{AA}C_{AA})$	AA
A_V	$g_m \cdot (R_{M1} // R_{load})$	AA & ACHZ

Fig. 5. Bode plot of ACHZ and AA loop.

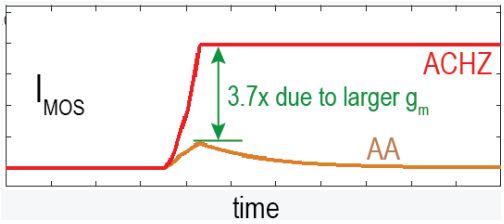


Fig. 6. Open-loop instantaneous compensation current simulation results of ACHZ and AA loops.

are used to save silicon area [11]. However, a large value of R_{AA} would affect the normal turn-on time of the power transistor since it is in the path between the drivers and the ground. To improve upon the speed–area tradeoff, the AA loop was modified to a NAND-based high-pass analog path (NAP) with NMOS power transistor in [12]. Using an NMOS power transistor together with a voltage doubler to boost the gate-driven voltage can achieve a fast response speed due to the inherent V_{GS}-I_D relationship. However, it has the drawbacks of limited input or output voltage range. In [12] and [19], the voltage doubler directly boosts the input voltage and the maximum input voltage of the LDO can only be half of the maximum supply voltage of the process, and the input/output range is only 150/200 mV in [12]. In [20], the voltage doubler boosts an internally generated voltage, which permits the input voltage to be the normal power supply voltage of the process. However, analog clamp and buffer blocks are needed, which is not suitable in digital LDO applications. Besides, the LDO output voltage is still limited to $V_{\mathrm{DD/PUMP}} - V_{\mathrm{TH}}$ and the dropout voltage can potentially be large. This problem becomes even worse in advanced process since the threshold voltage does not decrease as much as the supply voltage. The settling speed is also limited by the clock frequency of the charge pump.

On the other hand, the proposed ACHZ loop does not suffer from such tradeoffs. Specifically, there is no large high-pass resistance in the normal settling path, and thus, there is no RC-based tradeoff. In addition, since the output voltage droop is directly coupled to the gate of the sole power transistor, it can provide full compensation capabilities at all current levels, including the important case of a low (e.g., sleep mode) current. Moreover, due to the high impedance at V_G, the V_{out}-to-V_G coupling efficiency is set by $C_C/(C_C + C_G)$, where C_G is the parasitic capacitance at the gate of the power transistor. During this V_{out}-to-V_G coupling process, C_L does not affect the coupling efficiency. Therefore, only a small C_C value of 40 pF is required to achieve over 90% coupling efficiency, even for a 105-mA capable PMOS.

Importantly, the proposed ACHZ loop can, even with the same (high) load current, provide more compensation than the AA loop due to inherent loop stability advantages. In the AA loop, there are three poles and one zero, as shown in Fig. 5. To ensure that the system is stable, the loop gain $A_V = g_m \times R_{\mathrm{out}}$ is set to be <1 [21], which means a limited compensation current. The proposed ACHZ loop has only two poles, and the pole located at V_G (p_0), which is close to origin due to the high-impedance node, is canceled by the zero introduced by C_C. Thus, the ACHZ loop has only one effective pole, and thus, the ACHZ loop on its own is inherently stable (the stability of the overall multi-loop system will be discussed in Section IV). This means that the loop gain can be set to >1 to obtain larger g_m, improving compensation current by 3.7× over an AA loop for $I_{\mathrm{load,initial}} = 5$ mA, as shown in Fig. 6. Due to the high-impedance node, the compensation current can also last for a longer period of time, at least until the charge pump kicks in (which is not shown in this example).

When V_{out} falls out of the dead zone and the charge pump starts to drive V_G down (green segment of V_G in Fig. 2) to increase I_{MOS}, the falling V_G is coupled to V_{out} through C_C and may affect V_{out}. The coupling factor is

$$\frac{\Delta V_{\mathrm{out}}}{\Delta V_G} = \frac{R_L // \frac{1}{sC_L}}{\frac{1}{sC_C} + \left(R_L // \frac{1}{sC_L}\right)} \tag{1}$$

without considering the charging current from the power transistor. Large C_L can thus attenuate the effect from ΔV_G. However, this coupling voltage is very small and can be neglected due to the complementary relationship between ΔV_G and R_L. For example, when ΔI_L and ΔV_G are large, R_L is small and vice versa. Thus, when I_{load} jumps, for example to the maximum load current of 105 mA, ΔV_G has the largest amplitude. In this case, ΔV_G falls by 70 mV in 19 ns in simulation, and R_L is 500 mV/105 mA = 4.76 Ω. From simulation, even with zero load capacitance, the voltage coupled to output is about 700 μV. When ΔI_{load} is small, the output impedance is larger, but the amplitude of ΔV_G also becomes smaller, and the coupled voltage is small. From simulation, the output voltage decreasing coupled by V_G drop is less than 2 mV in the entire load range. Moreover, with the charging of I_{MOS} or an additional load capacitance C_L, its effect can be neglected.

Interestingly, the proposed LDO can potentially be even faster than an analog LDO designed with the same quiescent current, since high-power multi-stage amplifiers are usually used in analog LDOs to achieve a high loop gain. To achieve high speed, the last stage, which drives the large power transistor, requires a large static bias current to improve slewing during large load transient. While for the proposed LDO, since the power transistor is driven by a charge pump, and the charge pump is OFF for most of the time, a large static bias current is eliminated.

B. Output Ripple and Voltage Tuning Ability

Due to their inherent switching nature, baseline digital LDOs have ripples at their outputs, even at steady state. Unfortunately, this ripple amplitude can increase significantly when the load current is small since the ratio of the LSB transistor's resistance (which is fixed) to that of the effective load resistance gets worse at low currents [8].

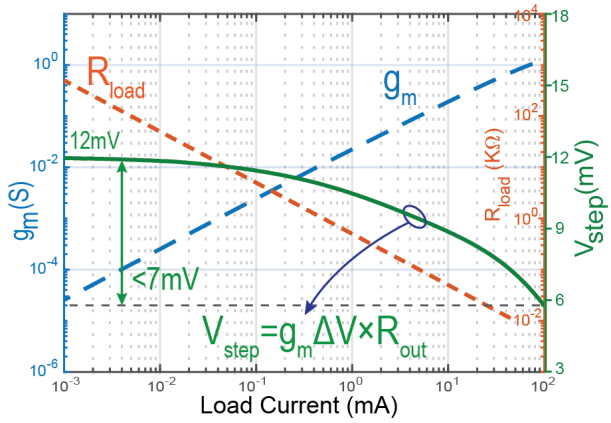


Fig. 7. Relationship between load resistance, power transistor g_m, and V_{step}.

Fortunately, the output ripple and tuning ability tradeoff is inherently mitigated in the proposed LDO. Since g_m of the power transistor is proportional to the load current, the decreased g_m compensates the increased R_{load} at small load current and generates small and stable step voltage. Similarly, the increased g_m compensates the decreased R_{load} at large load current, thereby maintaining a good voltage tuning ability in this case. Fig. 7 shows this intrinsic compensation, demonstrating that the step voltage varies between 6 and 12 mW, or a 7-mV variation, across the entire 100 000× load current range with zero load capacitance according to simulations. With an additional load capacitance, C_L, this ripple amplitude can be further reduced.

C. Dynamic Range

For an SR-based digital LDO, the load current dynamic range (DR) is given by

$$\text{DR} = \frac{I_{\max}}{I_{\min}} = \frac{N \times I_{\text{unit}}}{I_{\text{unit}}} = N \tag{2}$$

which is determined by the number of power transistors N. Increasing the number of power transistors can increase the dynamic range, however, at a cost of power consumption and the area of power transistor drivers. Using a binary-search control can mitigate this issue [8], but the MSB-first switching may potentially generate large output glitches.

Fortunately, the proposed LDO can achieve a large dynamic range without significant power or area overhead. Specifically, the charge-pump-based LDO generates the maximum current when the gate voltage of the power transistor is pulled down to zero, that is

$$I_{\max} = \frac{1}{2} \times \mu_P C_{\text{ox}} \frac{W}{L} (V_{\text{DD}} - |V_{\text{TH}}|)^2 \tag{3}$$

where μ_P is the transistor's mobility and C_{ox} is the gate oxide capacitance per unit area. The minimum current that the LDO can provide is set by the transistor's cutoff leakage current, that is, when the gate voltage of the power transistor is V_{DD}

$$I_{\min} = \mu_P C_{\text{ox}} \frac{W}{L} (n-1) \phi_t^2 e^{-V_{\text{TH}}/(n\phi_t)} \tag{4}$$

where n is the subthreshold coefficient and ϕ_t is the thermal voltage. With (3) and (4), the dynamic range of the charge pump LDO can be obtained as

$$\text{DR}_{\text{CPLDO}} = \frac{I_{\max}}{I_{\min}} = \frac{\frac{1}{2}(V_{\text{DD}} - |V_{\text{TH}}|)^2}{(n-1) \times \phi_t^2 e^{-V_{\text{TH}}/(n\phi_t)}}. \tag{5}$$

This dynamic range can be as large as 2×10^6 according to calculations and simulations.

IV. Comments on Stability

Stability analysis is critical to all LDO designs. As discussed in Section III-A, the ACHZ loop itself (i.e., when ignoring the contributions of the charge pump path) is inherently stable. Unfortunately, analysis beyond this loop is complicated by the inherently non-linear nature of the full LDO.

To help better intuitively understand the stability of the LDO, this section will first look at the transient operation of the proposed LDO in three cases and qualitatively discuss how the overflow current can potentially cause stability issues, which can be resolved by inclusion of the ACHZ loop. A non-rigorous stability criterion of the system is then ascertained from this discussion. Then, a concise piecewise linear time-domain analysis method is used to quantitatively analyze the non-rigorous stability criterion of the system. This analysis helps the designer model and understand the tradeoff and relationships among circuit parameters and the charge pump current, overflow current, and the time required for V_{out} to go back to the dead zone (t_1 to t_2). It should be noted that rigorous non-linear stability analysis is outside the scope of this article and may be the subject of a future publication.

A. Qualitative Analysis of Transient Operation

In conventional SR-based digital LDOs, a faster clock permits a shorter response and settling time. However, when f_{clk} is much larger than the effective frequency of the load's pole, f_L, the SR can potentially accumulate more zeros or ones than necessary, which can turn on or off more transistors than desired in a short period of time, which results in an oscillatory or unstable response, as described in [8].

The same sort of stability issue could, if not compensated for, occur if the charging or discharging speed in the charge pump of the proposed LDO is too fast. Fig. 8 will be used to qualitatively illustrate this for three different cases.

1) Slow charge pump Without the ACHZ Loop: After a sudden load step in example curve ①, a slow charge pump is activated after a brief delay through the dead zone and continuous-time comparator. This serves to decrease V_G, which increases the amount of current provided by the power PMOS, I_{MOS}. Once $I_{\text{MOS}} = I_{\text{load}}$, then V_{out} would ideally stop decreasing and stall at its current value. If this value of V_{out} is outside of the dead zone, then the charge pump will remain ON and provide a small amount of overshoot current until V_{out} returns to the dead zone.

2) Fast charge pump Without the ACHZ Loop: The previous example was found to be stable, at least qualitatively. To improve response and settling time, the charge pump current (i.e., its speed) can be increased. However, as illustrated

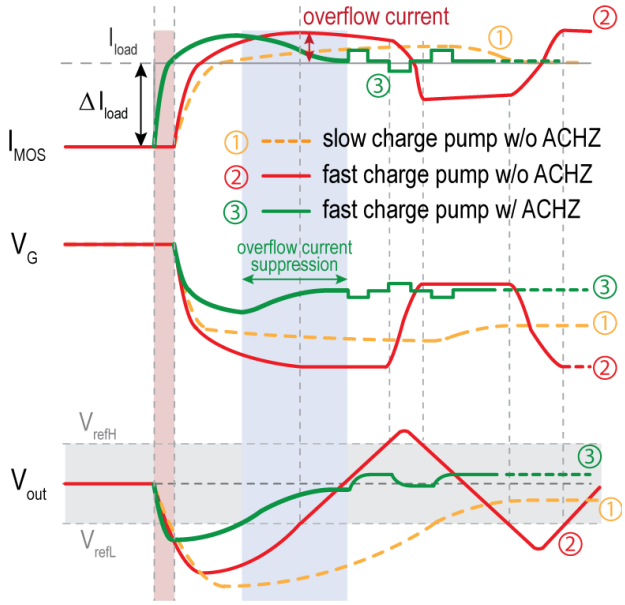


Fig. 8. Load transient waveforms comparison with and without ACHZ loop.

by example curve ②, stability issues can arise if the charge pump is made too strong. In this example, the high current available by the charge pump will help to more rapidly pull down V_G, rendering a slightly faster response time and a significantly reduced time for V_{out} to settle back into the dead zone. However, the overflow current at the time V_{out} enters the dead zone will be large. At this point, the charge pump turns off, and thus, V_G remains largely the same since it is a high-impedance floating node in this state, thereby keeping this large overflow current at approximately the same level as before. This can cause V_{out} to rapidly increase, possibly even shooting outside of the upper bound of the dead zone, which will trigger the upper bound detecting comparator to start charging V_G quickly, which may then compensate too much, such that V_{out} shoots outside the bottom of the dead zone and so on, rendering the system unstable. Because of this, the charge pump current without the ACHZ loop cannot be designed to be too large, thereby resulting in a direct speed–stability tradeoff.

3) Fast charge pump With the ACHZ Loop: Fortunately, the inclusion of the ACHZ loop can help facilitate an increased charge pump current without compromising stability—breaking this tradeoff. Example curve ③ qualitatively illustrates this. In this example, the ACHZ provides a nearly instantaneously compensation current before the continuous-time comparator can react, already improving the response time. Once the comparator does react (and after its propagation delay), then the charge pump is activated. This means that the gate of power transistor is no longer floating, and the coupling facilitated by the ACHZ loop is temporarily attenuated by the low-impedance charge pump's termination. Thus, at this time, the charge pump provides some overshoot current until V_{out} enters the dead zone. At this point, the charge pump is shut OFF, thereby making V_G high impedance again and re-activating the ACHZ loop. During this state, the increasing V_{out} (due to the overflow current) is coupled to V_G, which serves to increase V_G, thereby naturally suppressing the overflow current to help V_{out} settle within the dead zone. As a result, a much faster charge pump can be employed than without ACHZ, which helps to reduce settling time by 56% according to the simulations.

Note, however, that g_m of power transistor M_1 becomes very small when it enters the subthreshold region, and thus, the overflow current suppression loop is less effective in this case. To combat this, a subthreshold detection circuit is employed, where a comparator is used to compare the gate voltage with the threshold voltage of the power transistor. When it detects the power transistor enters the subthreshold region, it disables the large-current charge pump, which helps to extend the stable operation range down to 1 μA, for an effective 6.6-bit resolution improvement compared to without this technique.

B. Quantitative Piecewise linear Time-Domain Analysis

Normally, a digital LDO driven by a fixed clock can be linearized such that a small-signal model can be constructed and its stability can be analyzed via Bode diagrams [22], [23]. However, event-driven multi-loop LDOs do not have constant sampling rates and in fact have several working states, and thus, linearized small-signal models are not accurate [9]. Here, a time-domain stability analysis method is instead derived in order to give quantitative insight into the stability of the proposed LDO. Compared to the linearized small-signal model, the time-domain analysis method considers the initial and end conditions of each phase and gives a more accurate result (though is by no means a rigorous stability proof).

From the discussion in Section IV-A, we know that if the output voltage can settle within the dead zone, the system is stable; otherwise, it may result in an oscillatory output. The criterion to determine if V_{out} can settle within the dead zone is: whether the overflow current can be suppressed by I_{sup}, which is generated by coupling the rising V_{out} in the dead zone to the gate of the power transistor through the ACHZ loop. In this section, the expression of the overflow current I_{OF} and suppression current I_{sup} is derived. Then, using this criterion and comparing I_{OF} and I_{sup}, we can check whether the system is stable.

Consider the example shown in Fig. 9, where a sudden load transient occurs at t_0. Due to the fast edge rate of the resulting output droop, the ACHZ loop responses before the charge pump path and provides most of the compensation current between t_0 and t_1, as given by

$$I_L - I_{\text{ini}} = \eta \times Gm \Delta V_{\text{out}} \tag{6}$$

where η is the V_{out}-to-V_G coupling efficiency and G_M is the average transconductance of the power transistor. After t_1, the charge pump path starts working and V_{out} settles back, enters the dead zone at t_2 per the following:

$$\bar{I}_{t1t2} \times (t_2 - t_1) = C_L \times V_{\text{settle}} \tag{7}$$

where $\bar{I}_{t1t2}$ is the average charging current during t_1 to t_2 at output and

$$V_{\text{settle}} = \Delta V_{\text{out}} - \frac{1}{2} V_{\text{DZ}}. \tag{8}$$

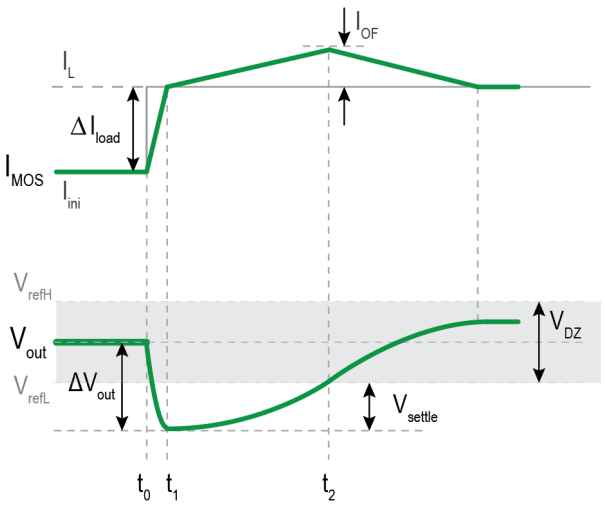


Fig. 9. Proposed LDO piecewise linear settling waveform during load transient.

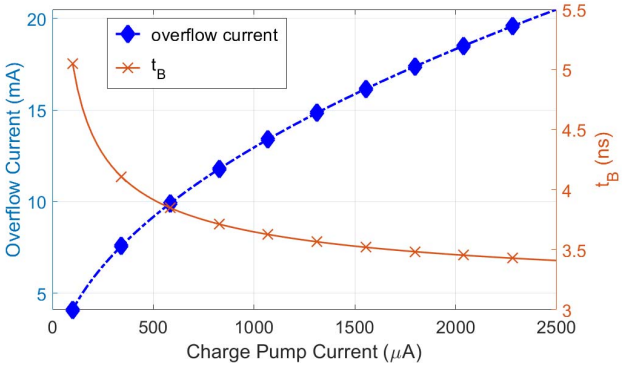


Fig. 10. Simulated relationship among charge pump current, overflow current, and settling time.

The increasing current from the power transistor is provided by discharging V_G

$$I_{\mathrm{CP}} \times (t_2 - t_1) = C_C \times \Delta V_{G,t1t2} \tag{9}$$

where I_{CP} is the charge pump current. At the time, the output voltage enters the dead zone, and the overflow current is

$$I_{\mathrm{OF}} = I_{t2} - I_L = Gm \times \Delta V_{G,t1t2} \tag{10}$$

while the maximum overflow current that the ACHZ loop can suppress is

$$I_{\mathrm{sup}} = Gm \times V_{\mathrm{DZ}}. \tag{11}$$

With the above-mentioned equations, the value of I_{OF} and I_{sup} can be calculated. If I_{sup} is larger than I_{OF}, it means that the ACHZ loop can suppress the overflow current and the output voltage can settle within the dead zone.

A MATLAB model is built and the relationship among charge pump current, overflow current, and the time required for V_{out} to go back to the dead zone (t_1 to t_2) t_B is plotted in Fig. 10. With a dead zone of 40 mV, I_{sup} is calculated to be 32 mA. From Fig. 10, it can be observed that with a larger charge pump current, the settling time can be reduced. However, the overflow current is also increased, which may degrade

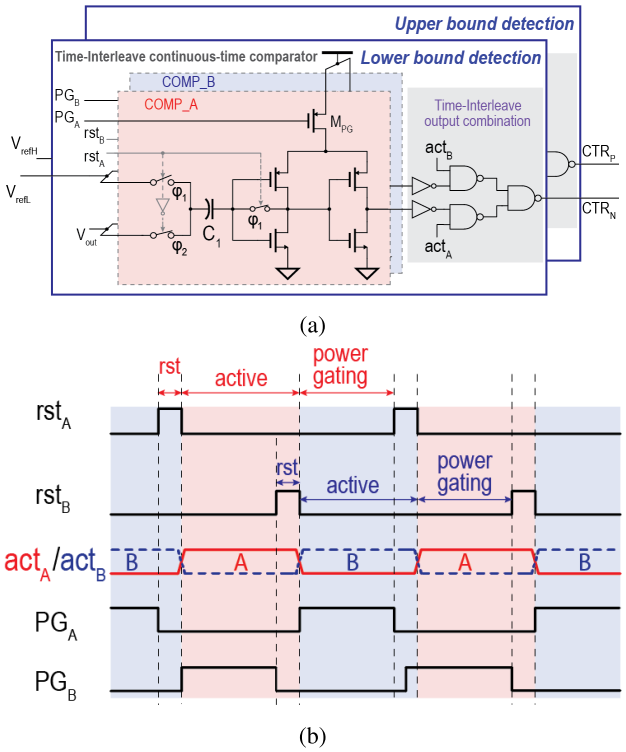


Fig. 11. Time-interleaved inverter-based continuous-time comparator (a) schematic and (b) timing diagram.

the system stability. When the charge pump current is larger than 1.5 mA, the improvement on t_B is very limited, while the overflow current is still increasing. Therefore, a charge pump current of 1.2 mA is selected, corresponding to a 14-mA overflow current, which is smaller than $I_{\mathrm{sup}} = 32$ mA, to achieve a fast settling speed while leaving some safety margin.

V. Circuit Implementation

The overall block diagram of the proposed LDO was shown earlier in Fig. 1 and was already generally described throughout this article. This section will focus on the implementation details of a few key circuits: the comparators, the ACHZ loop, and the power transistor.

A. Time-Interleaved Continuous-Time Comparator

The proposed architecture utilizes two continuous-time comparators to establish the upper and lower bounds of the dead zone, set by $V_{\mathrm{ref}H}$ and $V_{\mathrm{ref}L}$, respectively. The schematic of these two comparators is shown in Fig. 11(a). Their design is based on the design presented in [24], with one key addition to address an important issue.

The baseline design in [24] is an inverter-based design that has the advantages of resilience to PVT variation, process scalability, and low offset voltage. The design operates in two phases, shown in Fig. 12. During phase 1 (the reset phase), the input and output of the first inverter are connected together, and the reference voltage is sampled onto capacitor C_I. In phase 2 (the active phase), the input voltage is connected to

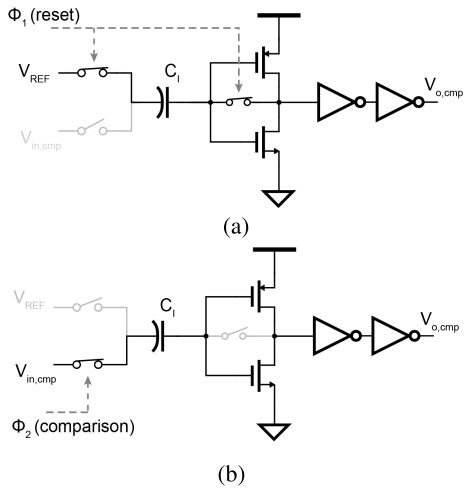


Fig. 12. Single dynamic-inverter-based comparator operation. (a) Phase 1. (b) Phase 2.

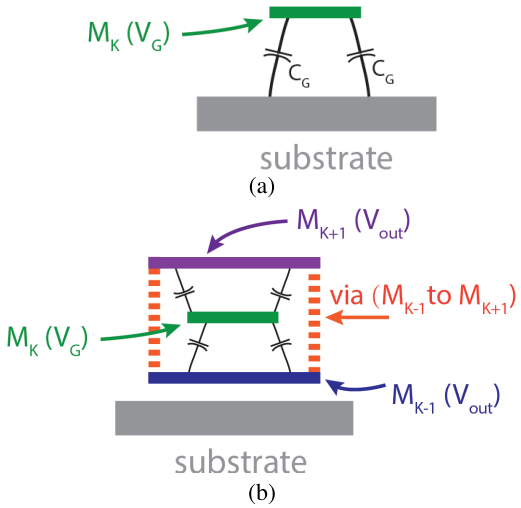


Fig. 13. V_G routing. (a) Normal routing. (b) Sandwich routing methods.

the bottom plate of capacitor C_I. Due to this double sampling feature, the inverter-based comparator has a very small offset voltage. However, it has to be reset during operation to refresh the charge stored on the sampling capacitor, which interrupts the detection. If a load transient happens in the reset phase, it cannot be detected and an error code will be produced [9].

To address this issue, a time-interleaved architecture is proposed in this design, as shown in Fig. 11(a). By time-interleaving two of these comparators, continuous-time operation is enabled throughout the reset phase. As shown in Fig. 11(b), when COMP_A is active, COMP_B is powered gated by M_{PG} to save power, and at the end of phase A, COMP_B is reset prior to the next activation to refresh the charge on sampling capacitor, C_I. Then, at the beginning of the next phase, COMP_B is activated and COMP_A is powered down to save power. In this way, the reset time slot is always hidden behind the activation phase, and the comparator is able to work continuously. Since only one comparator is activated at a time, and since the leakage current of the off-comparator is only 440 pA, the overall power of the time-interleaved comparator is almost the same as the original inverter-based comparator.

The output of the two inverter-based comparators is then combined and used to control the charge pump. When COMP_B (COMP_A) is power gated, its output is high impedance and may have an incorrect value. To eliminate its possible effects on the output, act_B (act_A) is set to ground so that the output of COMP_B (COMP_A) is blocked, and only the output of COMP_A (COMP_B) is effective.

$V_{\mathrm{ref}H}$ and $V_{\mathrm{ref}L}$ are generated off-chip to provide tuning flexibility during measurement. They can also be generated on chip using bandgap references with low-power buffers to drive the 1-pF sampling capacitors in the dynamic-inverter-based continuous-time comparators. V_{ref} is generated on-chip using $V_{\mathrm{ref}H}$ and $V_{\mathrm{ref}L}$ with a resistor ladder since it is connected to the gate of the clocked comparator and does not need to drive a heavy load.

B. ACHZ Loop

As mentioned in Section II, the V_{out}-to-V_G coupling efficiency is determined by $\eta = C_C/(C_C + C_G)$. A high coupling efficiency is desirable, as it can help to suppress the output voltage droop during load transient. Therefore, a small value of C_G and a large value of C_C are desired. However, the value of C_C should not be too large in order to save silicon area. Using a high metal layer to route V_G can reduce V_G to ground parasitic capacitance C_G, as shown in Fig. 13(a), but unfortunately, this shows only a minor improvement. Instead, a sandwich-based routing method is used in this design to minimize C_G and maximize C_C. As shown in Fig. 13(b), along the route of signal V_G (metal layer M_K), two metal layers M_{K-1} and M_{K+1} that are connected to V_{out} are put below and above it. The two metal layers are connected using M_{K-1} to M_{K+1} vias so that V_G routing is totally surrounded by V_{out}. Therefore, all V_G-to-ground parasitic capacitance on the routing wire are transformed into V_G-to-V_{out} coupling capacitance C_C, which increases the coupling efficiency.

C. Power Transistor

The parasitic resistance at the source and drain of the power transistor is also critical to the performance of an LDO that supports large load currents [25], [26]. In this design, the maximum load current is over 100 mA. This means even a 1-Ω parasitic resistance would result in an over 100-mV static voltage drop, which degrades the dynamic range. To minimize the parasitic resistance, the power transistor is split into 1680 multipliers and each one has 20 fingers whose width is less than 10 μm. In this manner, the parasitic resistance is reduced by a factor of 2.8×10^6 compared to using a single power transistor.

VI. Measurement Results

The proposed LDO is fabricated in a 65-nm process with an active area of 0.04 mm^2, including all capacitances. The

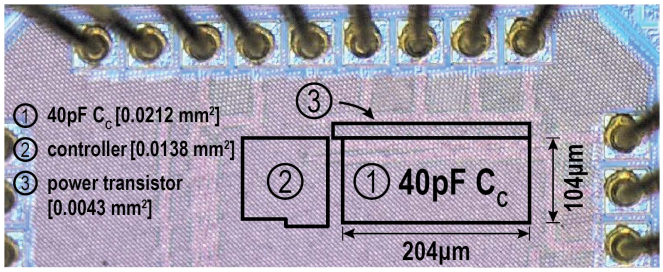


Fig. 14. Micrograph of the fabricated LDO.

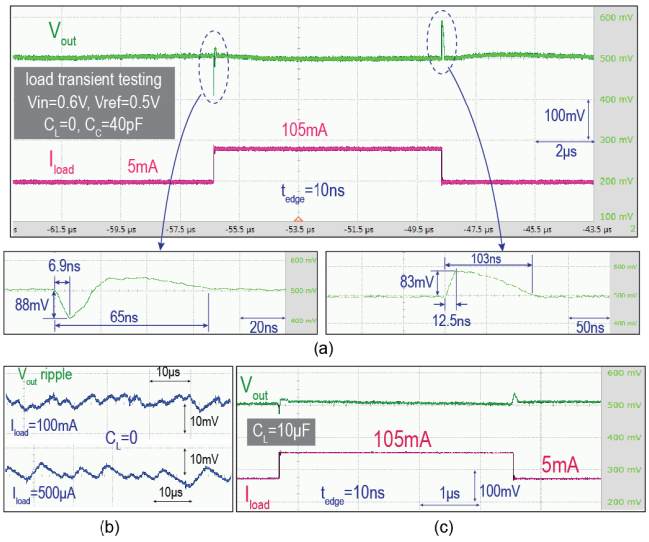


Fig. 15. Measured transient results. Response of the proposed LDO to a periodic load change with (a) $C_L = 0$ and (c) $C_L = 10$ μF. Output voltage ripple with (b) $I_L = 100$ mA and $I_L = 500$ μA.

chip micrograph is shown in Fig. 14. The total employed capacitance is 42 pF (40 pF for C_C and 2 pF for the comparators). Thanks to the high-impedance node at V_G and sandwich routing, the 40-pF C_C can provide an over 90% coupling efficiency. Since most of the parasitic capacitance from routing has been transformed to the coupling capacitor C_C, the power transistor intrinsic gate-to-ground parasitic capacitance contributes most of C_G. Therefore, the coupling efficiency can be improved if a smaller power transistor is used. The 40-pF capacitance of C_C occupies about 53% of the total effective active area. If the area budget for the LDO in the system is tight, a smaller coupling capacitor C_C can be used at the cost of lower coupling efficiency. A smaller sampling capacitor can also be used in the comparator with a shorter reset time interval to refresh the charge on the capacitor, at the cost of a higher power.

The measured transient response for $\Delta I_{\text{load}} = 100$ mA with a 10-ns edge rate (i.e., 10 mA/ns, which is the fastest edge rate among the previously reported low-FoM and high-current digital LDOs as shown in Table I) and zero load capacitance is shown in Fig. 15, demonstrating 6.9- and 65-ns response and settling times, respectively, with $V_{\text{droop}} = 88$ mV for an FoM of 1.8 fs. To achieve a faster settling during low-to-high load transient, the value of the discharging current is set to be larger than the charging current in the charge pump. In this case,

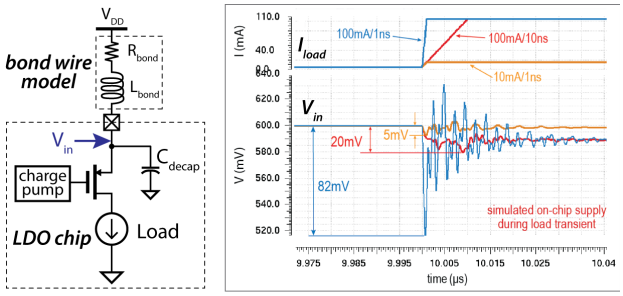


Fig. 16. (a) Illustration of the LDO bond-wire model. (b) Simulated on-chip supply (input of LDO) voltage V_{in} droop during large load transient current.

the output voltage may exit the dead zone as it settles back after the initial voltage droop. However, since the charging current is set to a value that ensures an overdamped settling, the output voltage will then settle within the dead zone when it is pulled down, as shown in the bottom left in Fig. 15(a). Thanks to the ACHZ and fast CP loops, the LDO can respond even before the end of the current transient, rendering in this case a response time that is faster than the edge rate.

Since the edge rate of the load transient can directly affect the response time and thus the FoM, the normalized edge rate of each design is listed in the table for comparison. To illustrate this effect, different edge rates are measured for the proposed LDO. To characterize the worst case FoM and push the LDO at edge rates beyond what have been reported in the literature, especially for high-current digital LDOs, $\Delta I_{\text{load}} = 100$ mA was also tested for a 1 ns edge, which is 10× faster than fastest other edge rate in the table. Naturally, the measured FoM of this design degrades with faster edge rates, yet it still remains below 4 fs in all cases in this design, which is still a state-of-the-art result, even despite the extreme edge rate.

It should be noted that other, non-LDO-based effects begin to come into play when large edge rates are tested. As shown in Fig. 16(a), the parasitic inductance of the bond wire and the on-chip decouping capacitor can potentially resonate during large transient events. For example, at the 100-mA/ns edge rate, a large input droop is also observed in simulations, as shown in Fig. 16(b). This 82-mV droop is due to the finite package and bond-wire parasitic inductance, which limits the current flowing from input voltage source, while the parasitic resistance causes a static 10-mV voltage drop when the output reaches the steady state. This input droop has nothing to do with the LDO design itself, but it does serve to reduce the measured FoM. Going from a bond-wire design to a flip-chip design could potentially significantly ameliorate this situation, for example.

The load step testing in Fig. 15(a) demonstrated that the proposed LDO can, with zero attached load decoupling capacitance, successfully regulate across representative large load changes with rapid response and settling times, all without oscillatory behavior. Fig. 15(c) then repeats this test, but a load decoupling capacitance of 10 μF is attached. Here, it can be seen that the proposed LDO can again successfully regulate with rapid response/settling time without oscillatory behavior. It should be noted that this would not be the case for a baseline digital LDO designed for a fast response—if the clock speed

TABLE I
COMPARISON WITH THE STATE OF THE ART

Design	Salem ISSCC'17	Huang ISSCC'17	Ma ISSCC'18	Tsou ISSCC'17	Kundu ISSCC'18	This Work			
Active area [mm^2]	0.102	0.03	0.006	0.19	0.03	0.04			
Process [nm]	65	65	28	40	65	65			
Architecture	BS+PD	AA+SR	NAP+SR	TB+TE	VCO based	Event-Driven charge pump+DCHZ			
V_{in} [V]	0.5-1	0.5-1	0.4-0.55	0.6-1.1	0.6-1.2	0.5-1			
V_{out} [V]	0.3-0.45	0.45-0.95	0.35-0.5	0.5-1	0.4-1.1	0.45-0.95			
Load range	100nA-2mA (20,000x)	0.2mA-13mA (65x)	0.5mA-20.5mA (41x)	1mA-201mA (201x)	20mA-100mA (5x)	1μA-105mA (105,000x)			
Load range with η>90%	33.6μA-2mA (60x)	N.R.	N.R.	N.R.	28mA-100mA (3.5x)	50μA - 105mA (2100x)			
C_L/total C [nF]	0.4/0.4	0/0.1	0/0.024	20/20	0.04/0.04	0/0.042			
Quiescent current [μA]	14	3.2	0.81	98.5	800	4.9			
Clock frequency	200MHz	10MHz	1MHz	N.R.	3.9MHz	1MHz			
Load transient current/ load step edge time	Load current range <50mA			Load current range (>50mA)					
	1.06mA/1ns* (1.06mA/ns)	10mA/1ns* (10mA/ns)	20mA/3ns* (6.6mA/ns)	200mA/1000ns (0.2mA/ns)	50mA/800ns (0.0625mA/ns)	100mA/1ns (100mA/ns)	100mA/10ns (10mA/ns)	100mA/30ns (3.33mA/ns)	100mA/60ns (1.67mA/ns)
V_{droop} [mV] for load transient test	40	105	117	36	148	185	88	56	36
FOM† [fs]	199,000	230	5.7	1,780	1,900	3.8	1.8	1.1	0.74
Settling time [ns]	100	3,000	9,000	1,600	1,240	62	65	45	53

N.R.= Not Reported
* For large current DLDOs, the edge rate is mainly limited by the input voltage droop due to parasitics during large load transient. The input voltage droop in lower-current DLDOs is typically less affected and can thus be tested at a higher edge rate.
† $\text{FoM} = \frac{C_{TOTAL} \cdot \Delta V_{OUT}}{\Delta I_L} \times \frac{I_Q}{\Delta I_L}$

f_S of such a design is much larger than the effective pole frequency of the load f_L, then V_{out} changes much slower than the decision of the controller, which would rapidly accumulate more zeros/ones in the barrel shifter, making the power transistor current much larger/smaller than the load current even if the load voltage has settled to V_{ref}, resulting in an oscillatory response as described in [8]. From the perspective of a z-domain model [22], a faster clock pushes the pole closer to the unit circle, thereby reducing the phase margin, which degrades system stability. Fortunately, the ACHZ loop in the proposed LDO helps to stabilize its operation even for a fast (high-current) charge pump, regardless of the load capacitance, as evidenced by the results in Fig. 15(c).

Thanks to the subthreshold detection and overflow suppression techniques, the LDO is measured to stably operate at load currents from 1 μA to 105 mA for a dynamic range of 105 000×, which is the largest among the prior art in Table I. The dynamic range is limited by two factors. Due to the large input IR drop at large load current, the gate–source voltage is reduced, which degrades the maximum load current that the LDO can provide. The minimum load current is limited either by the leakage of the power transistor or the leakage of the load circuit. To provide a >100-mA load current at high edge rates in the on-chip load test structure, LVT transistors are used. The leakage current of these load transistors is measured to be 1 μA, which is thus the lowest current that the implemented LDO can operate at. If a better load could be designed (or the edge rate specifications could be relaxed), it is possible that the LDO could be measured to achieve an even higher dynamic range.

The current efficiency over this entire dynamic range is shown in Fig. 17, where a current efficiency >90% is achieved over a 2 100× range from 50 μA to 105 mA for dc loading

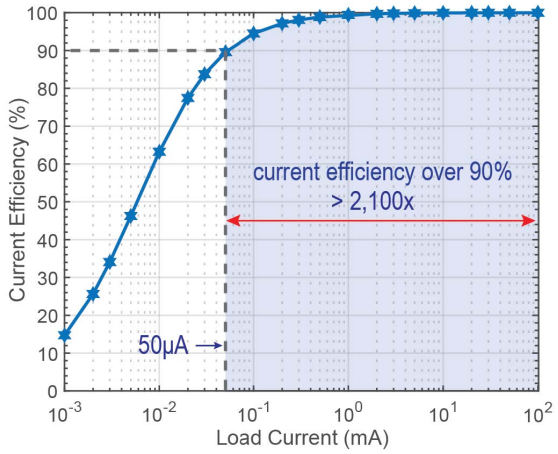


Fig. 17. Measured current efficiency at a 0.6-V input voltage for a 0.5-V output voltage.

conditions (noting that efficiency depends on the dynamics of the system and may get worse if the load current constantly changes by large amounts, throwing the output voltage frequently outside of the dead zone). Since the quiescent current of the LDO is independent of the dc load current, a high current efficiency of 99.995% is achieved when the load current is large.

Thanks to the fine-tuning capabilities and g_m-adjusting weighted-charge pump-based design, ripple is measured to be <10 mV at both $I_{\text{load}} = 100$ mA and 500 μA in Fig. 15(b) and <15 mV over the entire load range. The stable ripple amplitudes at different load currents verifies the analysis presented in Section III-B. It should be noted that the ripple amplitude is determined by the fine-tuning charge pump size,

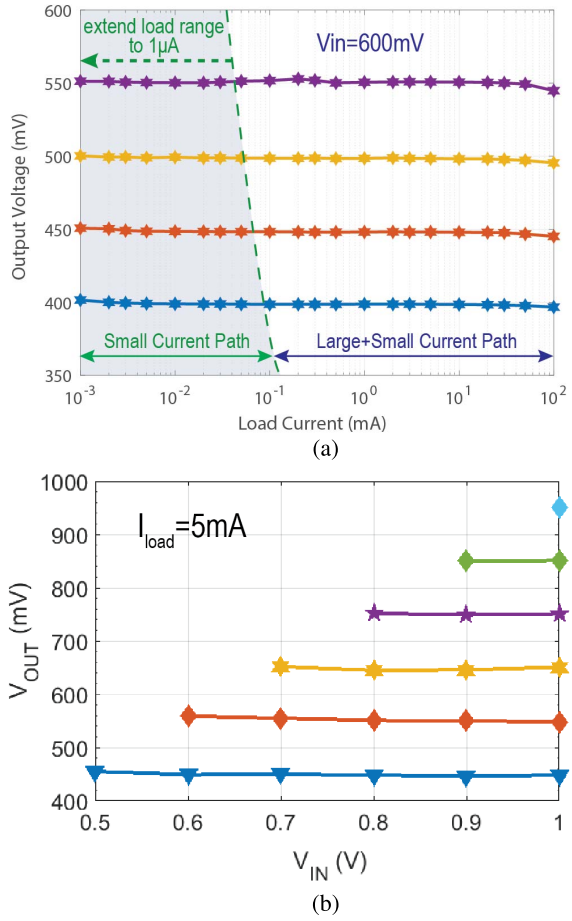


Fig. 18. Measurement results of (a) load regulation and (b) line regulation.

and it can be further reduced by using a fine-tuning charge pump that has a smaller size.

The measured load and line regulation results in Fig. 18 demonstrate 0.09-mV/mA and 6-mV/V worst case regulation, respectively. The good load and line regulation performance is mainly due to the high dc open-loop gain of the charge pump.

VII. Conclusion

An event-driven charge-pump-based LDO with ACHZ loop is presented in this article. Thanks to the ACHZ loop and low-latency event-driven charge pump path, the LDO can respond less than a clock cycle and achieves 6.9- and 65-ns response and settling times, respectively, with $V_{\text{droop}} =$ 88 mV for an FoM of 1.8 fs. With the help of the overflow current suppression, subthreshold detection, and dynamic g_m-adjusting, the LDO achieves a 105 000× load range (1 μA–105 mA). A <15-mV stable ripple amplitude is achieved over the entire load range.

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