Computers and Electrical Engineering 71 (2018) 43–59

Contents lists available at ScienceDirect

Computers and Electrical Engineering

journal homepage: www.elsevier.com/locate/compeleceng

# Designing ternary quantum-dot cellular automata logic circuits based upon an alternative model☆

Saman Mohammadi Mohaghegh[a], Reza Sabbaghi-Nadooshan[b,c,*], Majid Mohammadi[d]

[a] Department of Electrical Engineering, Arak Branch, Islamic Azad University, P. O. Box 38135-567, Arak, Iran
[b] Department of Electrical Engineering, Central Tehran Branch, Islamic Azad University, Tehran, Iran
[c] School of Computer Science, Institute for Research in Fundamental Sciences (IPM), P. O. Box 19395-5746, Tehran, Iran
[d] Computer Engineering Department of Shahid Bahonar University of Kerman, Kerman 76137, Iran

ARTICLE INFO

*Keywords:*
Adder
Decoder
Inverter
QCA
Subtractor
Ternary

ABSTRACT

Three-valued logic is recently being considered in the field of multi-valued logic due to its competitive advantages over binary logic for development of state-of-the-art digital systems. Despite several advances in this area, a comprehensive model that could have a profound impact on the trend of such a newfound system has so far not been proposed. Therefore, this study is an attempt to design basic ternary Quantum-dot Cellular Automata logic gates and various combinational ternary circuits like adders by use of our proposed model. To verify the design circuits, proposed ternary logic circuits are simulated by newly designed TQCAsim software while to scrutinize the effectiveness of simulation method, some prior proposed conventional gates have also been simulated. Moreover, effective factors such as area, energy consumption, fault tolerant and cost are investigated in the proposed circuits. The results show that, in addition to proper characterization, designed circuits are conveniently applicable for digital systems.

## 1. Introduction

According to Gordon Moore's law, every 18 months the number of transistors that could be integrated into a single chip is doubled which results in saving space and minimizing device sizes. The limitations of CMOS technology scaling caused by heat generation affect the device speed and density. This calls for alternative technologies to develop such as quantum-dot cellular automata (QCA), single electron tunneling, molecular electronics, silicon nanowire, carbon nanotube, tunneling phase logic, resonant tunneling devices, spin transistors and superconducting electronics.

In QCA which first proposed by [1], information can be transferred from one cell to another by propagating a polarization state instead of electrical current. Owing to beneficial properties like small size, high packing densities, small signal delays and low power consumption, QCA has gained attention recently. It was first proposed in binary form, though, there are more than two truth values known as multi-valued logic (MVL), that provides fast performance and inputs/outputs reduction [2]. Among the MVL logics, ternary logic (tQCA) is the most practical one. More details on QCA and tQCA will be presented in further sections.

Recently, some studies have been introduced various models for ternary logic gates. The first model [3], focusing on ternary majority gates. Within this study, ternary AND and OR logic functions are implemented as a hierarchy of three majority gate structures. In the second model, adiabatic pipelining technique is suggested [4,5]. They proposed that using this technique can meet

☆ Reviews processed and recommended for publication to the Editor-in-Chief by Associate Editor Dr. Debiao He.

* Corresponding author at: Department of Electrical Engineering, Central Tehran Branch, Islamic Azad University, Tehran, Iran.
*E-mail address:* r_sabbaghi@iauctb.ac.ir (R. Sabbaghi-Nadooshan).

https://doi.org/10.1016/j.compeleceng.2018.07.001
Received 19 October 2017; Received in revised form 24 May 2018; Accepted 9 July 2018

the challenges in designing ternary logic gates. In fact, exploiting this model, wire, fan-out, inverter and majority gate architectures are introduced. In a later study, a ternary memorizing cell has been designed using the same model [6]. The third model [7], illustrated a method to design an optimal tQCA logic circuit which can calculate an arbitrary ternary logic function and still others [8] introduced their work which is inspired by [1] whose configuration consists of nine dots potential well instead of eight dots. They also suggested 3-input, nine dot potential well majority gate. The last model [9] puts forward nonconventional QCA cell which implements multi-valued logic circuits with irregular shapes for ternary cells.

In our earlier work reported in [10], we proposed a new model to design ternary logic gates. To examine the effectiveness of this model, some prior proposed conventional gates like Min and Max gates has been implemented. Moreover, all presented gates are simulated by newly designed TQCAsim software which is designed based on the proposed model. However, the aim of this paper is to design more complicated and combinational ternary circuits like adders. For this purpose, we design various ternary gates like different kinds of inverters, decoder, and cycle. Using these gates leads us to design adder and subtractor. The simulation results show that the proposed design circuits are applicable.

The rest of the paper is organized as follows: Background of binary and ternary QCA is described in Section 2. Section 3 proposes ternary logic design and Section 4 implements basic ternary gates. Section 5 describes some combinational ternary circuits and the related simulation results. Finally, Section 6 concludes the paper.

## 2. Background of binary and ternary QCA

The binary quantum-dot cell is a square-shaped cell with four quantum dots occupying the four apexes of the cell. Based on Coulomb repulsion law two electrons can only occupy antipodal sides in the cell. Hence, each cell can have polarization state of either $P = 1$ or $P = -1$ with binary value states 1 and 0, respectively. Unlike binary area, in MVL, each bit can take more than a single logic value and more data can be saved in MVL memories compared to binary one. Low cost and faster numerical analysis are other advantages of MVL circuits. A significant discussion related to MVL is ternary logic [3] which can accept the values ``true", ``false", and ``unknown" (e.g. Łukasiewicz's, Kleene's and Priest's "logic). Ternary logic equals binary logic and even surpasses it, in some aspects. Ternary logic has main advantages which are as follows: (i) the least complex logic among MVLs (simplicity); (ii) ability to store more information in comparison with conventional binary logic; (iii) high speed; (iv) high performance and (v) cost-effective design. Therefore, using this logic can be beneficial in modern computing devices.

It is worth noting, one of the effective three-valued logic systems that can be compared with balanced ternary is Kleene's logic. The basic logic gates such as min (and), max (or) and inverter (not) gates are identical in Kleene's logic and balanced ternary logic. Naturally, all the ternary circuits are implemented by use of these basic gates and hence, the results of our proposed circuits are valid in Kleene's logic too. More information about this logic can be found in [11].

The most well-known ternary quantum-dot cell encompasses eight quantum wells located in a circle shape and a pair of electrons that can tunnel conveniently between these wells. Based on Coulomb Repulsion Force, a pair of electrons always stays furthest away from each other. Due to cell structure, these electrons can be placed in four different positions. Each position is equivalent to one logical state such as $-1$, $+1$, 0, and 0 (balanced ternary) or 0, 1, ½, ½ or 0, 0, 1, 2 (unbalanced ternary). Note that, two different positions have the same value. The electrons are allowed to move in a single cell, therefore, there is neither electron transfer between neighbor QCA cells, hence, current flows from one cell to another.

As mentioned so far, two mobile electrons are present in each QCA cell. Practically, these electrons can settle in their positions in quantum dots by means of the clock signal that fed to the input of QCA circuit. In fact, the clock can provide power and controls the movement of electrons within a specific cell (data transmission control). When the information is transferred to the circuit, it is joined with other inputs and produces the desired output. However, delayed inputs prevent the dissemination of information. Consequently, clock creates synchronicity in different parts of the circuit. It should be noted that QCA circuits do not need any external power. In any standard CMOS, the clock has two phases, but in QCA, it consists of four, including hold, release, relax, and switch. In other words, one of the clock roles is to control and change the polarization of the cell. Initially, cells are unpolarized, when the cell is biased by the input voltage (clock voltage), the barriers begin to rise during the switch phase and the movement of electrons is prevented, hence, electrons movement becomes slow. In hold phase, the barriers are raised completely and electrons remain in their own positions. In release phase, the barriers are lowered, then, electrons are released slowly while in relax phase, the barriers remain lowered and electrons are not localized to any particular dots within the cell, however, they are still confined to the cell and as a consequence, cells are unpolarized. More information about the clock performance can be found in [12].

It should be noted that, up to now, some binary QCA designs based on the various fabrication methods are theoretically and experimentally investigated [13,14]. However, according to our knowledge, no specific experimental results of ternary QCA have been reported.

## 3. Proposed ternary logic design

The main aim of this paper is to design various ternary logic circuits based on our earlier model reported in [10]. In this work, first, basic ternary logic gates like ternary majority gate and some ternary inverters are designed. Using this basic gates leads us to design combinational ternary circuits. Then, to evaluate our findings and results, all the proposed circuits are simulated precisely by TQCAsim software, designed for the first time by our team at IAUCTB laboratory. In addition, a trial version of TQCAsim software can be found online [15].

Before beginning to design, some significant items should be mentioned. The first item is cell configuration and value. Fig. 1,

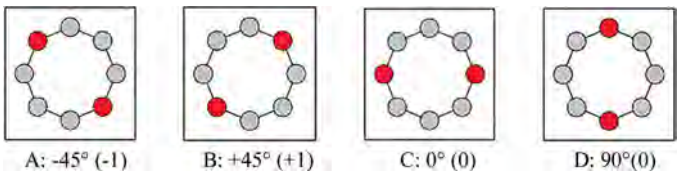



**Fig. 1.** Possible configurations of tQCA cell.

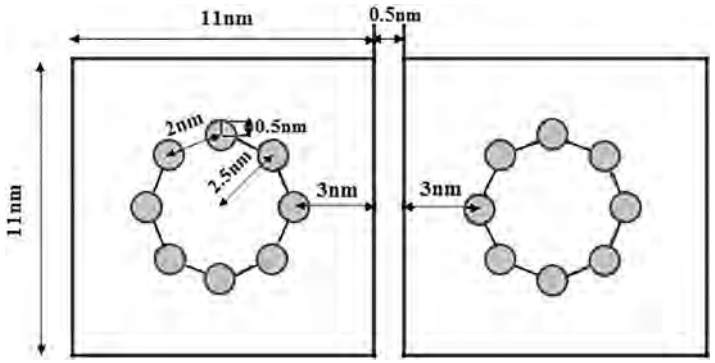



**Fig. 2.** The tQCA cell dimensions.

illustrates that tQCA cells can have four possible polarizations, named A, B, C, and D corresponding to logic values −1, + 1, 0, and 0, respectively. As mentioned earlier, state C and D have the same value of 0. The second item is to determine intracellular and extracellular distances. Fig. 2 shows our proposed dimensions in a tQCA cell which are determined based on the molecular scale. As seen in this figure, the quantum dots are spherical with a radius as small as 0.5 nm. In our proposed simulation tool, cell configurations and dimensions are defined like Figs. 1 and 2, respectively.

According to the proposed structure and cell dimension, (the barrier width is 1 nm while the barrier between two cells is at least 2 nm), it is concluded that we have a strong barrier and tunneling probability is exceptionally low. Therefore, quantum wells are isolated and have uncoupled ground state eigen energies [16]. Hence, electrons in their quantum dots are definitely localized and the effect of charge leakage can be ignored. It should be mentioned that the behavior of quantum dots is investigated in the hold phase of a clock cycle. In this state, the electrons are fixed into their positions.

## 4. Proposed basic ternary gates

In this section, ternary wire and basic ternary logic gates such as ternary majority gate (Min and Max gates) and different kinds of ternary inverters are introduced. Due to the fact that, ternary circuits are composed of ternary basic gates, defect and fault tolerant are investigated in this section.

### *4.1. Ternary wire*

By putting the ternary cells together in a row, a ternary wire can be created. As shown in Fig. 3(a), when two cells adjoin horizontally (or vertically) while assigning a value of + 1 (+ 45°) or −1 (−45°) to the input, the input and output values will be identical. However, by assigning a value of 0 (0° or 90°) to the input, the output value for the even-numbered chain of cells are 0 (90° and 0°) and for the odd-numbered chain are 0 (0° and 90°), respectively. Fig. 3(b) and (c) shows ternary wire. It's worth noting that, in our simulation design we used the junction cell that acts as a wire in such a manner that it can make the connection between input/intermediate cell and desired cell. For instance, a junction cell which is shown in Fig. 3(c) (sketched by pink), connects input A to entire circuit cells.

According to the proposed model, the significant defect in our ternary designs is displacement [17]. Fault in two ternary wires is scrutinized in Fig. 4. Fig. 4(a), shows two parallel wires with the distance between them. After testing different distances between these wires, it is concluded that *d* should be greater than 12 nm, otherwise, the double ternary wire cannot act properly. In Fig. 4(b), cell displacement of lower wire is presented. In this figure, intermediate cells (cells between input and output cells) of lower wire are displaced. For having defect-free wires, $d_1$ should be equal to 11.5 nm ($d_1 = 11.5$ nm) and $d_2$ should be greater than 12 nm ($d_2 \geq 12$ nm). In this case, $I_1 = O_1$ and $I_2 = O_2$.

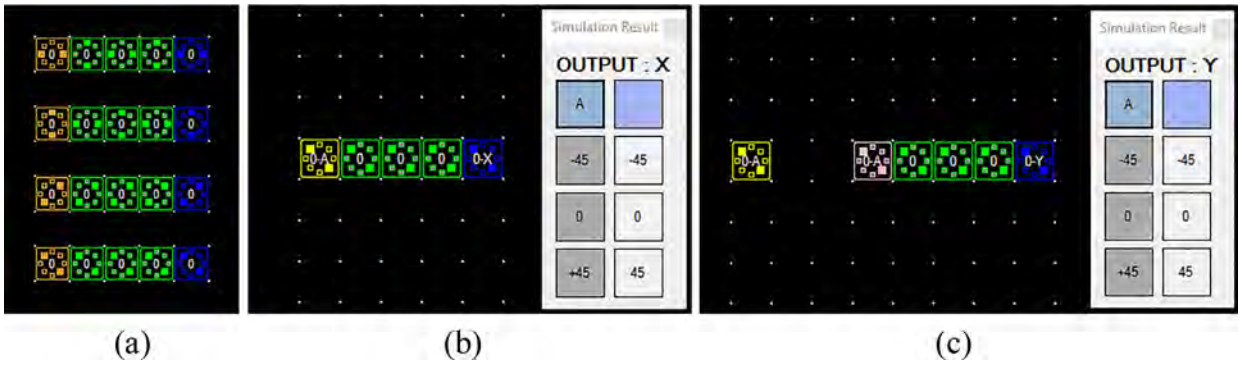



**Fig. 3.** Implementation of (a) ternary wire in four states (b) ternary wire using direct input and the related truth table (c) ternary wire using junction cell and the related truth table.

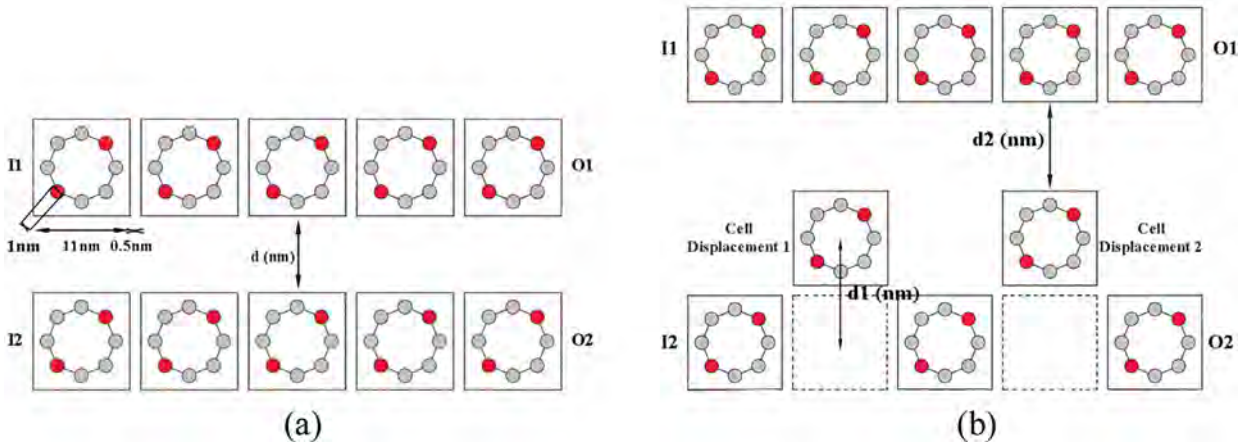



**Fig. 4.** Displacement in ternary wire: (a) fault free double ternary wire (b) defect in double ternary wire.

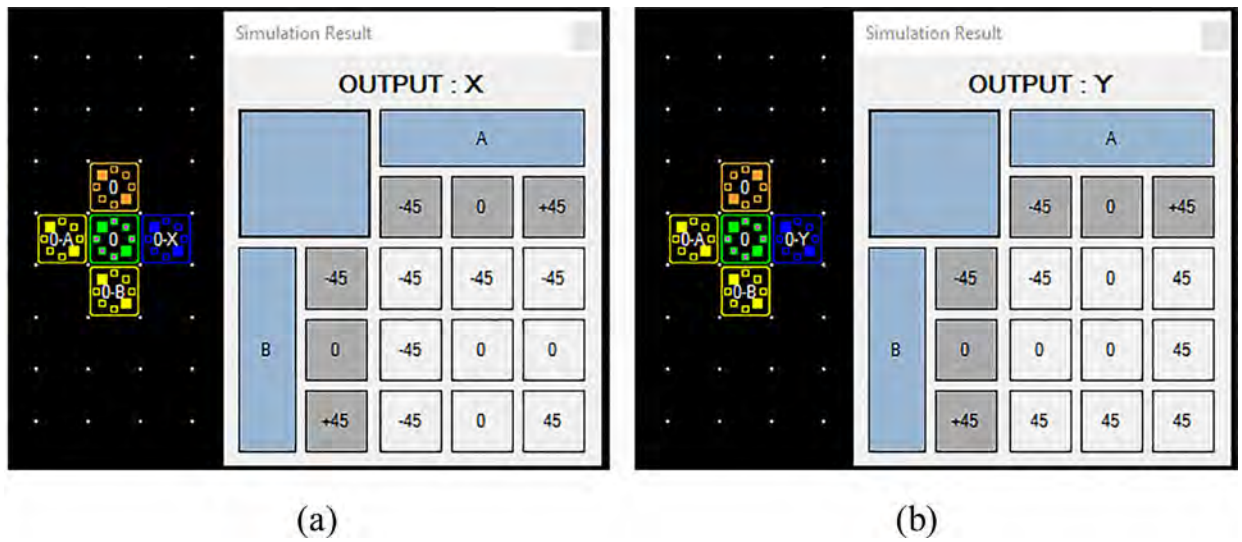



**Fig. 5.** Implementation of ternary (a) min and (b) max gates and their truth tables.

### 4.2. Ternary Min/Max gates

The first fundamental ternary gate is majority gate and normally has three inputs and an output. The Min (AND) and Max (OR) gates can be implemented by determining one of the inputs of the majority gate $-1$ and $+1$, respectively. The related functions are shown in Eq. (1). Implementation of the well-known Min and Max gates and their truth tables are shown in Fig. 5. It worth noting that, these gates were implemented in one clock. To create complicated circuits using the Min and Max gates, more than one clock should be used. If one of the inputs of Min and Max gates become zero, clamp down and clamp up gates will be obtained, respectively and if a standard inverter is added to the output of Min and Max gates, Antimin and Antimax gates will be achieved, respectively. It should be mentioned that, unlike binary majority gate, in ternary majority gate when inputs are different (such as $-1$, 0 and $+1$), the output should be undefined. These are unexpected values. However, in terms of logical view, all of the output values of this gate should be defined. According to our proposed ternary model which is based on energy calculation [10], due to the input values, TQCAsim software assumes that each time the output value is different ($-1$, 0 and $+1$) then, energy calculation is implemented for each state. The output with the minimum total energy is the correct answer. Thus, all the output values of majority gate are defined.

$$\begin{aligned} Output_{Min} &= (A \wedge B) = Min(A, B) \\ Output_{Max} &= (A \vee B) = Max(A, B) \end{aligned} \tag{1}$$

Fig. 6, displays cell displacement in majority gate. Based on our simulation results, majority gate is more vulnerable to displacement in the vertical direction than in the horizontal direction. According to this figure, majority gate can act normally (fault-free) only when input *2* displaced or input *2* and output displaced together. Indeed, when input *2* move to the west with $d_2 \leq 23$ nm, majority gate has normal operation.

### 4.3. Ternary inverter

The second basic ternary gate is the inverter. There are three common types of ternary inverters. The first and most common one is standard ternary inverter (STI). The positive ternary inverter (PTI) and the negative ternary inverter (NTI) are other types of ternary inverters. The related functions are shown in Eq. (2). Our proposed ternary inverters and their truth tables are illustrated in Fig. 7. As can be seen in Fig. 7(a), when two cells get together diagonally, and the input value set to $+1$ ($+45^{\circ}$) or $-1$ ($-45^{\circ}$), the output value is in contrast to the input value. However, when the input cell is 0 ($0^{\circ}$or $90^{\circ}$), the output value is 0. In both PTI and NTI gates (Fig. 7(b) and (c)), two fixed cells ($+1$ and $-1$) are used. If the output is along the main diagonal of the figure, PTI gate will be achieved and if the output is along the secondary diagonal, NTI gate will be achieved, therefore, an input and fixed cells can be substituted. It should be noted that, Fig. 7(b) and (c) are one of the possible configurations for PTI and NTI gates. These gates were implemented in one clock, but in more complex circuits, more than one clock should be used.

$$\begin{aligned} Output_{STI} &= -A \\ Output_{PTI} &= -(A = +1) \\ Output_{NTI} &= (A = -1) \end{aligned} \tag{2}$$

Another displacement in ternary QCA logic is double inverter chain displacement which occurs when cells rotated 45°. As we know, the ternary cell is symmetric, therefore, when the ternary cell rotated 45°, it would be similar to the original ternary cell, thus, this kind of displacement never happens in ternary QCA. In addition, ternary inverters like PTI and NTI are very sensitive to fault. Results show that when displacement occurs these gates are not fault free.

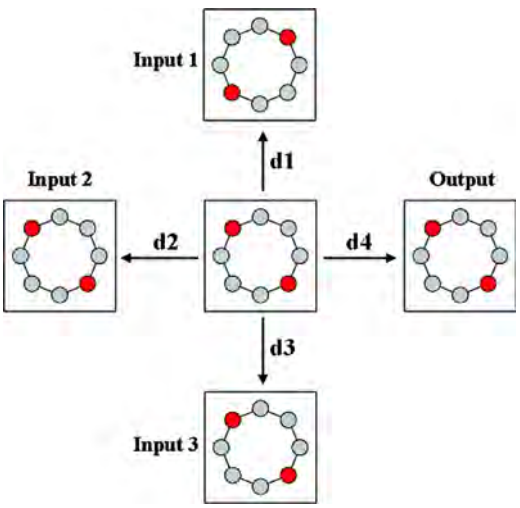



**Fig. 6.** Displacement in ternary majority gate.

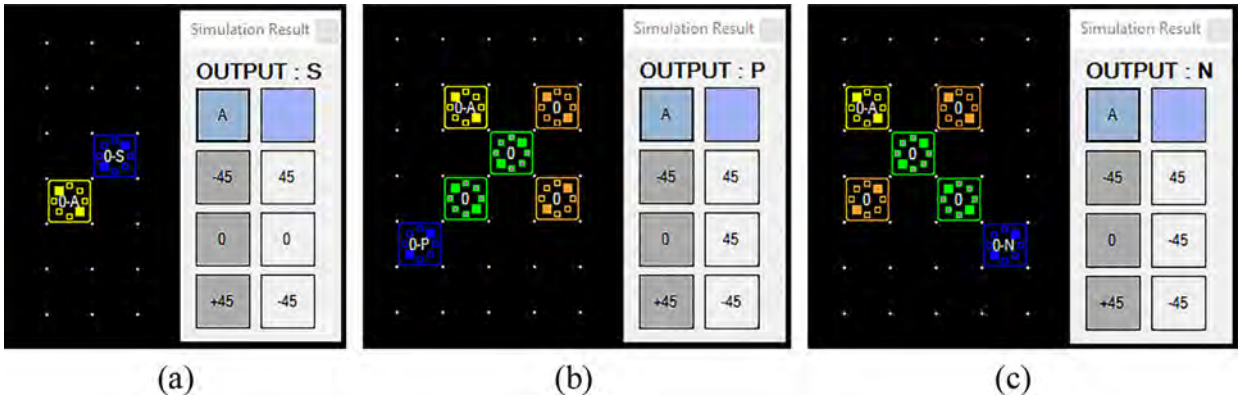



**Fig. 7.** Proposed ternary inverter (a) STI (b) PTI (c) NTI gates and their truth tables.

## 5. Proposed ternary circuits

Using the proposed ternary logic gates, lead us to design ternary logic circuits. In this section, all the significant combinational ternary circuits will be designed and investigated. Indeed, the final aim is to design adder and subtractor. Implementation of these circuits, the related truth tables, and clock simulation are presented. In addition, total area, cost, and energy consumption of the proposed circuit are calculated.

### 5.1. Ternary decoder logic

The ternary decoder is one of the most prominent combinational ternary logic circuits with a single input and multiple outputs which can be used in various applications. Indeed, using this gate leads us to design complicated ternary logic circuits like adders. According to Eq. (3), three decoding functions can be used to construct the decoder. A proposed ternary decoder and its relevant truth tables are presented in Fig. 8. As can be seen in this figure, three different types of inverters and a Min gate are used to implement the ternary decoder. Furthermore, clock simulation of the proposed decoder is illustrated in Fig. 9.

$$\begin{aligned} Ouput_{False} &= (A = -1) \\ Output_{Unknown} &= (A = 0) \\ Output_{True} &= (A = +1) \end{aligned} \tag{3}$$

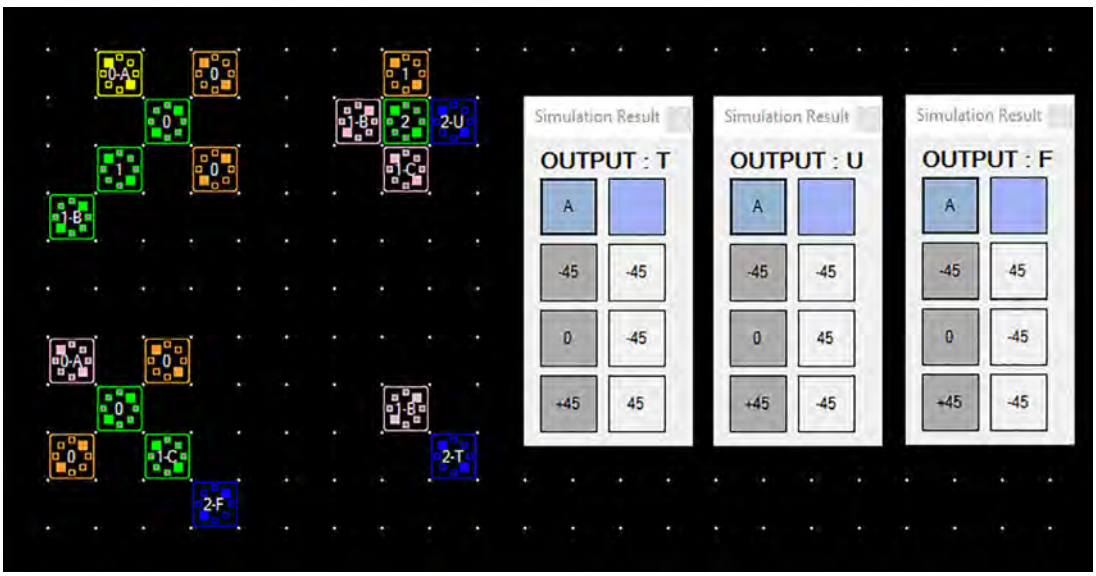



**Fig. 8.** Proposed ternary decoder and the related truth tables.

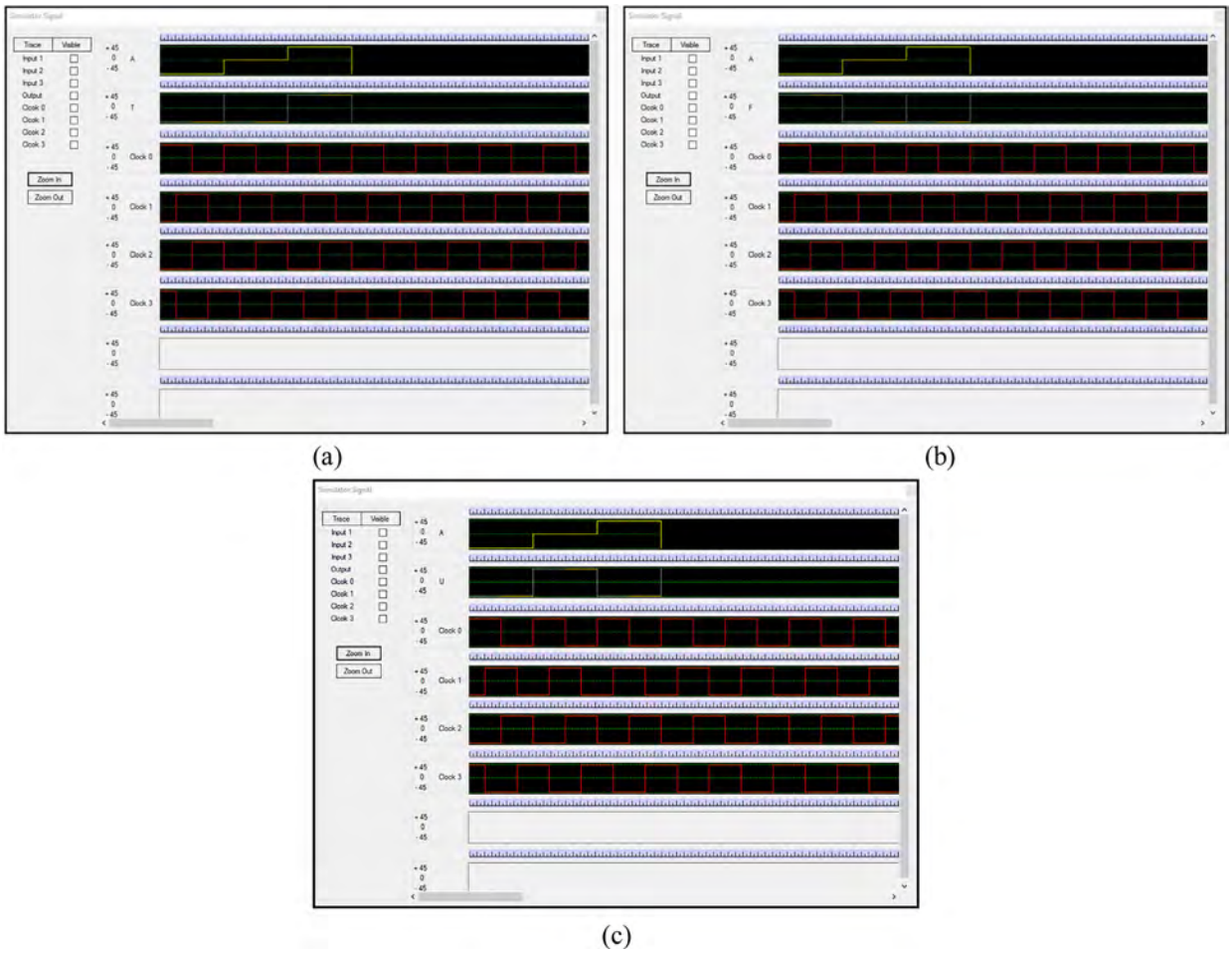



**Fig. 9.** Simulation results of ternary decoder (a) true (b) false (c) unknown gates.

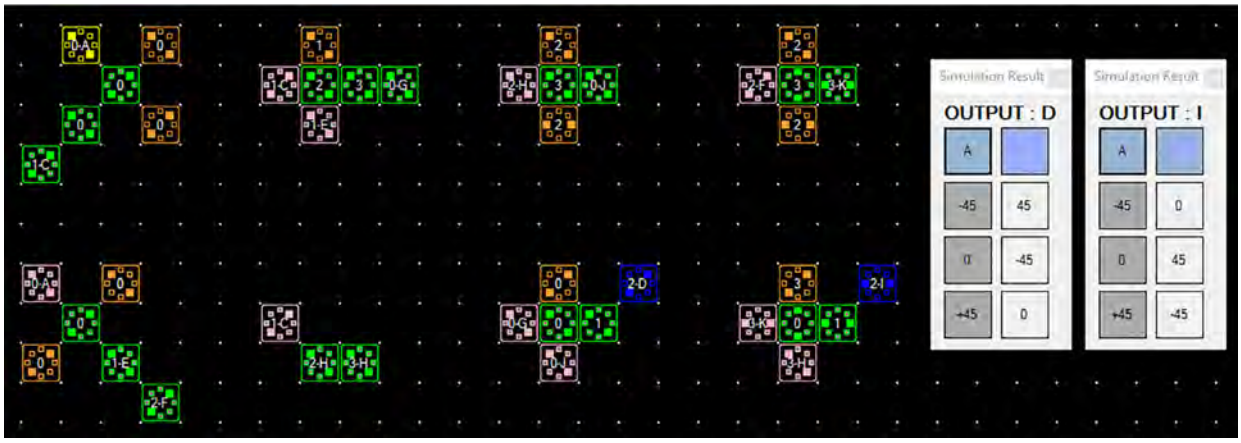



**Fig. 10.** Proposed ternary increment and decrement and their truth tables.

Area occupations of a circuit is an important assessment metrics, therefore, total area of each circuit should be evaluated. For the proposed decoder, total area is 0.012 μm$^2$. Another item which should be considered is the cost of the circuit. The cost function of ternary logic circuits can be expressed as follows [18]:

$$Cost = Area \times Delay \times Power \tag{4}$$

The first term of this equation is area which, previously calculated for the proposed decoder. The second term is delay. Clearly, delay is the time interval between the first input signal enters the circuit and it arrives at the output. This item can be determined by the number of clocking cycle (four phases). According to Fig. 9, delay of the proposed decoder is 1 clock cycle. The third term of the mentioned equation is power. In QCA, power dissipation is ultra-low and negligible though, it may cause thermal challenges. A low power consumption QCA circuit is a circuit with low energy dissipation. However, Ref. [19] indicates that power has a direct relation to complexity. Hence, we used complexity (number of cells) in this equation. In the proposed decoder, 19 cells are used. Due to the mentioned parameters and Eq. (4), the total cost of the proposed ternary decoder is:

$$Cost_{Decoder} = Area \times Delay \times Complexity = 0.012 \times 1 \times 19 = 0.228 \tag{5}$$

Due to the performance consideration of the QCA circuit, total power consumption is another significant item [19]. Clock should provide the required power of the circuit which leads the circuit to work properly. As we know, power has a direct relation to energy. To calculate the energy consumption of the circuit, intracellular and extracellular energies should be considered. In our previous work [10], we showed that, the internal energy is a fixed value for each ternary whilst we calculated all the possible states of extracellular energies. Using these values, energy consumption of the proposed decoder can be calculated as follows:

$$Total\ Energy\ Consumption = (E_{internal} \times Cell\ Number) + E_{external} \tag{6}$$

$$Energy\ Consumption_{Decoder} = (4.612 \times 10^{-20} \times 19) + 1.574 \times 10^{-20} = 89.202 \times 10^{-20}(J) = 5.568(ev) \tag{7}$$

### 5.2. Ternary increment and decrement (Cycle)

Ternary increment and decrement have been called ‘inverse cycle’ or ‘rotate up/down’. Using inverse cycle helps us arrange ternary values in a cyclic order. According to Eq. (8), the ternary increment is a right shift function and the ternary decrement is a left shift one. The proposed ternary increment and decrement and their truth tables are illustrated in Fig. 10. Note that, the output *I* and output *D* indicate increment and decrement gates, respectively. As shown in this figure, a decoder, two clamp down and two Antimax gates are used to implement cycle gates. Moreover, the related clock simulation displays in Fig. 11.

$$\begin{aligned} Output_{increment} &= (A + 1) \\ Output_{decrement} &= (A - 1) \end{aligned} \tag{8}$$

For the proposed cycle (increment and decrement together), total area is 0.03 $\mu m^2$. According to the cost function (Eq. (4)), number of cells of the proposed cycle is 43 and as shown in Fig. 11, the latency of this circuit is 3 clock cycle. Hence, the total cost of the proposed ternary cycle is as follows:

$$Cost_{Cycle} = 0.03 \times 3 \times 43 = 3.87 \tag{9}$$

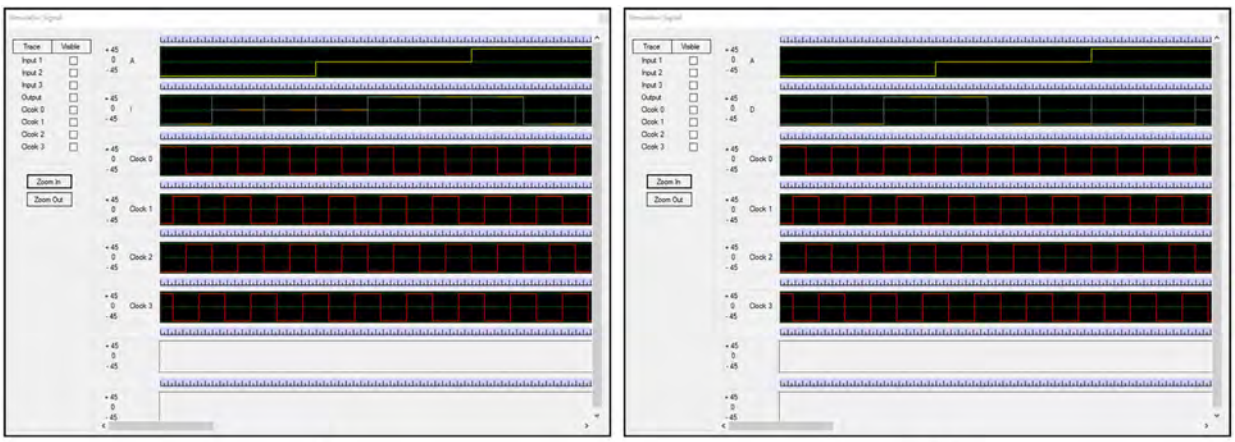



**Fig. 11.** Simulation results of ternary cycle (a) increment (b) decrement.

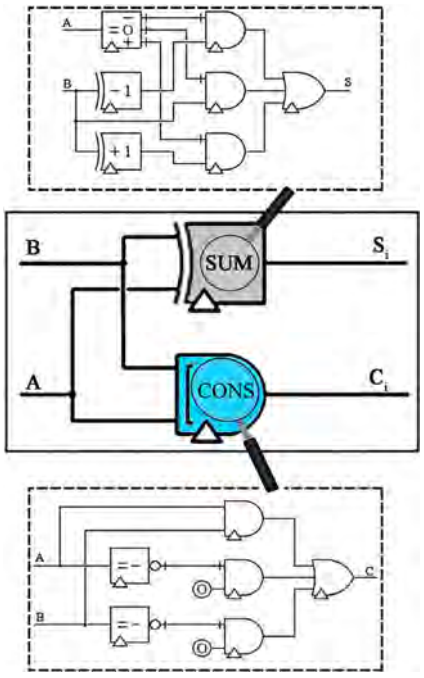



**Fig. 12.** Schematics of ternary half adder [40].

Energy consumption of this circuit is calculated as follows:

$$Energy\ Consumption_{Cycle} = (4.612 \times 10^{-20} \times 43) + 4.892 \times 10^{-20} = 203.208 \times 10^{-20}(J) = 12.683(ev) \quad (10)$$

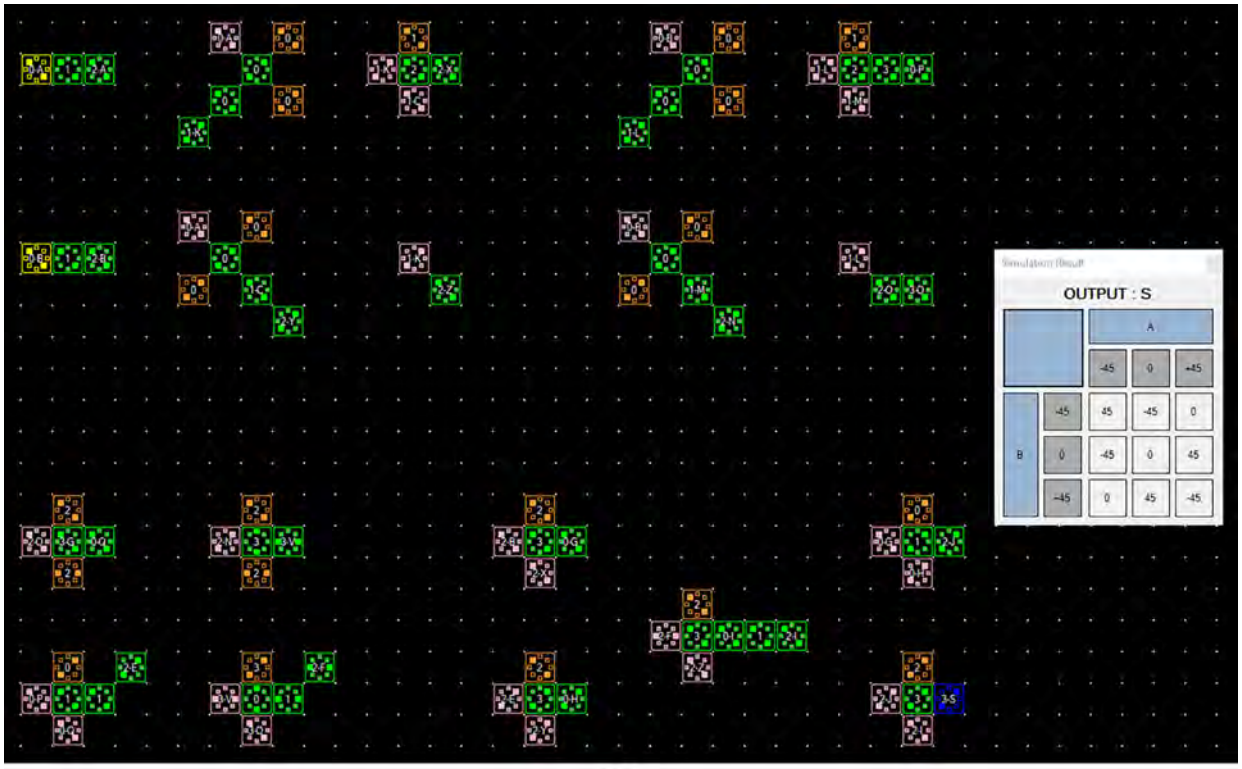
### 5.3. Ternary half adder

Based on the above introduced logic gates, to build a balanced ternary half adder which is a two-input two-output circuit, various structures can be exploited. For instance, in one of these structures, two Min gates, a Max gate, and an inverter are used [20]. Other architectures such as multiplexer [21] or optical ternary logic [22] are exploited to realize half adder functions. Here, we implement another structure of a half adder [23] which is shown in Fig. 12. It is noteworthy that, the sum function in ternary is the same as the sum function in binary and a ternary consensus is identical to the carry function (Eq. (11)). As can be seen in Fig. 12, the sum gate comprises a decoder, an increment, a decrement, a Max and three Min gates. Moreover, the consensus circuit includes two NTI gates, a Min, a Max and two clamp down gates and standard inverter. All these components -mentioned gates- were implemented earlier. Implementation of the proposed ternary half adder –sum and cons gates- and the related truth tables depicted in Fig. 13, while the clock simulation is presented in Fig. 14.

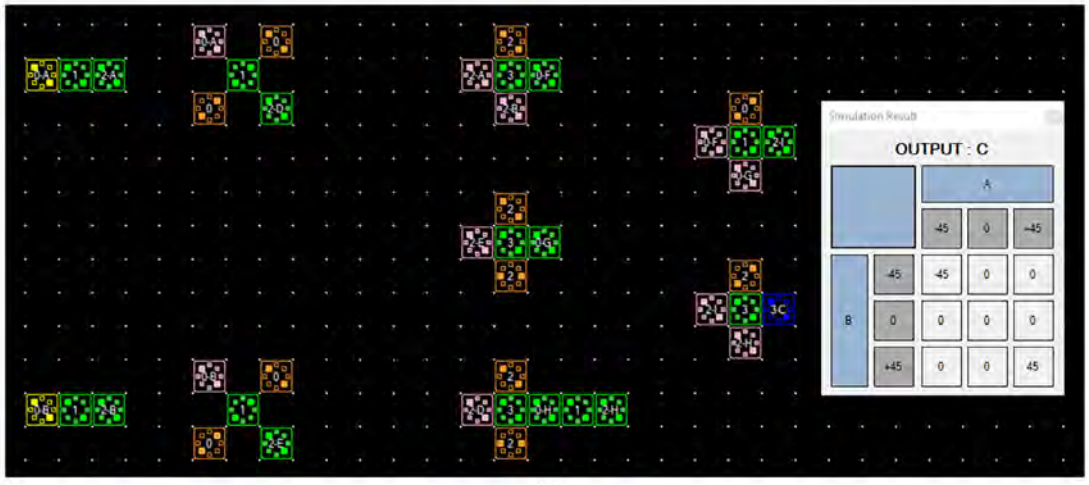
$$\begin{aligned} Output_{Sum} &= S_i = (A + B) = ((A = -1) \wedge (B - 1)) \vee ((A = 0) \wedge (B)) \vee ((A = +1) \wedge (B + 1)) \\ Output_{Consensus} &= C_{i+1} = (A \boxtimes B) = Cons(A, B) = (A \wedge B) \vee ((A \neq -1) \wedge 0) \vee ((B \neq -1) \wedge 0) \end{aligned} \quad (11)$$

Area consumption of the proposed sum and cons circuits are 0.091 $\mu m^2$ and 0.039 $\mu m^2$, respectively. Furthermore, number of cells in sum circuit is 95 and number of cells in cons circuit is 43. It is also clear from Fig. 14, that the proposed sum and cons circuit can be achieved in 3 clock cycle. Thus, the cost of these circuits can be calculated using the obtained values (Eq. (12)).

$$\begin{aligned} Cost_{Sum} &= 0.091 \times 3 \times 95 = 25.935 \\ Cost_{Cons} &= 0.039 \times 3 \times 43 = 5.031 \end{aligned} \quad (12)$$




(a)




(b)

**Fig. 13.** Implementation of the proposed ternary half adder and their truth tables (a) sum (b) cons.

Total energy consumption of these circuits is calculated in Eq. (13).

$$\begin{aligned} \textit{Energy Consumption}_{Sum} &= (4.612 \times 10^{-20} \times 95) + 12.485 \times 10^{-20} = 450.625 \times 10^{-20}(J) = 28.126(ev) \\ \textit{Energy Consumption}_{Cons} &= (4.612 \times 10^{-20} \times 43) + 5.15 \times 10^{-20} = 203.466 \times 10^{-20}(J) = 12.699(ev) \end{aligned} \tag{13}$$

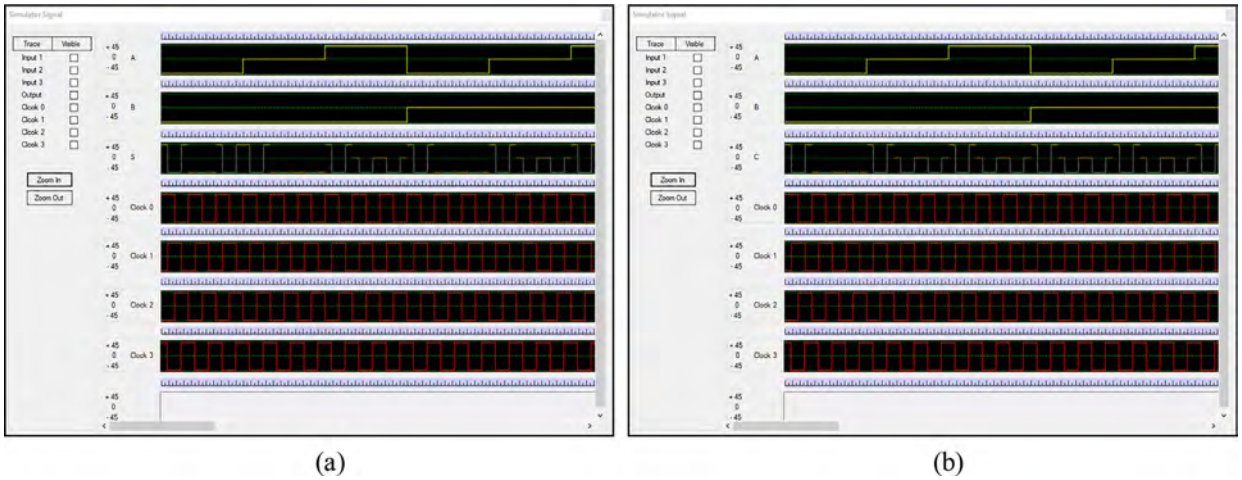



**Fig. 14.** Simulation results of ternary half adder (a) sum (b) cons.

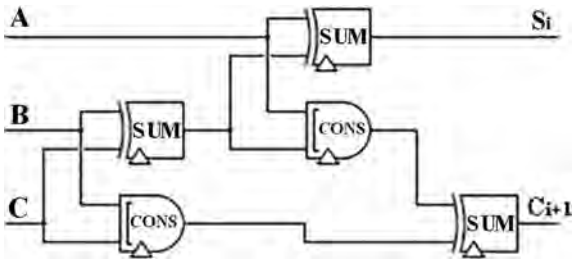



**Fig. 15.** Schematic of the ternary full adder.

### 5.4. Ternary full adder

A ternary full adder is a three-input two-output circuit and as can be seen in Fig. 15, contains two ternary half adders that are joined together by an ANY (Accept Anything) gate or sum gate. It worth noting that, the truth tables of ANY and sum (Fig. 13(a)) are similar to each other except when both inputs are equal. Since, the outputs of two Cons gates can never be + 1 and −1 at the same time, in a full adder circuit, we can use both of these gates. We used sum gate in the mentioned full adder. Implementation of this full adder and the related truth table are illustrated in Figs. 16 and 17, respectively. Note that, $S_i$ and $C_{i+1}$ outputs (Fig. 15), are specified by $S_3$ and $S_5$ (Fig. 17), respectively. In addition, the clock simulations of these circuits are represented in Fig. 18(a) and (b).

The total area of the proposed full adder is 0.51 $\mu m^2$ and 352 cells are used in this circuit. According to Fig. 18, the delay is 9 clock cycle. Hence, the cost of the proposed full adder can be calculated as follows:

$$Cost_{Full\ Adder} = 0.51 \times 9 \times 352 = 1615.68 \tag{14}$$

Comparing the obtained cost with others [24,25], it can be concluded that the proposed full adder occupied less area and less cell number. Consequently, the cost of our proposed ternary full adder shows a relative improvement as compared to analogous binary full adders.

### 5.5. Ternary half subtractor

A ternary half subtractor circuit has two inputs and two outputs (difference and borrow). These outputs are similar to the outputs of the ternary half adder (sum and carry). The difference output is responsible for subtract the inputs while the borrow output is related to carry digit. Implementation of the ternary half subtractor and the related truth tables are displayed in Fig. 19(a) and (b),

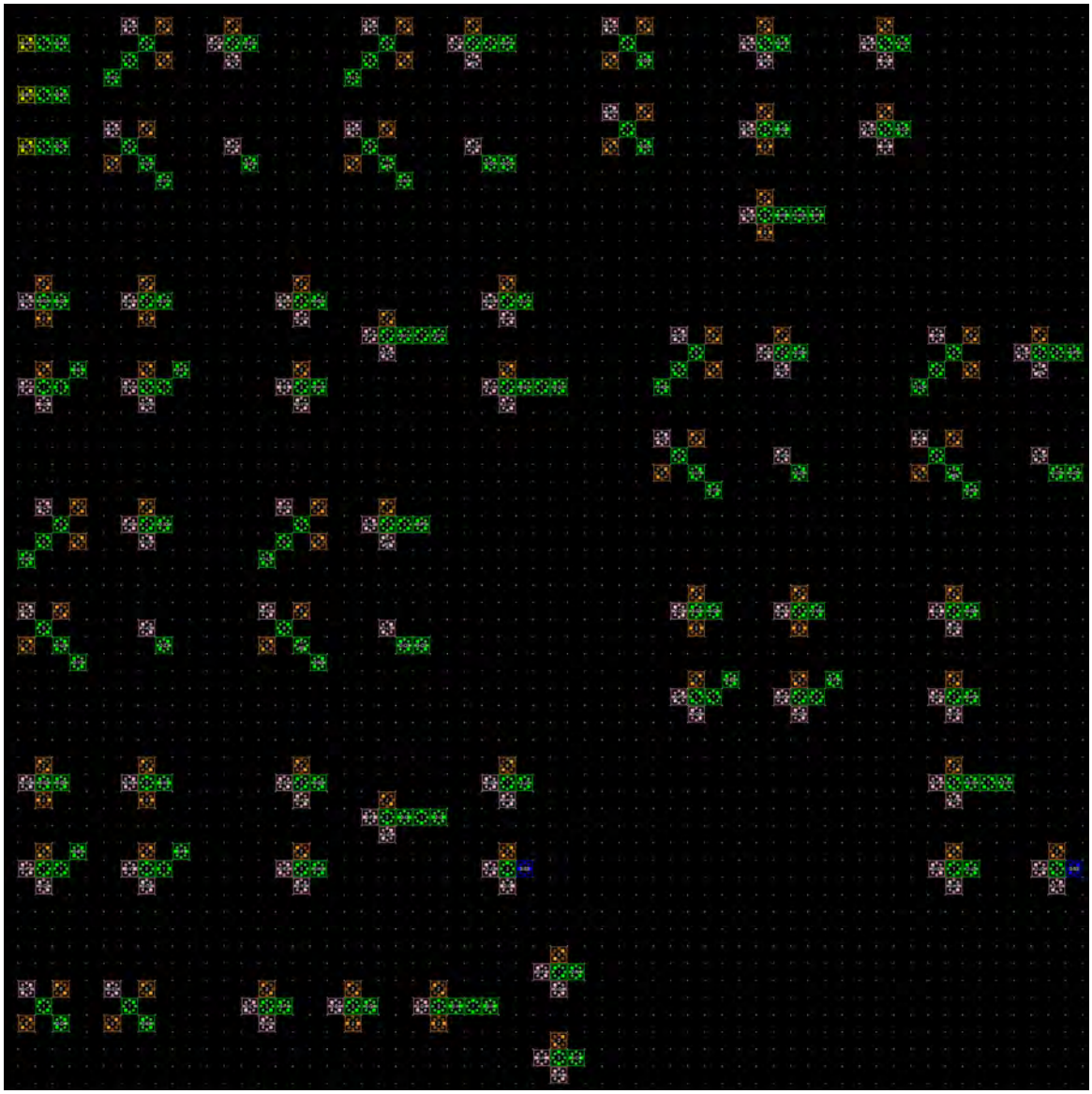


**Fig. 16.** Implementation of the proposed ternary full adder.

Simulation Result

OUTPUT : S3

| B1 \ A1 | C1 = -45 | | | C1 = 0 | | | C1 = +45 | | |
|---|---|---|---|---|---|---|---|---|---|
| | -45 | 0 | +45 | -45 | 0 | +45 | -45 | 0 | +45 |
| -45 | 0 | 45 | -45 | 45 | -45 | 0 | -45 | 0 | 45 |
| 0 | 45 | -45 | 0 | -45 | 0 | 45 | 0 | 45 | -45 |
| +45 | -45 | 0 | 45 | 0 | 45 | -45 | 45 | -45 | 0 |

(a)

Simulation Result

OUTPUT : S5

| B1 \ A1 | C1 = -45 | | | C1 = 0 | | | C1 = +45 | | |
|---|---|---|---|---|---|---|---|---|---|
| | -45 | 0 | +45 | -45 | 0 | +45 | -45 | 0 | +45 |
| -45 | -45 | -45 | 0 | -45 | 0 | 0 | 0 | 0 | 0 |
| 0 | -45 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 45 |
| +45 | 0 | 0 | 0 | 0 | 0 | 45 | 0 | 45 | 45 |

(b)

**Fig. 17.** Truth tables of the proposed ternary full adder: (a) $S_3$ output (b) $S_5$ output.

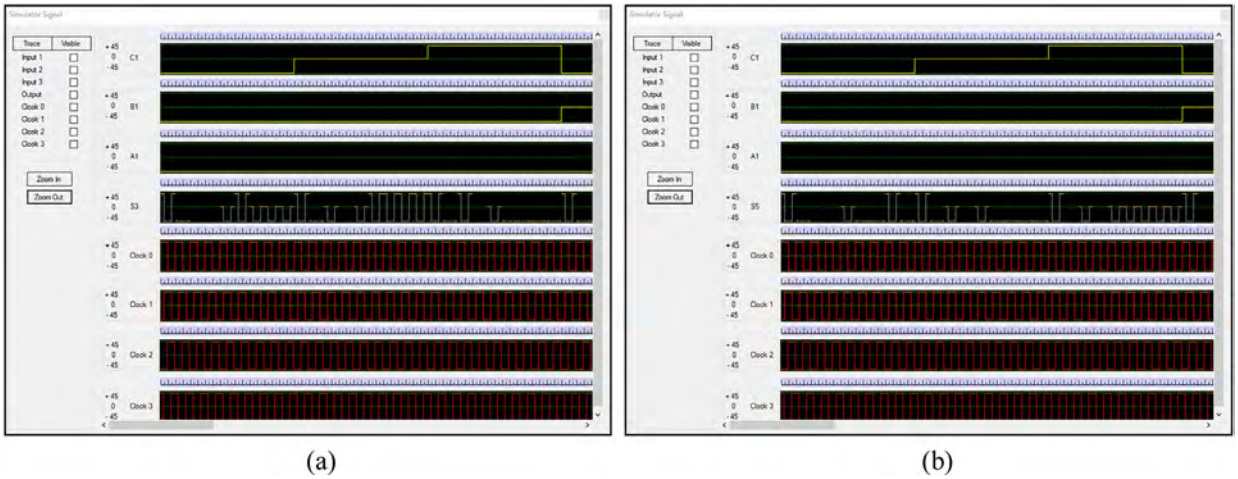



**Fig. 18.** Simulation results of ternary full adder: (a) $S_3$ output (b) $S_5$ output.

respectively. As can be seen, for having ternary half subtractor, input *B* of the proposed ternary half adder is inverted. In addition, the clock simulation of difference and borrow are illustrated in Fig. 20(a) and (b), respectively.

Due to the similarity between the proposed ternary half adder and half subtractor, total area, number of cells and energy consumption of these circuits are the same. According to Fig. 20, delay of difference and borrow circuits are 4 clock cycle. Hence, cost of these circuits can be considered as follows:

$$Cost_{Difference} = 0.091 \times 4 \times 95 = 34.58$$
$$Cost_{Borrow} = 0.039 \times 4 \times 43 = 6.708 \quad (15)$$

### 5.6. Ternary full subtractor

In ternary full subtractor that is a three-input and two-output circuit, input *B* is inverted in comparison with the proposed full adder. This circuit and the related truth tables are shown in Figs. 21 and 22, respectively while the clock simulation is depicted in Fig. 23.

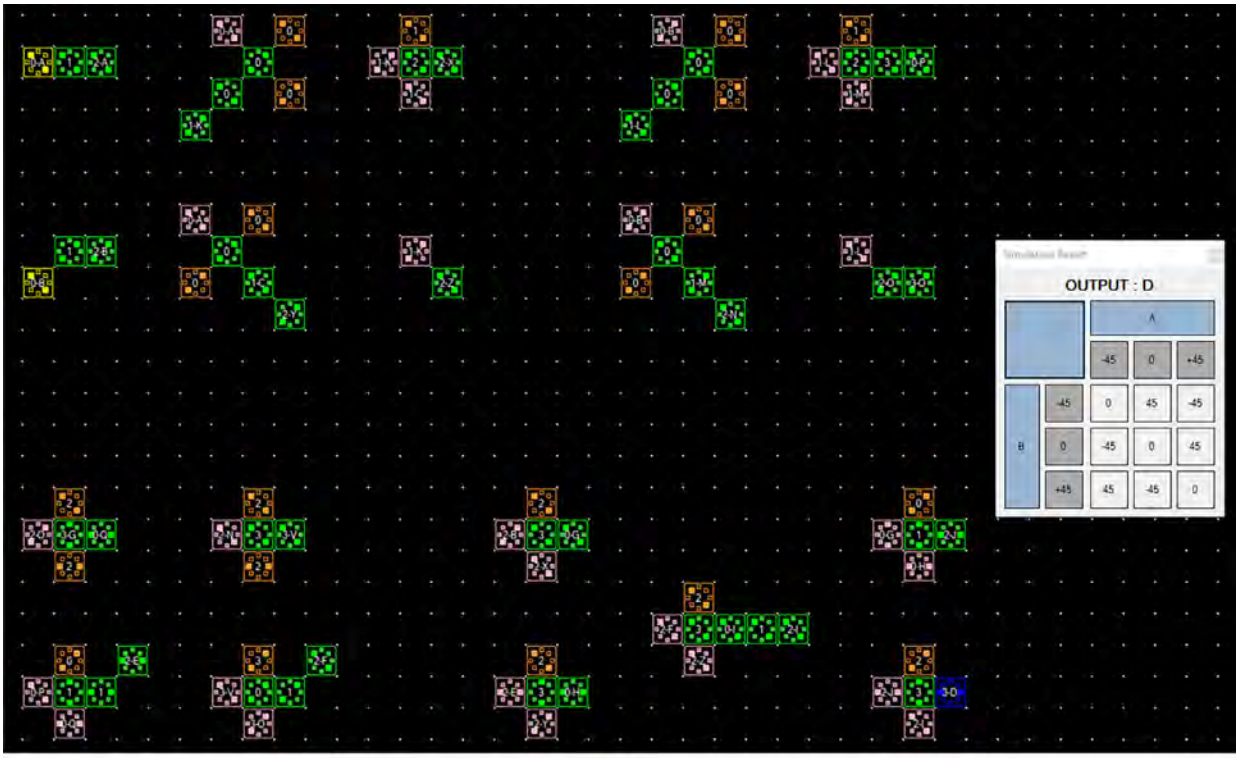
According to the mentioned similarity between the proposed ternary full adder and full subtractor, total area and number of cells of these circuits are the same. As shown in Figs. 23 and 10 clock cycle delay is considered. Thus, the cost function of this circuit can be calculated as follows:

$$Cost_{Full\ Subtractor} = 0.51 \times 10 \times 352 = 1795.2 \quad (16)$$

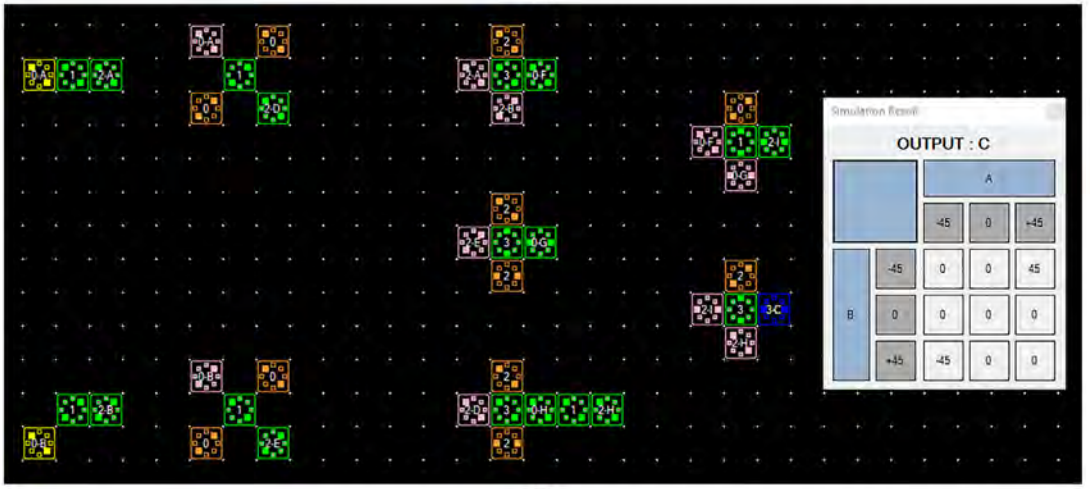
The proposed full subtractor has less area and cell number as compared to that reported for binary one [24].

## 6. Conclusion

We have demonstrated an alternative model for implementing ternary logic circuits and to ascertain our model capability in digital circuits, a novel simulation method is accomplished. This model which is presented earlier is based on the electron-electron interactions and their energy calculations in ternary cells and it can effectively solve the problems of ternary logic QCAs structures. Exploiting the proposed model, the basic ternary gates -such as Min, Max and various kind of inverters- and subsequently combinational ternary circuits -such as a decoder, cycle, adder, and subtractor- are designed and simulated. Based on the final observation, it is concluded that the correct value for the output and accurate clock simulation is achieved. In addition, prominent items such as area, energy consumption, cost function, defect, and fault tolerant are considered in the proposed circuits. Furthermore, no counterexample was found among the outcomes. These investigations reveal that the proposed model appears to be logical, hence, it is possible to design any ternary logic circuits by use of the proposed model.




(a)




(b)

**Fig. 19.** Implementation of the proposed ternary half subtractor and their truth tables: (a) difference (b) carry (borrow).

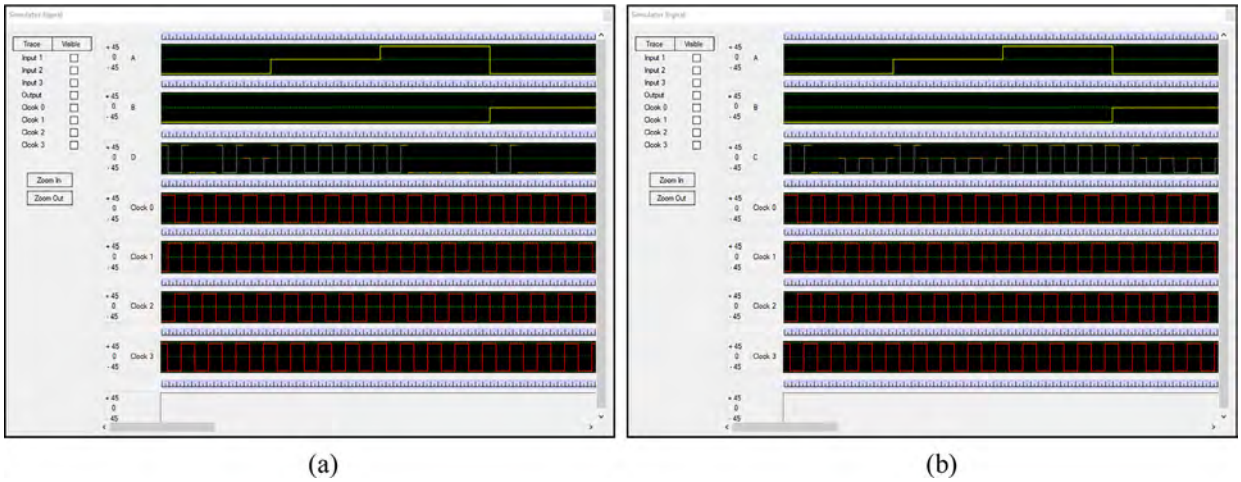



**Fig. 20.** Simulation results of ternary half subtractor: (a) difference (b) carry (borrow) .

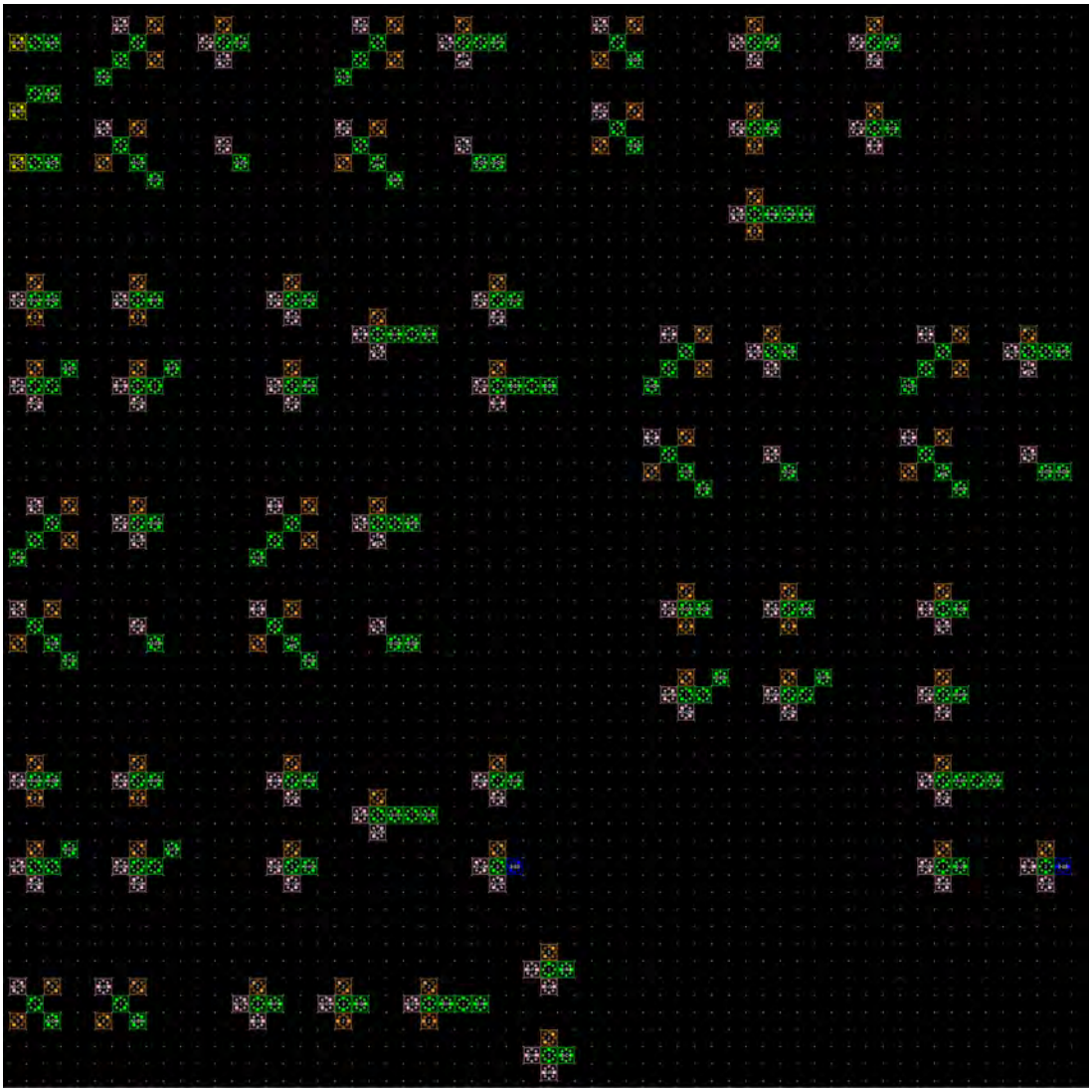


**Fig. 21.** Implementation of the proposed ternary full subtractor .


**Fig. 22.** Truth tables of the proposed ternary full subtractor: (a) $S_3$ output (b) $S_5$ output.

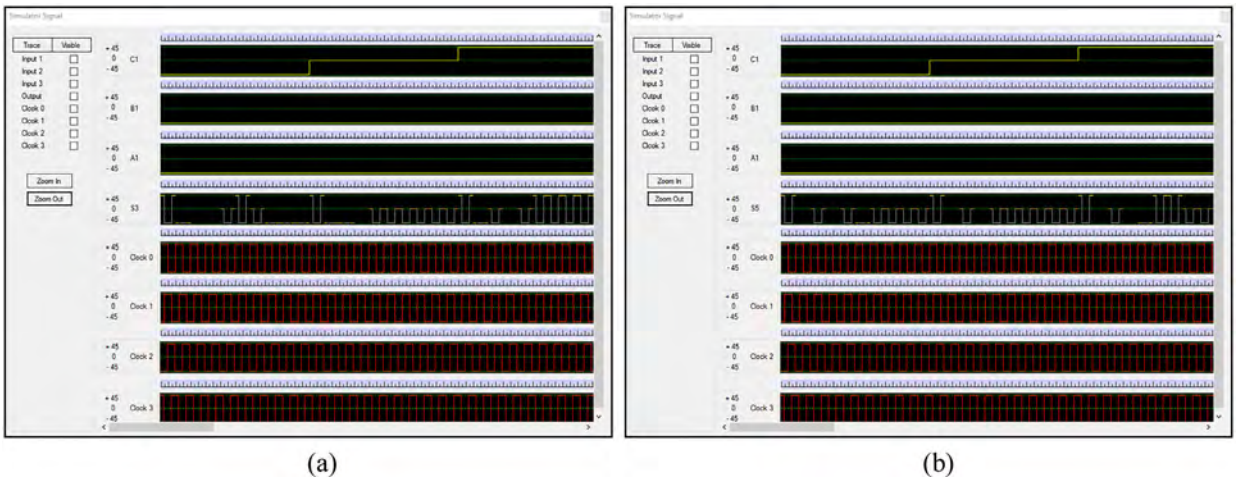



**Fig. 23.** Simulation results of ternary full subtractor: (a) $S_3$ output (b) $S_5$ output.

## Acknowledgment

This work was supported by IPM grant.

## References

[1] Lent CS, Tougaw PD, Porod W, Bernstein GH. Quantum cellular automata. Nanotechnology 1993;4(1):49–57.
[2] Mohammadi M, Niknafs A, Eshghi M. Controlled gates for multi-level quantum computation. Quantum Inf Process 2011;10(2):241–56.
[3] Bajec IL, Zimic N, Mraz M. The ternary quantum-dot cell and ternary logic. Nanotechnology 2006;17(8):1937–42.
[4] Pecar P, Ramsak A, Zimic N, Mraz M, Bajec IL. Adiabatic pipelining: a key to ternary computing with quantum dots. Nanotechnology 2008;19(49):495401.
[5] Pecar P, Mraz M, Zimic N, Janez M, Bajec IL. Solving the ternary QCA logic gate problem by means of adiabatic switching. J Appl Phys 2008;47(6):5000–6.
[6] Pecar P, Janez M, Zimic N, Miha M, Bajec IL. The ternary quantum-dot cellular automata memorizing cell. 2009.
[7] Janez M, Bajec IL, Pecar P, Jazbec A, Zimic N, Mraz M. Automatic design of optimal logic circuits based on ternary quantum-dot cellular automata. World Sci Eng Acad Soc 2008;7(9):919–28.
[8] Tehrani MA, Bahrami S, Navi K. A novel ternary quantum-dot cell for solving majority voter gate problem. Appl Nanosci 2013;4(3):255–62.
[9] Tehrani MA, Navi K. A novel quantum-dot cellular automata for implementation of multi-valued logic. Paper presented at the nano today conference. Elsevier; 2009.
[10] Mohaghegh SM, Sabbaghi-Nadooshan R, Mohammadi M. Innovative model for ternary QCA gates. IET Circ Devices Syst 2018;12(2):189–95.
[11] Malinowski G. Kleene logic and inference. Bull Sect Logic 2014;43(1/2):43–52.
[12] Lombardi F, Huang J. Design and test of digital circuits by quantum-dot cellular automata. Artech House Publishers; 2007. p. 46–9. p.
[13] Imre A. Experimental study of nanomagnets for magnetic quantum-dot cellular automata (MQCA) logic applications. University of Notre Dame; 2005.
[14] Snider GL, Orlov AO, Kummamuru RK, Ramasubramaniam R, Amlani I, Bernstein GH, et al. Quantum-dot cellular automata: Introduction and experimental overview. Nanotechnology, IEEE-NANO 2001. Proceedings of the 2001 1st IEEE conference. IEEE; 2001.
[15] Khani M, Sabbaghi-Nadooshan R. Ternary quantum-dot cellular automata simulator software. 2017http://tqca.ir [accessed].
[16] Levi AFJ. Applied quantum mechanics. 2nd ed. Cambridge University Press; 2006. p. 192–3.
[17] Tahoori MB, Momenzadeh M, Huang J, Lombardi F, editors. Defects and faults in quantum cellular automata at nano scale. VLSI Test Symposium, 2004

Proceedings 22nd. IEEE; 2004. IEEE.
[18] Oklobdzija VG. The computer engineering handbook. CRC press; 2001. p. 81–6.
[19] Srivastava S, Sarkar S, Bhanja S. Estimation of upper bound of power dissipation in QCA circuits. IEEE Trans Nanotechnol 2009;8(1):116–27.
[20] Shamshad A, Mansaf A. Balanced-ternary logic for improved and advanced computing. Int J Comput Sci Inf Technol 2014;5(4):5157–60.
[21] Giri S, Saraswathi N. Implementation of combinational circuits using ternary multiplexer. Int J Comput Eng Res 2008;2(2):457–63.
[22] Roy JN, Bhowmik P, Chattopadhyay T. Design of all optical ternary logic based half adder circuit and it's applications. J Opt 2015;44(4):322–9.
[23] Jones DW. Standard ternary logic. 2012http://homepage.divms.uiowa.edu/~jones/ternary/logic.shtml.
[24] Gladshtein M. Quantum-dot cellular automata serial decimal adder. IEEE Trans Nanotechnol 2011;10(6):1377–82.
[25] Cho H, Swartzlander Jr EE. Adder and multiplier design in quantum-dot cellular automata. IEEE Trans Comput 2009;58(6):721–7.

**Saman Mohammadi Mohaghegh** received her B. Sc. and M. A. degrees in electrical engineering from Islamic Azad University Central Tehran Branch, Tehran, Iran, in 2008 and 2012, respectively. She is a Ph.D. student in electrical engineering in Islamic Azad University Arak Branch since 2013. Her research interests include digital electronics such as quantum cellular automata and multi valued logic.

**Reza Sabbaghi-Nadooshan** received the M.S. degree in electrical engineering from the Iran University of Science and Technology in 1994 and the Ph.D. degree in electrical engineering from the Science and Research Branch, Islamic Azad University in 2010. Now he is Associate Professor of Electronics Department in Central Tehran branch, Islamic Azad University. His research interests include QCA and Nanocomputing.

**Majid Mohammadi** received the Ph.D. degree in Computer engineering from the Shahid Beheshti University, Tehran, Iran in 2009. Now he is Associate Professor of Department of Computer Engineering in Shahid Bahonar University of Kerman, Kerman, Iran. His current research interests include reversible gates, QCA and Nanocomputing.