A 6-bit, 1-GS/s, 9.9-mW, Interpolated Subranging ADC in 65-nm CMOS

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***Abstract*—A 6-bit, 1-GS/s subranging analog-to-digital converter (ADC) implemented in 65-nm CMOS is developed. The same capacitor DACs (CDACs) are used to sample the analog signals, thereby eliminating the errors between the coarse and fine decisions that occur when two different samplers are used to capture the signal. Both decisions use the same comparators, and a digitally assisted calibration circuit compensates for the errors in the different threshold levels used for the two decisions. This calibration eliminates redundant comparators, and thus, reduces the area. Reference voltages generators, which are implemented using resistor ladders in conventional subranging ADCs, are eliminated thanks to the use of the CDACs together with interpolation in the comparators. This solves two problems related to the resistor ladder, namely, the trade-off between the settling time and the static-current consumption and signal dependent on-resistance of switches connected to intermediate potential nodes. A test chip fabricated in 65-nm CMOS technology operates at 1 GS/s with SNDR of 32.8 dB. Its active area is 0.044 mm^2, and its power consumption is 9.9 mW at a 1.1-V supply voltage.**

***Index Terms*—Analog–digital conversion, CMOS analog integrated circuits, foreground calibration, interpolation, subranging.**

I. Introduction

HIGH-SPEED analog-to-digital converters (ADCs) with around 6-bit resolution have been used for oscilloscopes and the read channels of data-storage devices (such as HDDs and DVD drives) since the 1990s [1], [2]. Currently, such ADCs are used in Ethernet, electrical wire-line links, and optical communication systems [3]. Flash ADCs are traditionally used for these applications because of their high operation speed. However, flash ADCs have a drawback: their area and power consumption increase exponentially with the resolution [4]. In addition, because the number of the comparators increases, the input capacitance of the ADC becomes larger, and this often restricts performance [5]. A time-interleaved successive approximation register (SAR) architecture have been used to address these issues and attain conversion speeds of several tens of GS/s [6]. However, although an SAR ADC has high power efficiency, the overall performance deteriorates as the number of time-interleaved channels grows, because the clock delivery needs to cover a larger area and clock timing accuracy becomes critical at a high conversion rate. Subranging architectures have coarse and fine decisions wherein the conversion range of the fine decision is determined according to the coarse decision result. This architecture potentially gives a conversion speed, area, and power that are roughly half way between those of flash ADC and SAR ADC. The subranging architecture can thus minimize the problems that arise from the large area of time-interleaved SAR ADCs [6]. To achieve this end, several issues should be addressed. One is that the conversion speed and resolution are limited by the settling time of the reference voltages, because the conventional subranging architecture uses reference resistor ladders to generate various threshold voltages for the coarse and fine decisions. Additionally, the use of different samplers for the coarse and fine decisions [4] causes sampling errors between decisions. Since the sampling errors cannot be compensated for by calibrating the comparators, redundant comparators are needed [7]. To solve these problems, this paper proposes a scheme in which the reference voltages for coarse and fine decisions are generated without using resistive ladders. The proposed scheme eliminates the sampling error by using the same CDACs to capture the input signal for both decisions. In addition, a calibration technique is used to reduce the error caused by the offset voltages of comparators. These measures enable the use of the same comparators for both decisions without any redundant comparators and further reduce the ADC area. Section II of this paper explains the design issues concerning the conventional subranging architecture and the proposed interpolated subranging ADC. Section III describes the circuit implementation of a 6-bit ADC and its calibration method. The results of the measurement of a test chip are presented in Section IV. Section V presents the conclusion.

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II. Subranging ADCs

A. Issues With Conventional Subranging ADCs

The operating principle of subranging ADCs is schematically illustrated in Fig. 1 by taking a structure that performs 2-bit coarse and 2-bit fine decisions as an example. First, comparators for the coarse decision convert the analog input signal into a 2-bit digital output signal, specifying in which of the four ($= 2^2$) subranges the input signal lies. Next, the reference voltages for the fine decision are set to the fine-decision comparators such that the conversion range of the fine conversion coincides with the subrange determined by the coarse decision. The fine decision is then made at a fine-decision resolution of 2 bits, resulting in 4-bit ($= 2 + 2$) overall resolution. In the example

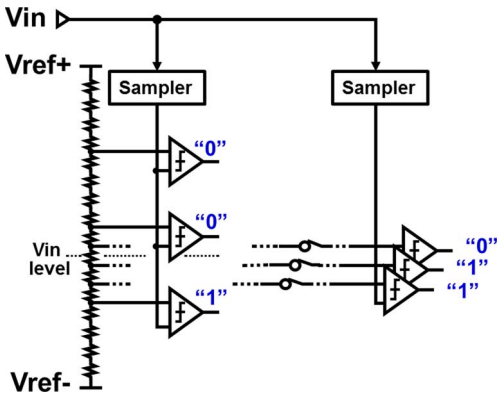

Fig. 1. Block diagram of operation of a 2-bit + 2-bit subranging ADC.

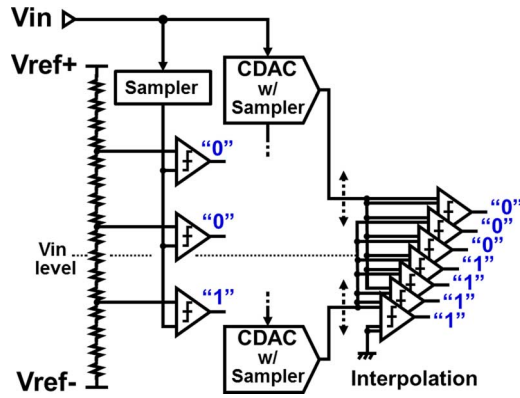

Fig. 2. Block diagram of the conventional circuit with the interpolation scheme.

ADC, the samplers for the coarse and fine decisions sample the analog input signal independently, and this causes errors between decisions due the samplers' gain and timing variations [4]. Another problem arises because a resistor ladder generates the reference voltages of the comparators [8]. Since the ladder nodes are at intermediate potentials rather than VDD or GND, the on-resistances of the switches are high, and these increase the settling time after switching to the fine reference voltage. Although increasing the transistor size of the switch could reduce the switch's on-resistance, the additional parasitic capacitances, and larger clock feed-through and charge injection effects restrict the performance of the ADC [9]. The reference ladder resistance cannot be reduced too much because the static current of the ladder will increase. Alternatively, large on-chip capacitances connecting the ladder nodes to VSS or VDD would reduce the ac output impedance of the ladder but would also enlarge the area.

B. Conventional Subranging ADC With CDACs

In order to resolve the issues found in the switches connected to intermediate potential nodes, CDACs have been used together with an interpolation technique for making the fine decisions [10] (Fig. 2). In this scheme, the switches used for generating a reference voltage in the CDAC are connected to either VDD or GND, not to an intermediate voltage of the resistive ladder. In addition, by using an interpolation technique, only two CDACs are needed to drive all of the comparators when performing the fine decision. Although the settling-time issues due to the resistive ladders are eliminated in the fine decision in [10], different samplers are used for the coarse and fine decisions. Thus sampling errors between the decisions would occur and redundancy is still needed.

C. Proposed Subranging Architecture

In the proposed subranging ADC (Fig. 3), the input signal is sampled into the capacitors of CDACs once, and the same sampled charge is used for the coarse and fine decisions. Interpolating the CDACs' outputs in the comparators generates threshold levels for both decisions, eliminating resistive ladder altogether. Also, the same comparator array performs the coarse and fine decisions by using a calibration setting dedicated for each decision, and this reduces the area occupied by the comparators.

The comparator array consists of seven dynamic-latch comparators that share their inputs and generates a seven-bit thermometer code. Each comparator uses two input-differential pairs to form a weighted sum of the input signals before the comparison. As explained in Section III-B, the comparator's threshold level is determined by the weights of the sum, which is implemented by sizing the input devices.

The switch control circuits control the switches in the CDACs by using the state signals ϕS, ϕHC and ϕHF. The control circuits also refer to the output of the comparator array T1 to T7 obtained in the coarse decision in order to generate appropriate threshold levels for the fine decision. Signals ϕS, ϕHC and ϕHF are generated by a clock-generator circuit (CLK Gen.) on the basis of a 2-GHz input clock signal, CLK. Signal ϕS has a frequency of 1 GHz with a duty ratio of 25%, ϕHC has 1 GHz and 25%, and ϕHF has 1 GHz and 50% (Fig. 4).

During the sampling period, in which ϕS is "H," ϕHC is 'L' and ϕHF is "L," the input analog signal is sampled by the CDACs. During the coarse decision period, in which ϕS is "L," ϕHC is "H" and ϕHF is "L," the CDACs generate voltages for the coarse decision. The comparators are then activated and the coarse decision results, T1 to T7, are produced. During the fine-decision period, in which ϕS is L, ϕHC is L, and ϕHF is H, the voltage for the fine decision is generated by the CDACs by using T1 to T7. Finally, the comparators are activated again to perform the fine decision, and the output signals from the coarse and fine decisions are synchronized and converted into a 6-bit binary code Dout, which is the output of the ADC. Code TH_CNTL controls the threshold level of each comparator and is comprised of a code DTC for the coarse decision and a code DTF for the fine decision.

III. Circuit Implementation

A. CDAC

To generate an appropriate reference level in the comparator, two differential CDACs, i.e., CDACU and CDACL, each of which is composed of two single-ended CDACs (Fig. 5) are used. CDACU is composed of $\mathrm{CDACU\_P}$ and $\mathrm{CDACU\_N}$, and CDACL is composed of $\mathrm{CDACL\_P}$ and $\mathrm{CDACL\_N}$. Although the analog signal path is fully differential, as can be seen in Figs. 5 and 6, single-ended representations referring to positive

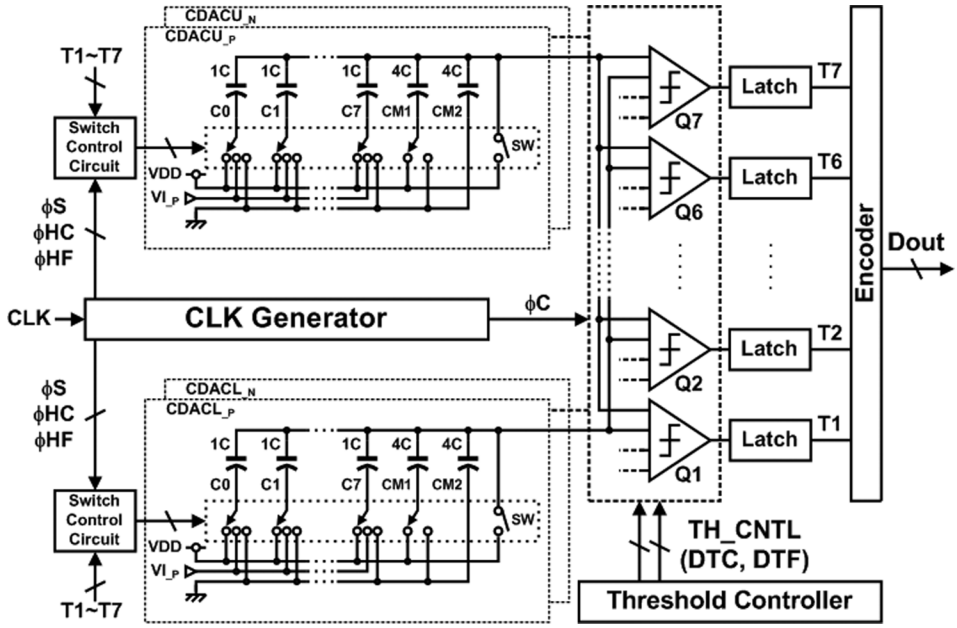

Fig. 3. Block diagram of the proposed ADC.

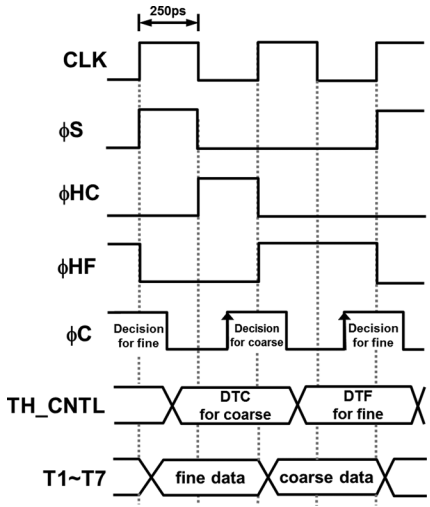

Fig. 4. Timing diagram of the proposed ADC.

half circuits are often used for simplicity. When needed, a suffix _P or _N are used to specify to whether a positive or negative half circuit is being referred.

Each CDAC is composed of eight unit capacitors, C0 to C7, a reset switch SW, and capacitors CM1 and CM2 for generating the common-mode voltage. The top plates of C0 to C7 and CM1 to CM2 are connected to the CDAC output node. SW is placed between the output node of the CDAC and VDD. The bottom plates of C0 to C7 are connected to either one of VDD, GND, or the input signal VI, through switches controlled by the switch-control circuit, which itself is controlled by ϕS, ϕHC, ϕHF, and T1 to T7. The nominal capacitance of C0 to C7 is 1C, and the nominal capacitance of CM1 and CM2 is 4C. The unit capacitance of the proposed ADC is large enough (1C = 5 fF) that the CDAC can endure the mismatch and kT/C noise.

During the sampling period, the reset switch SW turns on, connecting the top plates of C0 to C7 and CM1 to CM2 to VDD. Therefore, VU and VL, which are the voltages of the output nodes of CDACU and CDACL, become VDD. The bottom plates of C0 to C7 are connected to the signal input node VI, and the bottom plates of CM1 and CM2 are connected to VDD and GND, respectively.

To generate the voltage for the coarse decision, the bottom plate of CM1 is connected to GND, the bottom plates of C0 to C7 of CDACU are connected to VDD, and the bottom plates of C0 to C7 of CDACL are connected to GND. If the parasitic capacitance at the CDAC output node is neglected, the CDAC output voltages ($\mathrm{VU_C}$ and $\mathrm{VL_C}$) can be expressed as

$$\mathrm{VU_C} = \mathrm{VCM} - \left(\frac{1}{2}\right) * (\mathrm{VI} - \mathrm{VDD}) \tag{1}$$

$$\mathrm{VL_C} = \mathrm{VCM} - \left(\frac{1}{2}\right) * \mathrm{VI} \tag{2}$$

$$\mathrm{VCM} = \left(\frac{3}{4}\right) * \mathrm{VDD}. \tag{3}$$

The dependence of the coarse-decision CDAC outputs on the input voltage (VI) is conceptually illustrated in Fig. 6(a).

During the fine-decision operation, both CDACU and CDACL use the thermometer-code output of latches (T1 to T7) on the basis of the coarse decision; the bottom plates of C1 to C7 are connected to either VDD (when Tk is H, $\mathrm{k} = 1, 2, \ldots, 7$) or to GND (when Tk is L). The bottom plate of C0 in CDACU is connected to VDD, and the bottom plate of C0 in CDACL is connected to GND. The resulting values of VU and VL become

$$\mathrm{VU_F} = \mathrm{VCM} - \left(\frac{1}{2}\right) * \left\{\mathrm{VI} - \frac{(\mathrm{p}+1)}{8} * \mathrm{VDD}\right\} \tag{4}$$

$$\mathrm{VL_F} = \mathrm{VCM} - \left(\frac{1}{2}\right) * \left(\mathrm{VI} - \frac{\mathrm{p}}{8} * \mathrm{VDD}\right) \tag{5}$$

where the index p specifies the sum of the thermometer-coded bits obtained in the coarse decision, i.e., p varies between 0 for

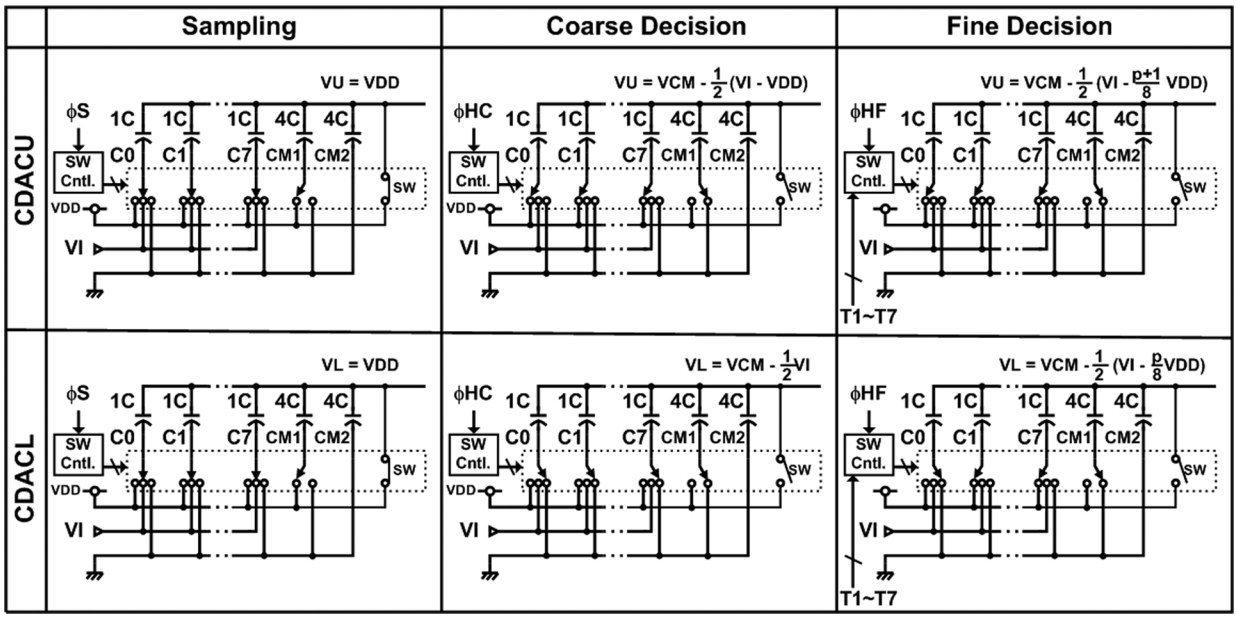

Fig. 5. Operational diagram of CDACs.

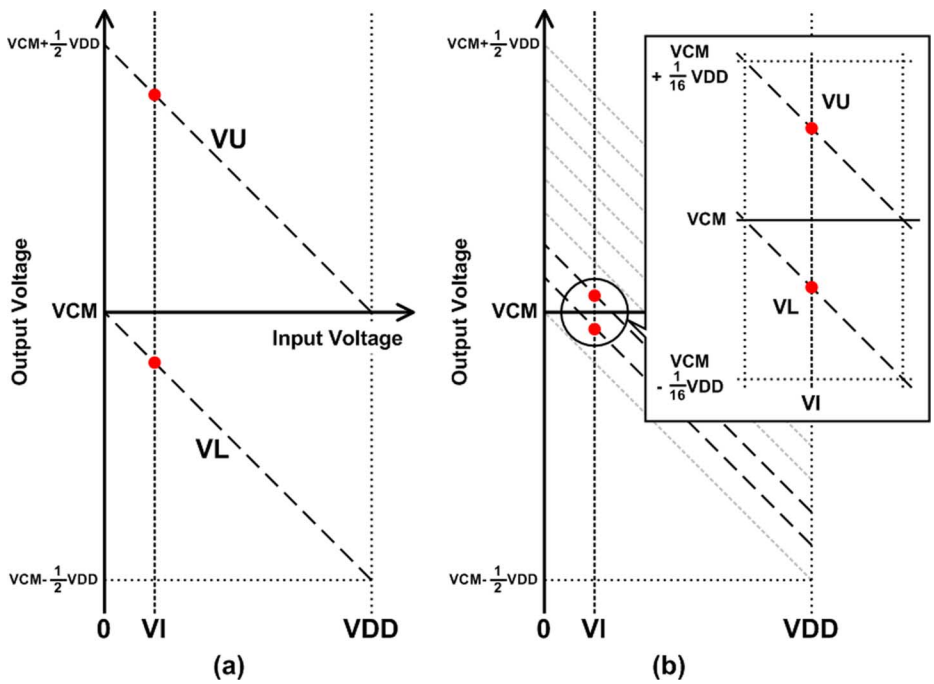

Fig. 6. Conceptual diagram of CDAC output (a) for coarse decision and (b) for fine decision.

the thermometer code 0000000 and 7 for 1111111. Thus, the difference between the CDAC's output voltages (i.e., VU − VL) for the fine decision is 1/8th ($= 1/2^3$) that for the coarse decision. Fig. 6(b) is a conceptual diagram of the outputs VU and VL of the CDAC versus input voltage VI for the fine decision. In our design, the CDACs do not generate an excessively high gate voltage that would cause reliability issues, because there is parasitic capacitance at their output nodes.

B. Interpolating Comparator

Seven active-interpolation comparators Q1 to Q7, each of which has two input pairs, receive the CDACs outputs VU and VL (Fig. 7). The input pair formed by transistors M1 and M3 receives $\mathrm{VU\_P}$ and $\mathrm{VU\_N}$, and the pair formed by M2 and M4 receives $\mathrm{VL\_P}$ and $\mathrm{VL\_N}$ (Fig. 8). The pairs pull currents from the source nodes of the cross-coupled inverters that perform the regeneration action. Transistors M1 and M3 are composed of m parallel-connected unit transistors, and M2 and M4 are composed of n parallel-connected unit transistors. For the comparator Qi ($\mathrm{i} = 1, 2, \ldots, 7$), the values of m and n are expressed as $\mathrm{m} = \mathrm{i}$ and $\mathrm{n} = 8 - \mathrm{i}$.

During the initial stage of the comparator activation, the input transistors operate in saturation because their drain nodes are at VDD. The amount of drain current ID through each unit

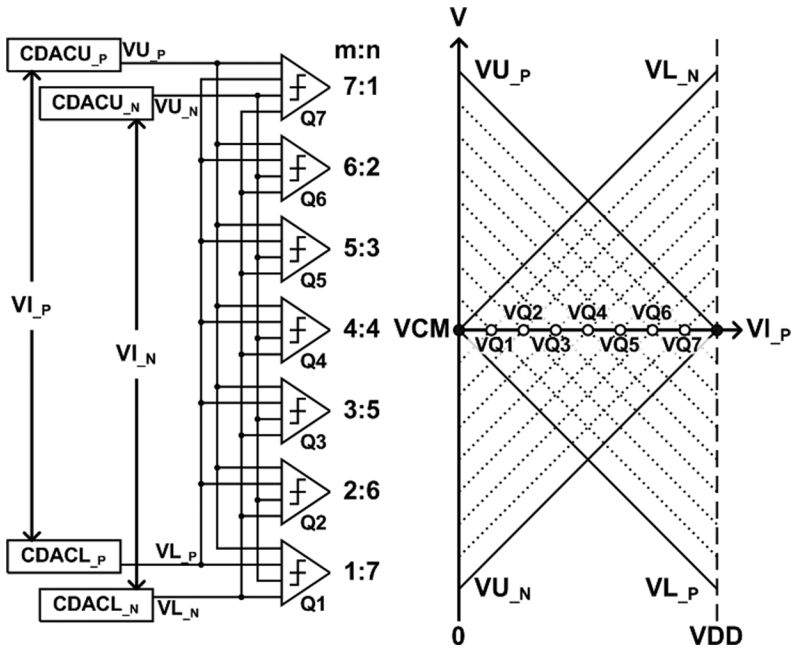

Fig. 7. Interpolation of signals with the proposed circuit.

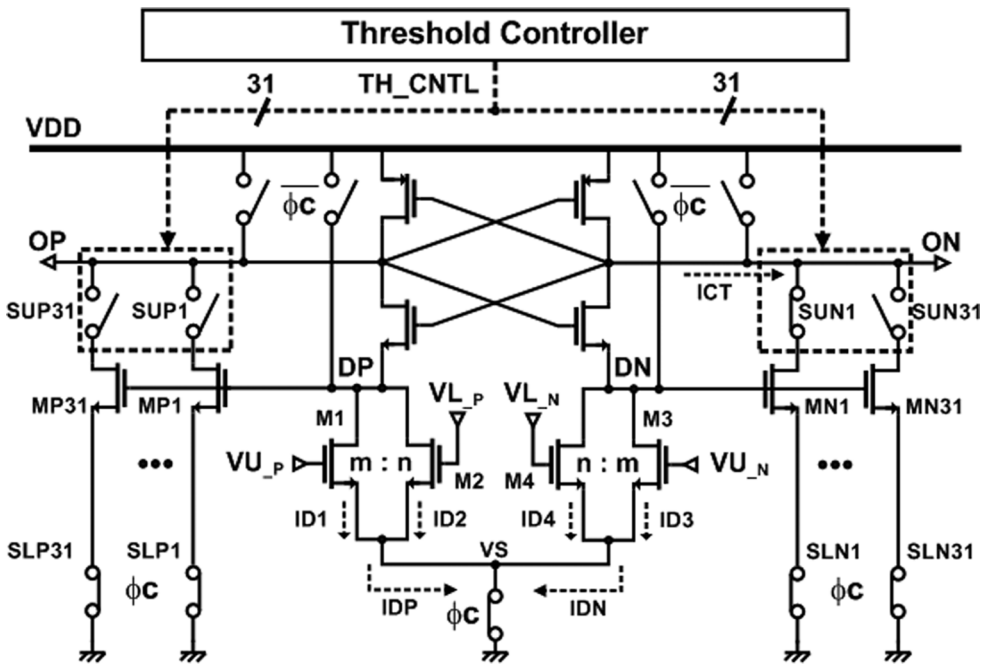

Fig. 8. Schematic diagram of comparator with circuits for controlling the threshold level.

transistor is approximately proportional to the difference between the gate source voltage and the MOS threshold voltage (VTH) in deep-submicron CMOS process technology [10]. In the 65-nm technology of our design, ID can be written as

$$\begin{aligned}\mathrm{ID} &= \gamma * \left(\frac{\mathrm{W}}{\mathrm{L}}\right) * (\mathrm{VG} - \mathrm{VS} - \mathrm{VTH}) \\ &= \gamma * \left(\frac{\mathrm{W}}{\mathrm{L}}\right) * \mathrm{VG} - \gamma * \left(\frac{\mathrm{W}}{\mathrm{L}}\right) * (\mathrm{VS} + \mathrm{VTH}) \quad (6)\end{aligned}$$

where γ is a process-dependent coefficient, W and L are the width and length of the unit transistor, VG the input voltage to the gate, and VS the source-node voltage. The finite source–drain resistance due to the short-channel effect is neglected in (6).

When there are no variations in the device size and characteristics, the difference between the currents pulled from the positive- and negative-source nodes of the cross-coupled inverter of the comparator Qi is expressed as

$$\Delta \mathrm{I} = \gamma * \left(\frac{\mathrm{W}}{\mathrm{L}}\right) (\mathrm{i} * \Delta \mathrm{VU} + (8 - \mathrm{i}) * \Delta \mathrm{VL}). \quad (7)$$

$$\Delta \mathrm{VU} = \mathrm{VU\_P} - \mathrm{VU\_N}, \text{ and } \Delta \mathrm{VL} = \mathrm{VL\_P} - \mathrm{VL\_N}. \quad (8)$$

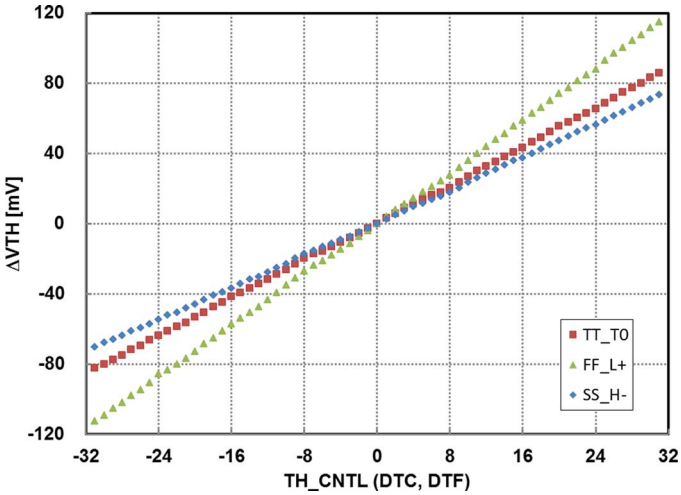

Fig. 9. Simulated controllable range of the comparator's threshold level vs. control code. TT_T0: Typically, T = 25 °C, VDD = 1.2 V, FF_L+: Fast, T = −40 °C, VDD = 1.3 V, SS_H−: Slow, T = 125°C, VDD = 1.1 V.

The comparator produces H or L at an equal probability (i.e., 50%/50%) when $\Delta I = 0$. Substituting (1)–(2) or (4)–(5) along with their negative-half-circuit counterparts into (7) produces the nominal threshold level of the comparator Qi ($i = 1, 2, \ldots, 7$) for the coarse (Fig. 7) and fine decisions as follows:

$$VQ_C(i) = \left(\frac{i}{8}\right) VDD$$
$$VQ_F(i) = \left\{\frac{(8-i)}{8}\right\} VQ_C(p) + \left(\frac{i}{8}\right) VQ_C(p+1). \quad (9)$$

The coarse-decision threshold voltages are evenly distributed between 0 to VDD from $i = 1$ to $i = 7$. The fine-decision threshold voltages are evenly distributed between $VQ_C(p)$ and $VQ_C(p+1)$ with the value of p determined by the coarse decision. This decision-threshold arrangement is consistent with proper operation of the proposed subranging ADC.

C. Comparator-Threshold-Level Adjustment

The proposed comparator has additional current-injection devices for controlling its threshold level (Fig. 8). The current-injection devices are composed of cascaded connections of upper switches SUPj or SUNj, NMOS transistors MPj or MNj, and lower switches SLPj or SLNj ($j = 1, 2, \ldots, 31$). A digital threshold controller controls the comparator threshold by switching SUPj or SUNj thereby adjusting the total current (ICT) that flows through the current-injection devices. Each comparator has 31 current-injection devices on each of the output nodes OP and ON. The digital code TH_CNTL controls the number of active current-injection devices. The simulated relationship between the comparator's threshold level and the control code are plotted for typical, slow, and fast conditions in Fig. 9. Here, ΔVTH is defined as the variation from the original threshold voltage. A negative code value means that the current-injection devices connected to OP are activated, and the plus value means the devices connected to ON are activated.

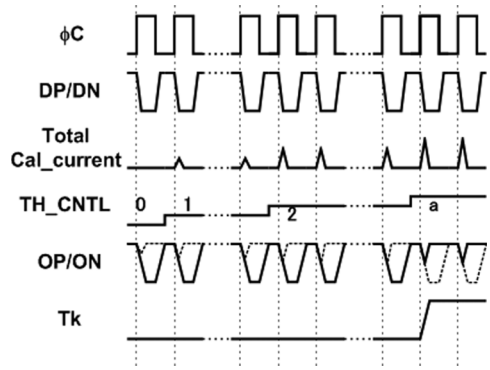

Fig. 10. Timing diagram for controlling the comparator's threshold level.

The threshold adjusting devices cause a power and speed penalty since they consume current and add an extra capacitive load to the comparator. To mitigate the extra current consumption, the gate of MPj (MNj) is connected to DP (DN), and SLPj and SLNj are controlled by clock ϕC (Figs. 8 and 10) so that a current ICT flows momentarily in the initial stage of the comparison. The power penalty due to the static current is reduced in comparison with that of [12], in which the comparator's threshold level is controlled by adding current paths that conduct static currents. In contrast to [13], in which the threshold level is adjusted by adding capacitors at the output nodes, the proposed approach suppresses the speed penalty by using current injection to increase the response speed.

D. Foreground Calibration

As a result of CMOS process variations, the comparators' threshold voltages, VQ_C and VQ_F, are likely different from the values given by (9). The deviation can be expressed as an offset current, IOFF, which is defined as the current that should be added to the comparator's regeneration node to force the comparator into a state that produces H or L with equal probability when the nominal threshold voltage is applied as an input voltage.

The offset current is the sum of two current components. One is the component caused by the difference between the currents through the differential input transistors when the input voltages are held at the nominal threshold voltage. The other component is an extra current, Iext, needed to compensate for asymmetry in regenerative latches including mismatches in parasitic capacitances of the regeneration nodes. This extra current does not depend on the input voltages.

Thus, from (6), the overall offset current can be written as

$$IOFF = \gamma * \left\{ m * \left(\frac{W_1}{L_1}\right) * VU\_P + n * \left(\frac{W_2}{L_2}\right) * VL\_P - m * \left(\frac{W_3}{L_3}\right) * VU\_N - n * \left(\frac{W_4}{L_4}\right) * VL\_N \right\} + I_0$$
$$I_0 = Iext - \gamma * \left\{ m * \left(\frac{W_1}{L_1}\right) * (VS + VTH_1) \right.$$

$$+ \mathrm{n} * \left(\frac{\mathrm{W}_2}{\mathrm{L}_2}\right) * (\mathrm{VS} + \mathrm{VTH}_2) - \mathrm{m} * \left(\frac{\mathrm{W}_3}{\mathrm{L}_3}\right) * (\mathrm{VS} + \mathrm{VTH}_3) - \mathrm{n} * \left(\frac{\mathrm{W}_4}{\mathrm{L}_4}\right) * (\mathrm{VS} + \mathrm{VTH}_4)\Bigg\} \tag{10}$$

where the subscript i in $(\mathrm{W_i}/\mathrm{L_i})$ corresponds to the values with regard to transistor Mi. The value of I_0 varies among the comparators but does not depend on the input voltages VU and VL; thus, it is common to each comparator for making the coarse and fine decisions.

There are two sets of VU and VL values (VUC, VLC) and (VUF, VLF) corresponding to two nominal threshold voltages, VQC for the coarse decision and VQF for the fine decision, and this results in there being two different offset currents, IOFFC and IOFFF. From (10), the equivalent offset current (IOFF_0) when the input voltages are all VCM as follows:

$$\mathrm{IOFF}_0 = \gamma * \left\{\mathrm{m} * \left(\frac{\mathrm{W}_1}{\mathrm{L}_1}\right) * \mathrm{VCM} + \mathrm{n} * \left(\frac{\mathrm{W}_2}{\mathrm{L}_2}\right) * \mathrm{VCM} - \mathrm{m} * \left(\frac{\mathrm{W}_3}{\mathrm{L}_3}\right) * \mathrm{VCM} - \mathrm{n} * \left(\frac{\mathrm{W}_4}{\mathrm{L}_4}\right) * \mathrm{VCM}\right\} + \mathrm{I}_0. \tag{11}$$

It follows from (10) and (11) that

$$\mathrm{IOFF_C} - \mathrm{IOFF}_0 = \gamma * \left\{\mathrm{m} * \left(\frac{\mathrm{W}_1}{\mathrm{L}_1}\right) * (\mathrm{VU_{C\_P}} - \mathrm{VCM}) + \mathrm{n} * \left(\frac{\mathrm{W}_2}{\mathrm{L}_2}\right) * (\mathrm{VL_{C\_P}} - \mathrm{VCM}) - \mathrm{m} * \left(\frac{\mathrm{W}_3}{\mathrm{L}_3}\right) * (\mathrm{VU_{C\_N}} - \mathrm{VCM}) - \mathrm{n} * \left(\frac{\mathrm{W}_4}{\mathrm{L}_4}\right) * (\mathrm{VL_{C\_N}} - \mathrm{VCM})\right\} \tag{12}$$

$$\mathrm{IOFF_F} - \mathrm{IOFF}_0 = \gamma * \left\{\mathrm{m} * \left(\frac{\mathrm{W}_1}{\mathrm{L}_1}\right) * (\mathrm{VU_{F\_P}} - \mathrm{VCM}) + \mathrm{n} * \left(\frac{\mathrm{W}_2}{\mathrm{L}_2}\right) * (\mathrm{VL_{F\_P}} - \mathrm{VCM}) - \mathrm{m} * \left(\frac{\mathrm{W}_3}{\mathrm{L}_3}\right) * (\mathrm{VU_{F\_N}} - \mathrm{VCM}) - \mathrm{n} * \left(\frac{\mathrm{W}_4}{\mathrm{L}_4}\right) * (\mathrm{VL_{F\_N}} - \mathrm{VCM})\right\}. \tag{13}$$

Conversion range of the fine decision is 1/8th (i.e., $= 1/2^3$) of the coarse decision for the proposed 3-bit-coarse and 3-bit-fine subranging configuration. Thus, fine-voltage terms like $\mathrm{VU_{F\_P}} - \mathrm{VCM}$, measured when the input voltage equals the ideal threshold of a comparator during the fine decision, will be 1/8th of the corresponding coarse-voltage terms like $\mathrm{VU_{C\_P}} - \mathrm{VCM}$, obtained when the input voltage is adjusted to place the same comparator at the threshold during the coarse decision. Therefore, $\mathrm{IOFF_F} - \mathrm{IOFF}_0$ is given by

$$\mathrm{IOFF_F} - \mathrm{IOFF}_0 = \frac{(\mathrm{IOFF_C} - \mathrm{IOFF}_0)}{8}. \tag{14}$$

From (14), the offset current for the fine decision ($\mathrm{IOFF_F}$) becomes

$$\mathrm{IOFF_F} = \frac{(\mathrm{IOFF_C} - \mathrm{IOFF}_0)}{8} + \mathrm{IOFF}_0. \tag{15}$$

Note that the generation of $\mathrm{VU_F}$ and $\mathrm{VL_F}$ for the fine calibration requires the use of either intermediate reference voltages combined with the existing CDACs or higher resolution CDACs, both of which would increase the circuit complexity and area. Instead of using these means, the fine-decision control code is obtained by a digital calculation based on (15).

The flow chart of the calibration is shown in Fig. 11. First, the calibration for the coarse decision is performed. The voltages $\mathrm{VU_C}$ and $\mathrm{VL_C}$ that correspond to the nominal coarse-decision threshold voltages are generated by the CDACs by connecting the bottom plates of C0 to $\mathrm{Ck} - 1$ to VDD and Ck to C7 to VSS during sampling period for the positive-half CDACs (Fig. 11). (For the negative-half CDACs, connection to VDD and VSS are swapped.) The resulting voltages are output to all comparators. During the coarse calibration, comparator Qk continuously makes decisions and outputs Tk while the control code (TH_CNTL) is swept so that the value of ICT increases from the minimum to the maximum (Fig. 10). The threshold controller searches for the threshold control code (TH_CNTL) that makes the probabilities of the comparator producing H and L equal. The resulting value of TH_CNTL is stored in the register as the control code for the coarse decision (DTCk) for comparator Qk.

To perform the calibration for the fine decision, CDACs are set so that all comparators' input voltages become a common mode voltage VCM, and the threshold controller searches for the control code DT0k that forces the comparator Qk to produce H and L with equal probability (Fig. 11). VCM is generated by connecting the bottom plates of C0 to C7 to VDD in CDACU and C0 to C7 to VSS in CDACL during the sampling period. Since the comparator's threshold voltage linearly depends on the control code, as shown in Fig. 9, the control code for the fine decision (DTFk) can be obtained from (15) as

$$\mathrm{DTFk} = \frac{(\mathrm{DTCk} - \mathrm{DT0k})}{8} + \mathrm{DT0k} \quad (\mathrm{k} = 1, 2, \ldots, 7). \tag{16}$$

All calibration circuits are implemented on-chip, and no off-chip manual adjustment is needed. Since the calibration is done in the foreground, it cannot compensate for the variations due to VDD and temperature changes that happen afterward. Circuit simulations showed that 15% a decrease in VDD from the maximum value (1.3 V) causes the SNDR to deteriorate by 2 dB, and the temperature variation from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ causes the SNDR to change by less than 1 dB. A recalibration is needed when a better accuracy is needed.

In the ENOB-degradation estimation, we calculate the maximum value of the uncompensated offset error when the VDD or temperature value experiences the maximum possible excursion after the foreground calibration. Then the error is translated into the ENOB degradation assuming that the offset causes an additional decision error uniformly distributed with the peak-to-peak value equal to the maximum offset error. Note that these

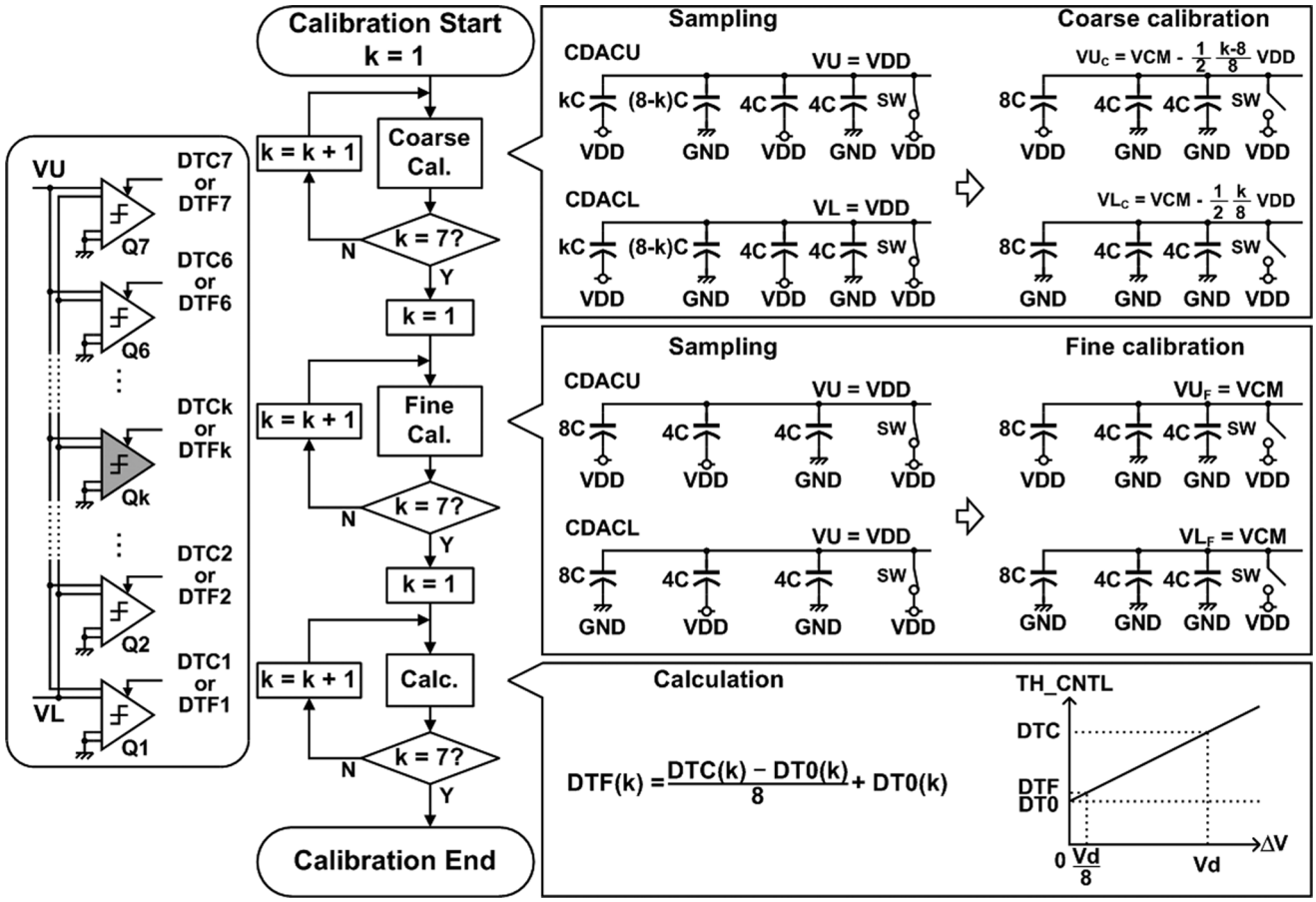

Fig. 11. Flow chart for the foreground calibration.

degradations will be recovered if a calibration is remade after the supply voltage and/or temperature changed.

IV. Measurement Results

The proposed ADC was fabricated in 65-nm 1P7M CMOS technology with MIM capacitors. A photograph of the chip is shown in Fig. 12. The active area (including the on-chip calibration circuit) is 0.044 mm^2.

The measured DNL and INL (with and without calibration) are shown in Fig. 13. Before calibration, the DNL and INL each reach 3 LSB. After calibration they are reduced to 0.8 LSB. The measured spectrum after calibration is shown in Fig. 14. Here, the sampling frequency is 1 GS/s and the frequency of the input signal is 501 MHz. The SNDR is 32.8 dB, resulting in 5.16 ENOB at the Nyquist frequency. Here, the output data is decimated by a factor of eight due to limitations in the measurement instruments. SNDR and SFDR are plotted against input frequency in Fig. 15. SNDR stays above 32.8 dB up to the Nyquist frequency. Table I summarizes the performance of the proposed ADC. The power consumption of the whole circuit (including calibration) is 9.9 mW, and FoM is 278 fJ/conv.-step at a 1.1-V supply voltage. The clock drivers account for 40% of the total power, the comparators 22%, the threshold-level controller 32%, and the CDACs 6%.

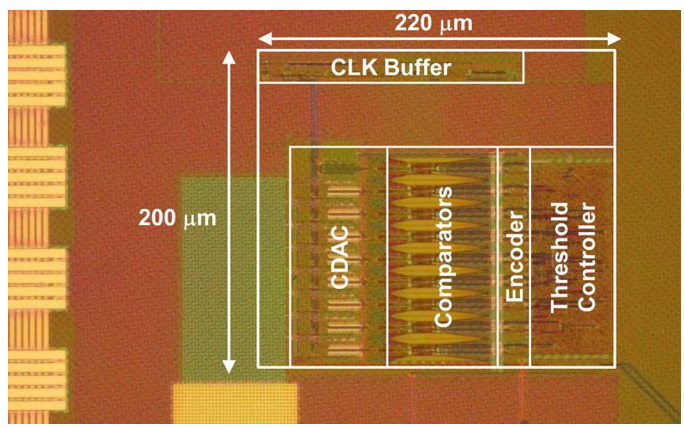

Fig. 12. Chip micrograph.

To confirm the effect of the use of coarse and fine calibration, we observe the control codes, i.e., DTCk for the coarse decision, DT0k achieved when the comparator inputs are held at VCM, and resulting DTFk for the fine decision. For a chip operating off a 1.2 V supply, the DTCk values were +6, +7, 0, 3, −4, +6, and 0 for k = 1 through 7, and the DTFk values +8, +9, −1, +1, −4, +3, and −4. When we applied the codes DT0k for both the coarse and fine decisions, the measured ENOB was 4.67. When we used the DTCk for the coarse

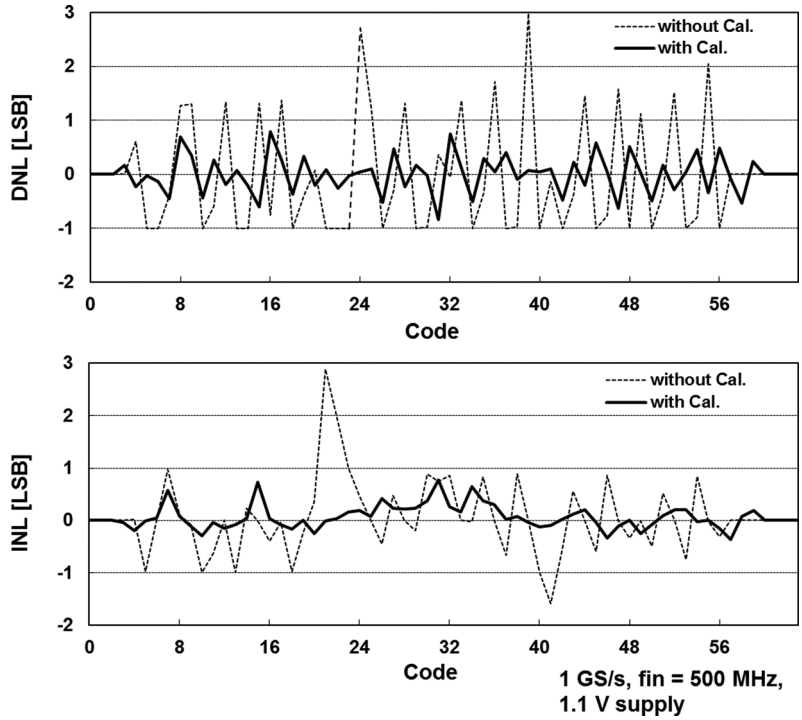

Fig. 13. Measured DNL and INL.

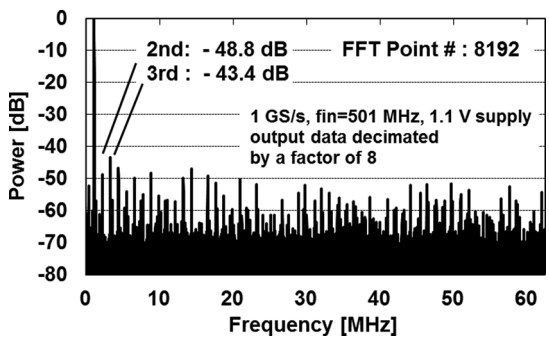

Fig. 14. Measured spectrum.

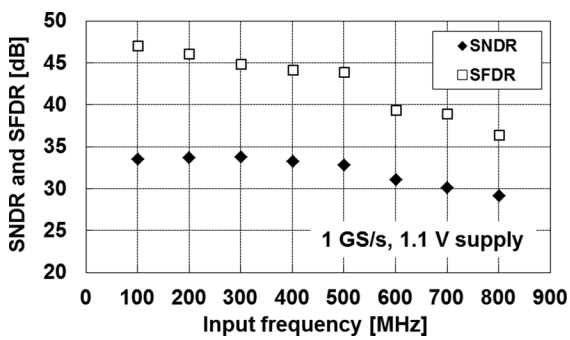

Fig. 15. SNDR and SFDR vs. input frequency.

decision and DT0k for the fine decision, the ENOB was 5.20. Using the complete set of the control codes, i.e., DTCk for the coarse decision and DTFk for the fine decision resulted in ENOB of 5.41.

TABLE I
SUMMARY OF ADC PERFORMANCE

	Ref. [9]	Ref. [10]	This work
Resolution [bit]	8	6	6
SNDR (Nyquist) [dB]	41.3	34.0	32.8
Conversion rate [GS/s]	0.77	0.7	1.0
Supply voltage [V]	1.2	1.2	1.1
Power consumption [mW]	70	7	9.9
Active area [mm^2]	0.605	0.130	0.044
FoM [fJ/conv.-step]	940	250	278
Process [nm]	90	90	65
Architecture	subr.	subr.	subr.

V. CONCLUDING REMARKS

An improved subranging architecture was proposed to deal with issues caused by the settling time of the reference voltages and switches connected to intermediate potential nodes in subranging ADCs. In this ADC architecture, the reference-voltage generator and its accompanying switches are eliminated by the use of CDACs and the comparators' threshold level is digitally controlled by means of active interpolation. In addition, to reduce the area of the ADC and sampling error, the same set of comparators (there are no redundant comparators) is used for

the coarse and fine decisions. To realize this architecture, different threshold-control codes for the coarse and fine decisions are supplied to each comparator. A digitally assisted control circuit obtains the threshold-control code for the coarse decision by generating an nominal voltage with the CDACs. The code for the fine decision is obtained by digital calculation using the coarse code rather than by using a high-resolution DAC, and all the calibrations are done on-chip.

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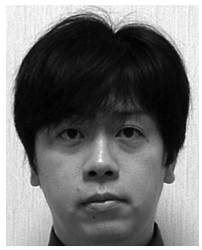

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