A New Bridgeless PFC Sepic and Cuk Rectifiers with Low Conduction and Switching Losses

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***Abstract* – New bridgeless single phase ac-dc power factor correction (PFC) rectifiers based on Sepic and Cuk topologies are proposed. The absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each switching cycle results in less conduction losses and improved thermal management compared to the conventional Sepic and Cuk PFC converters. The proposed topologies are designed to work in discontinuous conduction mode (DCM) to achieve almost unity power factor in a simple and effective manner. The DCM operation gives additional advantages such as: zero-current turn-on in the power switches, zero-current turn-off in the output diode, and reduces the complexity of the control circuitry. The proposed rectifiers are investigated theoretically. Performance comparisons between the proposed and conventional Sepic PFC rectifiers are performed. Simulation and experimental results are provided for a design example of a 65W/48V at 100 V_{rms} line voltage to evaluate the performance of the proposed PFC rectifier.**

***Keywords* – Bridgeless rectifier, Cuk converter, power factor correction (PFC), rectifier, Sepic converter, total harmonic distortion (THD).**

I. INTRODUCTION

The preferable type of power factor correction (PFC) circuit is the active PFC since it makes the load behave like a pure resistor, leading to near unity load power factor and generating negligible harmonics in the input line current. Most active PFC circuits as well as switched mode power supplies (SMPS) on the market today comprise a front-end bridge rectifier followed by a high frequency dc-dc converter. Fig. 1 shows an example of a conventional PFC Sepic and Cuk rectifiers. Referring to Fig.1, it is clear that the current path flows through two rectifier bridge diodes and the power switch (Q) during the switch on-time, and two rectifier bridge diodes and the output diode (D_o) during the switch off state. Thus, during each switching cycle the current flows through three power semiconductor switches. This approach is suitable for a low power range. In the low line input and high power applications, the high conduction loss caused by the high forward voltage drop of the bridge diode begins to degrade the overall system efficiency, and the heat generated within the bridge rectifier may destroy the individual diodes. Hence, it becomes necessary to utilize a bridge rectifier with higher current handling capability or heat dissipating characteristics. This increases the size and cost of the power supply, which is unacceptable for an efficient design.

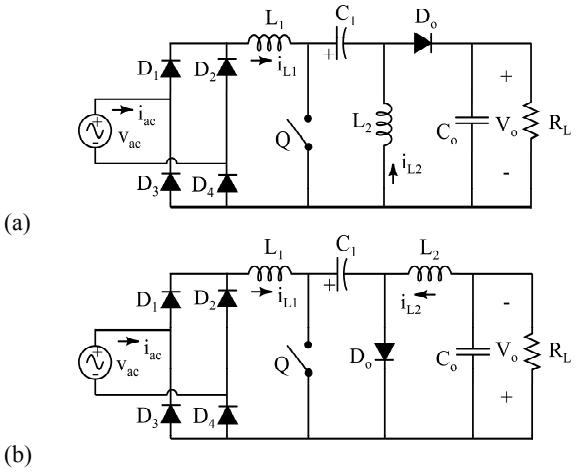

Fig. 1. Conventional PFC rectifiers: (a) Sepic topology. (b) Cuk topology.

In an effort to maximize the power supply efficiency, considerable research efforts have been directed towards the development of efficient bridgeless PFC circuit topologies [1]-[18]. A bridgeless PFC circuit allows the current to flow through a minimum number of switching devices compared to the conventional PFC circuit. Accordingly, the converter conduction losses can be significantly reduced and high efficiency can be obtained as well as cost savings.

Most of the presented bridgeless topologies so far implement a boost-type circuit configuration (also referred to as dual boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. These features have led power supply companies to start looking for bridgeless PFC circuit topologies. In [19], a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. On the other hand, the bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter.

In order to overcome the drawbacks of bridgeless PFC boost rectifier, two bridgeless topologies which are suitable for step-up/step-down applications are introduced in [20], [21]. However, the proposed topology in [20] still suffers from having three semiconductors in the current conduction path during each switching stage and it requires an isolated gate-drive. On the other hand, the bridgeless topology

presented in [21] has several advantages such as the presence of one or two semiconductors in the current conduction path and reduced voltage stress across the semiconductor devices; however, it also requires an isolated gate-drive.

II. The Proposed Bridgeless Rectifiers

This paper proposes bridgeless PFC circuits based on Sepic and Cuk topologies with low conduction losses, as shown in Figs. 2(a) and 2(b), respectively. Unlike the boost converter, the Sepic and Cuk converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple, and less electromagnetic interference (EMI) associated with the DCM topology [22]. Similar to the bridgeless boost presented in [5] and [8], the proposed topologies in Fig. 2 are formed by connecting two dc-dc Sepic or Cuk converters, one for each half-line period of the input voltage. The operational circuits during positive and negative half-line period for the proposed bridgeless Sepic rectifier of Fig. 2(a) are shown in Figs. 3(a) and 3(b), respectively.

Note that, by referring to Fig. 3, there are one or two semiconductor(s) in the current flowing path; hence, the conduction losses as well as the thermal stresses on the semiconductor devices are further reduced, and the circuit efficiency is improved compared to the conventional Sepic rectifier. Moreover, Fig. 3 shows that the input ac line voltage is always connected to the output ground through the slow-recovery diodes D_p and D_n. Thus, the proposed topologies do not suffer from the high common-mode EMI noise emission problem and has common-mode EMI performance similar to the conventional topologies of Fig. 1. Consequently, the proposed topologies appear to be promising candidates for commercial PFC products.

Each of the proposed rectifiers utilizes two power switches (Q_1 and Q_2), two low-recovery diodes (D_p and D_n), and a fast diode (D_o). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies in Fig. 1, which are often described as a disadvantage in terms of size and cost. However, a better thermal performance can be achieved with the two inductors compared to a single inductor. On the other hand, as shown in Fig. 2(c), the three inductors in the proposed topologies can be coupled on the same magnetic core allowing considerable size and cost reduction. Additionally, the 'near zero-ripple-current' condition at the input port of the rectifier can be achieved without compromising performance. This condition is very desirable especially for the DCM operation, because the generated EMI noise is minimized, reducing input filtering requirements dramatically. Furthermore, both the conventional Sepic/Cuk PFC rectifiers of Fig. 1 and the proposed rectifiers of Fig. 2 have the same count of total components when coupled inductor technique is implemented. Another advantage of the proposed rectifier is a reduction in the power switch current stress as compared to the conventional Sepic/Cuk PFC rectifiers. This is because each power switch is operating during half line period. On the other hand, components' voltage stresses are equal to their counterparts in the conventional Sepic converter.

The remainder of this study is organized as follows: Principle of operation is presented in sections III. Detailed analysis, modeling, and comparisons are presented in section IV. Analysis of the proposed rectifier with coupled-inductor structure is also presented in section IV. Simulation and experimental results are given in section V, followed by conclusions in Section VI.

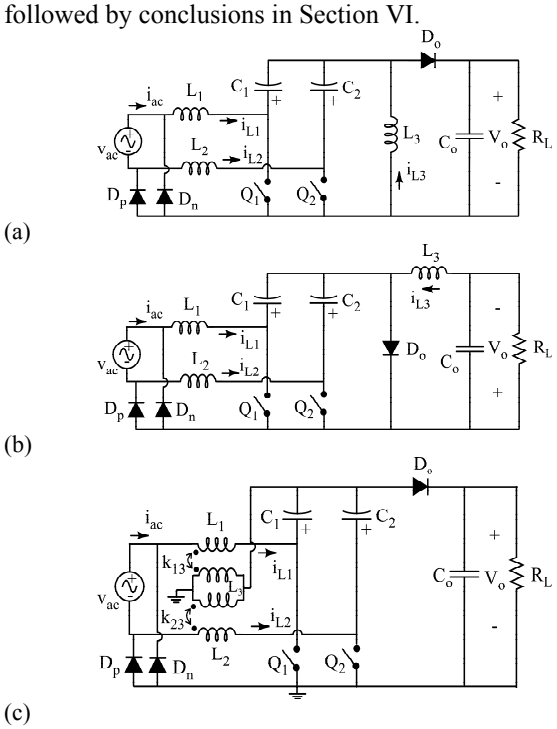

Fig. 2. Proposed bridgeless rectifiers. (a) Sepic derived. (b) Cuk derived. (c) Sepic with coupled inductors derived.

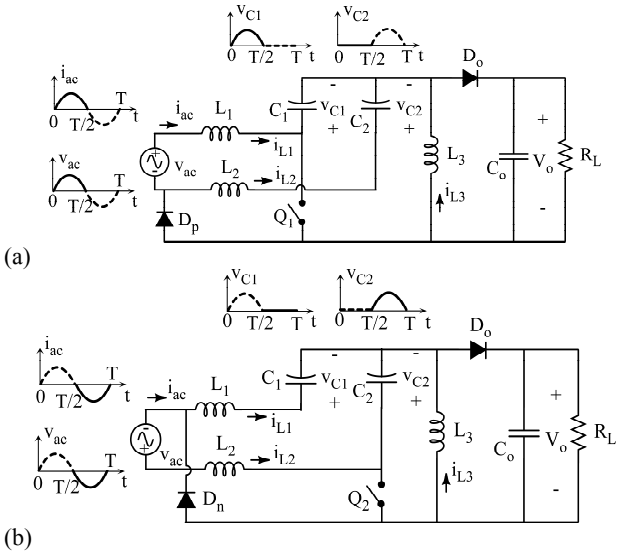

Fig. 3. Equivalent circuits for the rectifier of Fig. 2(a): (a) During positive half-line period, and (b) During negative half-line period of the input voltage.

III. Principle Of Operation Of The Proposed Bridgeless Rectifiers

The proposed bridgeless rectifiers shown in Fig. 2 are constructed by connecting two dc-dc converters. Referring to Fig. 2, during the positive half-line cycle, the first dc-dc Sepic (or Cuk) circuit, L_1-Q_1-C_1-L_3-D_o, is active through diode D_p, which connects the input ac source to the output ground. During the negative half-line cycle, the second dc-dc Sepic (or Cuk) circuit, L_2-Q_2-C_2-L_3-D_o, is active through diode D_n, which connects the input ac source to the output ground. Thus, due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half-period of the input voltage. Moreover, the operation of the proposed rectifiers of Fig. 2 will be described assuming that the three inductors are operating in DCM. By operating the rectifier in DCM, several advantages can be gained. These advantages include: natural near-unity power factor, the power switches are turned-on at zero current, and the output diode D_o is turned-off at zero current. Thus, the loss due to the turn-on switching losses and the reverse recovery of the output diode are considerably reduced. Furthermore, the circuit operations for the Sepic and Cuk rectifiers of Fig. 2(a) and (b), respectively, are identical. Therefore, due to the space limit, only the bridgeless Sepic rectifier of Fig. 2(a) will be analyzed, but a similar development can be made for the bridgeless Cuk rectifier of Fig. 2(b). Equations for both rectifiers are identical, provided that the voltages on the capacitors for the Sepic rectifier are,

$$v_{C1}(t)=\begin{cases} v_{ac}(t) & 0\le t\le \dfrac{T}{2} \\ 0 & \dfrac{T}{2}\le t\le T \end{cases} \tag{1}$$

And for the Cuk rectifier,

$$v_{C1}(t)=\begin{cases} v_{ac}(t)+V_o & 0\le t\le \dfrac{T}{2} \\ V_o & \dfrac{T}{2}\le t\le T \end{cases} \tag{2}$$

where T represents the period of the line voltage. Similar to the conventional Sepic and Cuk converters, the DCM for the proposed rectifier occurs when the current through diode D_o drops to zero before the end of the switch off-time. Thus, the circuit operation during one switching period Ts in a positive half-line period can be divided into three distinct operating modes as shown in Fig. 4(a-c), and it can be described as follows:

Stage 1 [t_0, t_1]*, Fig. 4(a):* when the switch Q_1 is turned-on, diode D_p is forward biased by the sum inductor currents i_{L1} and i_{L2}. As a result, diode D_n is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage (v_{ac} + V_o). In this stage, the three-inductor currents increase linearly at a rate proportional to the input voltage v_{ac}. The rate of increase of the three inductor currents are given by

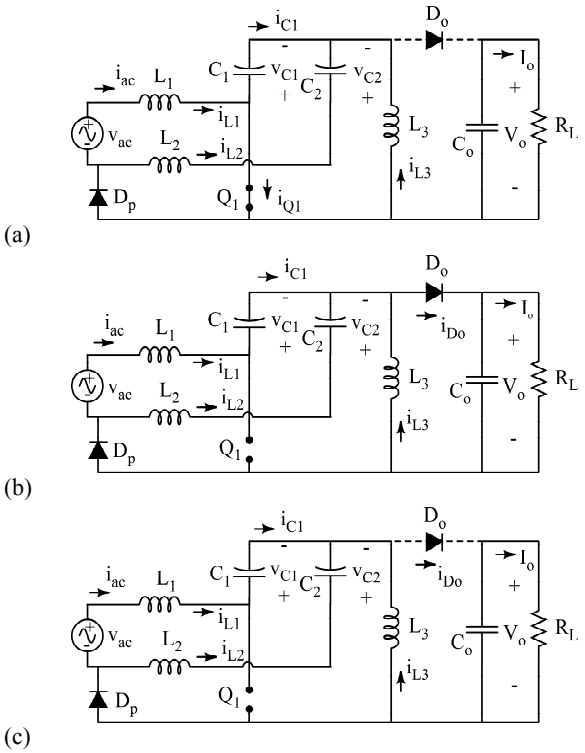

Fig. 4. Topological stages for the bridgeless Sepic rectifier of Fig. 3(a) during switching cycle T_s: (a) Switch ON topology. (b) Switch OFF topology. (c) DCM topology. Solid and dashed lines represent active and inactive elements, respectively.

$$\frac{di_{Ln}}{dt}=\frac{v_{ac}}{L_n},\ n=1,\ 2,\ 3 \tag{3}$$

During this stage, the switch current is equal to the sum of the three inductors' currents. Thus, the peak switch current, $I_{Q1\text{-}pk}$, is given by

$$I_{Q1,pk}=\frac{V_m}{L_e}D_1\,T_s \tag{4}$$

where,

$$\frac{1}{L_e}=\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3} \tag{5}$$

and D_1 is the switch Q_1 duty-cycle. This interval ends when Q_1 is turned-off, initiating the next subinterval.

Stage 2 [t_1, t_2]*, Fig. 4(b):* At the instant t_1, switch Q_1 is turned-off, diode D_o is turned-on simultaneously providing a path for the three inductor currents. Diode D_p remains conducting to provide a path for i_{L1} and i_{L2}. In this stage, the three inductor currents decrease linearly at a rate proportional to the output voltage, V_o. The three inductors' currents are given by

$$\frac{di_{Ln}}{dt}=\frac{-V_o}{L_n},\ n=1,\ 2,\ 3 \tag{6}$$

This interval ends when the output diode current, i_{Do}, reaches smoothly to zero and D_o becomes reverse-biased. The normalized length of this interval is given by

$$D_2=\frac{D_1}{M}\sin(\omega t) \tag{7}$$

where $M = V_o/V_m$ is the voltage conversion ratio.

Stage 3 [t_2, T_s], *Fig. 4(c):* In this stage, both Q_1 and D_o are in their off-state. Diode D_p provides a path for i_{L3}. The three inductors behave as current sources, which keep the currents constant. Hence, the voltage across the three inductors is zero. Capacitor C_1 is charging up by i_{L1}, while C_2 is discharged by i_{L2}.

Fig. 5 shows the main theoretical waveforms during one switching period T_s. It should be mentioned here that if the two active switches Q_1 and Q_2 are implemented as standard MOSFET, then the body diode of Q_2 will conduct during the first stage and the circuit will not function properly. In other words, there are reverse voltages applied to the active switches, so that the switches must have reverse blocking capability. Therefore, unidirectional current conducting device must be implemented for Q_1 and Q_2. In this case, turning ON or OFF Q_2 during the first stage will not change the circuit operation mode. Accordingly, both of the switches, Q_1 and Q_2, can be driven by the same control signal, which helps in reducing the cost and complexity of the driving circuit.

IV. Analysis And Comparison

A. Voltage Conversion Ratio, M

The voltage conversion ratio $M = V_o/V_m$ in terms of circuit parameters can be found by evaluating the average output diode current, I_{Do}, during one line-cycle of the ac input voltage i.e.

$$I_{Do} = \frac{1}{T}\int_0^T \bar{i}_{Do}\, dt \tag{8}$$

where the symbol "¯" denotes the average value during one switching period T_s. From Fig. 5, the average output diode current over one switching period is given by

$$\bar{i}_{Do} = \frac{D_1^2\, T_s\, v_{ac}^2}{2\, L_e\, v_o} \tag{9}$$

Substituting (9) in (8), and evaluating (8) gives

$$I_{Do} = \frac{V_m^2}{2\, R_e V_o} \tag{10}$$

where R_e is the emulated input resistance of the converter and equals,

$$R_e = \frac{2\, L_e}{D_1^2\, T_s} \tag{11}$$

On the other hand, the average output diode current during one line-cycle is equal to the average current through the load R_L, I_o. Thus, one can simply show that the desired voltage conversion ratio M is equal to:

$$M = \sqrt{\frac{R_L}{2\, R_e}} = \frac{D_1}{\sqrt{2\, K_e}} \tag{12}$$

where the dimensionless parameter K_e is defined as

$$K_e = \frac{2\, L_e}{R_L\, T_s} \tag{13}$$

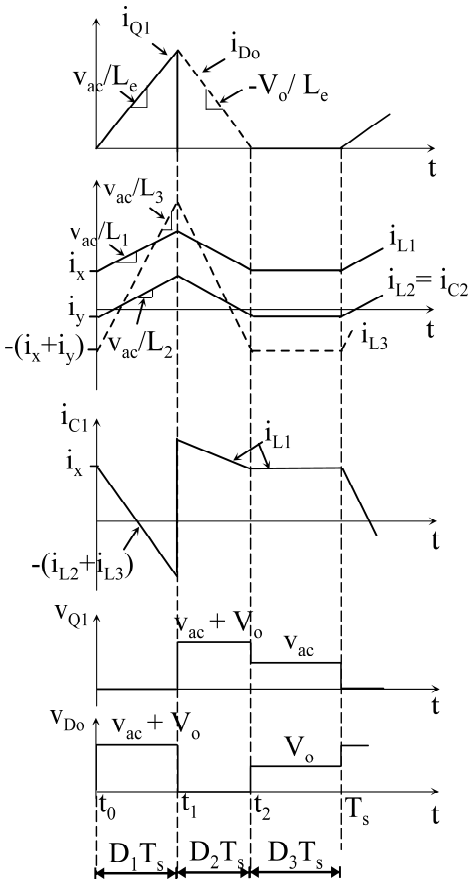

Fig. 5. Theoretical DCM waveforms during one switching period T_s for the converter of Fig. 3(a).

The voltage conversion ratio M in (12) is the same expression obtained for conventional PFC Sepic rectifier in DCM [22], except for the definition of L_e.

B. Input Line Current

Assuming that the efficiency is close to unity, the averaged input current over one switching period can be obtained from the instantaneous power balancing between the input and output ports of the rectifier; thus,

$$v_{ac} \cdot \bar{i}_{ac} = v_o \cdot \bar{i}_{Do} \tag{14}$$

where $\bar{i}_{ac}$ represents the input line current averaged during one switching cycle. Substituting (9) in (14) we obtain,

$$\bar{i}_{ac} = \frac{v_{ac}}{R_e} \tag{15}$$

Similar to the conventional Sepic PFC rectifier, (15) shows that the input port of the proposed rectifier obeys Ohm's law so that the input current is sinusoidal and in phase with the input voltage.

C. Boundaries between CCM and DCM

Referring to the output diode D_o current waveform in Fig. 5, the DCM operation mode requires that the sum of the duty-cycle and the normalized switch off-time length to be less than one, i.e.

$$D_2 < 1 - D_1 \tag{16}$$

Substituting (7) into (16) and using (12), the following condition for DCM is obtained,

$$K_e < K_{e-crit} = \frac{1}{2\left(M+1\right)^2} \tag{17}$$

For values of $K_e > K_{e\text{-}crit}$, the converter operates in CCM; otherwise, the converter operates in DCM.

D. The Proposed Bridgeless PFC Rectifiers with Coupled Inductors

In the proposed circuit of Fig. 2(a) and (b), the three inductors have identical voltage waveforms; hence, they can be magnetically coupled into a single magnetic core. Fig. 2(c) shows the proposed bridgeless Sepic with coupled inductors. The topological stages for the coupled inductors circuit of Fig. 2(c) are similar to the three topological stages of the uncoupled case. Referring to Fig. 2(c), the inductors L_1 and L_3 are magnetically coupled together with a coupling coefficient k_{13}, whereas L_2 and L_3 are magnetically coupled together with a coupling coefficient k_{23}. Note that, there is no magnetic coupling between L_1 and L_2. Moreover, by proper coupling between the three windings, it is possible to obtain an input current having very low high-frequency content (near zero current ripples). On the other hand, it is preferred that inductors L_1 and L_2 have equal values so that they carry the same ripple current. Accordingly, when L_1=L_2=L, then k_{13}=k_{23}=k, and the near zero current ripples in the input line current can be demonstrated by writing the characteristic equations of the coupled inductors during switch on-time which is given by,

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix} = \frac{1}{\Delta}\begin{bmatrix} L\,L_3 - L_M^2 & L_M^2 & -L\,L_M \\ L_M^2 & L\,L_3 - L_M^2 & -L\,L_M \\ -L\,L_M & -L\,L_M & L^2 \end{bmatrix}\begin{bmatrix} v_{ac} \\ v_{C1} - v_{C2} \\ v_{C1} \end{bmatrix} \tag{18}$$

where

$$\Delta = L^2\,L_3 - 2L\,L_M^2 > 0 \tag{19}$$

$$L_M = k\sqrt{L\,L_3} \qquad (0 < k < 1) \tag{20}$$

where L_M is the mutual inductance. Note that (19) must be positive since the total inductance matrix is symmetric positive definite, i.e. it has a positive determinant. At a steady state, $v_{C1} = v_{ac}$, and $v_{C2} = 0$, then from (18) the following condition must be satisfied for zero current ripples in the input current,

$$\frac{di_{L1}}{dt} = 0 \Rightarrow \quad L_M = L_3 \;\Rightarrow\; k = \sqrt{\frac{L_3}{L}} \tag{21}$$

During switch off-time, one can show that the condition for zero current ripples in the input current is similar to (21). It should be mentioned here that the steady-state analysis presented in Sec. III and IV, for the three separate inductors, is also valid for the coupled inductors extension, except for the definition of the effective inductance L_e (5). This is because the switching current ripple is only determined by the output inductor L_3. Thus, for the coupled inductors case, the definition of L_e becomes $L_e = L_3$.

E. Comparison between Conventional and Bridgeless Sepic PFC Rectifier

The circuit components in both the conventional PFC Sepic rectifier (shown in Fig. 1(a)) and the proposed bridgeless PFC Sepic have similar peak voltage and current stresses. However, the bridgeless Sepic subjects the input inductors (L_1 and L_2), the coupling capacitors (C_1 and C_2), and the active switches (Q_1 and Q_2) to a lower rms current stress compared to their counterparts in the conventional Sepic topology. Moreover, since the bridgeless Sepic is constructed by connecting two dc-dc converters each operating as Sepic dc-dc converter, switching performance of the two converters remains the same, which results in similar switching losses. In contrast, as shown in Table I, the input current in the bridgeless Sepic flows through fewer power semiconductor devices compared to the conventional Sepic PFC. Thus, efficiency improvement by using bridgeless Sepic relies mainly on the conduction loss difference between the two topologies.

An efficiency comparison between the conventional and the bridgeless PFC Sepic rectifiers is performed based on simulation results. In this comparison, both the conventional and the bridgeless PFC Sepic rectifiers are assumed to operate in DCM with the same operating conditions and parameters. The simulated efficiency presented in Fig. 6, includes conduction and switching losses of the semiconductor devices, inductors' copper losses, as well as capacitors ESR losses. Furthermore, Pspice actual semiconductor models have been used to simulate the semiconductor devices: STTH2003CR (300 V, 10 A, V_F = 0.85 V) high efficiency ultrafast diode for the output Sepic diode, and 1N5402 (200 V, 3 A, V_F = 1 V) standard recovery rectifier for the slow diodes. Three different MOSFETs (IRFB4332PBF with $R_{DS\text{-}ON}$ = 29 mΩ, STY60NM50 with $R_{DS\text{-}ON}$ = 45 mΩ, and IRF450 with $R_{DS\text{-}ON}$ = 400 mΩ) as well as an IGBT (HGTG40N60A4 with $V_{CE\text{-}Sat}$ = 1.7 V @ 40 A) actual models have been used for the active switches. Furthermore, for the bridgeless Sepic PFC rectifier, a low voltage drop with very low reverse leakage current Schottky barrier diode (type PDS3200 with V_F = 0.63 V @ 1 A) is connected in series with the power MOSFET to prevent any current from flowing through the MOSFET body-diode. On the contrary, an ideal diode is connected in series with the IGBT to resemble the reverse blocking IGBT (RB-IGBT) device. It is worth mentioning here that using the newly available RB-IGBT instead of using conventional IGBT with series connected diode, presents very low on-state characteristics, which lead to low conduction losses in a converter that requires reverse blocking voltage switches.

It is evident from Fig. 6 that the employment of a low $R_{DS\text{-}ON}$ power MOSFET improves the efficiency in both the conventional and the bridgeless PFC Sepic topologies. However, for all the different types of switches, Fig. 6 shows that the efficiency of the bridgeless PFC Sepic rectifier is higher than that of the conventional PFC Sepic rectifier for an output power level above 50-W. Fig. 6 also shows that efficiency improvement is more pronounced when an IGBT is utilized as the switching device.

V. Simulation And Experimental Results

To verify the feasibility of the proposed bridgeless PFC rectifiers, simulation and experimental results for the bridgeless Sepic of Fig. 2(a) are presented. The rectifier is designed for the following power stage specifications:

- Input voltage, v_{ac} = 100 V_{rms} @ 50 Hz
- Output voltage, V_o = 48 V_{dc}
- Output power, P_{out} = 65 W
- Switching frequency, f_s = 50 kHz
- Maximum input current ripple, $\Delta i_{L1} < 25\%$ of fundamental current.
- Output voltage ripple, $\Delta v_o < 5\%$ of V_o

The main circuit component values are given according to the analysis presented in Sec. IV as: $L_1 = L_2 = 2.2$ mH, $L_3 = 68$ µH, $C_1 = C_2 = 1$ µF, and $C_o = 2200$ µF. Actual semiconductor models have been used in the simulation. The input and output diodes types are similar to the one presented in Sec. (IV.E). For the power switch, the IRFB4332PBF MOSFET with a series connect PDS3200 Schottky rectifier models have been implemented.

The simulation waveforms are shown in Fig. 7. It can be observed from Fig. 7(a) that the input line current is in phase with the input voltage. The percent of the total harmonic distortion in the input line current is 0.46%. Fig. 7(b) shows the voltage across the intermediate capacitors C_1 and C_2 along with the input voltage v_{ac}. It is clear from Fig. 7(b) that (1) is fully fulfilled. That is, v_{C1} closely tracks the positive portion of the input ac voltage (v_{ac}) while $-v_{C2}$ tracks the negative portion of v_{ac}. Likewise, Fig. 7(c) shows the two input diodes conduct in alternate half-line cycles as predicted by the analysis in this study. The waveforms of the three inductors' currents at peak input voltage are depicted in Fig. 7(d) which correctly demonstrates the DCM operating mode. Fig. 8 shows the simulated input voltage and input current waveforms for the coupled inductors case. The coupling coefficient is set to k = 0.18 according to (21). It is evident from Fig. 8 that the high frequency switching ripple current is significantly suppressed due to the coupling of the three inductors. Thus, the generated EMI noise level is greatly minimized as well as the requirement for the input filtering.

A laboratory prototype is built to validate the proposed topology and the simulation results. The experimental waveforms of the converter at full load are depicted in Fig. 9. The input voltage and the input line current (i_{ac}) waveforms are shown in Fig. 9(a). The input line current waveform is obtained without utilizing an input filter and results in a measured THD about 1.6%. Fig. 9(b) depicts the voltages across the intermediate capacitors C_1, C_2 and the input ac voltage. The waveforms of the three inductors' currents (i_{L1}, i_{L2}, and i_{L3}) during a few switching periods at peak input voltage are depicted in Fig. 9(c) which correctly demonstrates the DCM operating mode. A very good agreement can be seen between simulation and experimental results. Finally, the measured efficiency is about 92.8% at full rated load.

TABLE I.
A Comparison Between Conventional And Bridgeless Sepic PFC in DCM

Item		Bridgeless Sepic	Conventional Sepic
Slow diode		2	4
Fast diode		1	1
Switch		2	1
Current conduction path	Stage1	1 slow diode, 1 switch	2 slow diodes, 1 switch
	Stage2	1 slow diode, 1 fast diode	2 slow diodes,1 fast diode
	DCM	1 slow diode	2 slow diodes

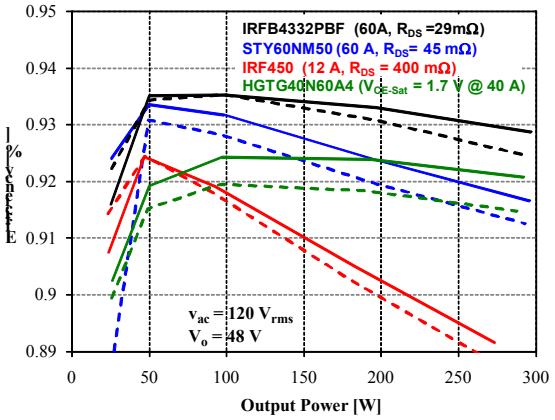

Fig. 6. Simulated efficiency of conventional PFC Sepic rectifier in Fig. 1(a) (dashed lines) and bridgeless PFC Sepic rectifier in Fig. 2(a) (solid lines) operating in DCM.

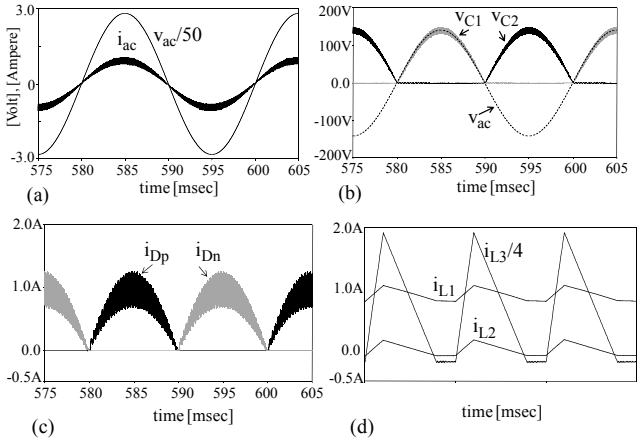

Fig. 7. Simulated waveforms for the converter of Fig. 2(a) in DCM.

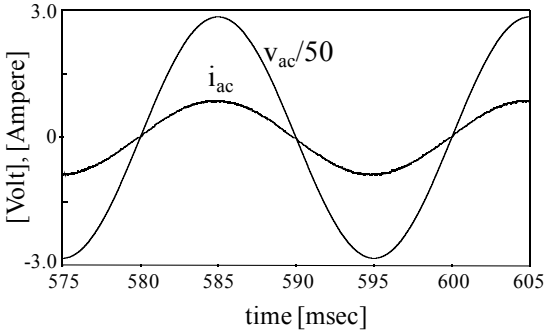

Fig. 8. Simulated waveforms for the converter of Fig. 2(c) in DCM.

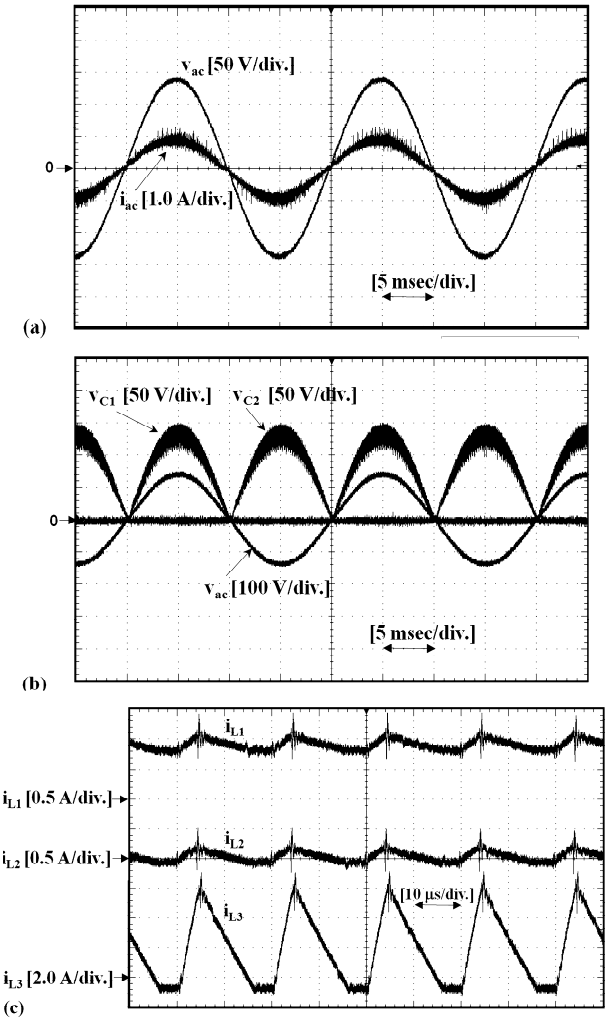

Fig. 9. Experimental waveforms for the converter of Fig. 2(a).

VI. Conclusion

Two new single-phase bridgeless rectifiers with low input current distortion and low conduction losses has been presented and analyzed. The proposed bridgeless rectifiers are derived from the conventional Sepic and Cuk converters. Comparing with conventional Sepic and Cuk PFC circuit, due to the lower conduction loss and switching loss, the proposed topologies can further improve the conversion efficiency. Namely, to maintain same efficiency, the proposed circuits could operate with higher switching frequency. Thus, additional reduction in the size of PFC inductor and EMI filter could be achieved. Besides improving circuit topology and performance, a further reduction in rectifier size could be realized by integrating the three inductors into a single magnetic core. Experimental results of the proposed bridgeless Sepic rectifier on a 65-W prototype at 100-V input voltage have been given to show high performance in terms of high power factor and efficiency.

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