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Advanced CAD tool for noise modeling of RF/microwave field effect transistors with large gate widths

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Abstract In the millimeter-wave frequency range, electromagnetic (EM) effects can significantly influence a device behavior. As the core of modern communication systems, active devices such as field effect transistors (FETs) require up-to-date models to accurately integrate such effects, especially in terms of noise performance since most of communication systems operate in noisy environments. Furthermore, to keep low-noise amplification over a wide frequency band, the transistor noise resistance R_n must be substantially reduced to make the system insensitive to impedance matching. Since this can be realized through large gate-width devices, a novel large gate-width FET noise model is proposed which efficiently integrates EM wave propagation effects, one of the most important EM effects in mm-wave frequencies.

Keywords CAD · Coupling · FET · Noise · Wave effects · Width

1 Introduction

Efficient models are the key of successful designs. Widely used in modern wireless communication systems, active devices such as field-effect transistors (FETs) require up-to-date models to achieve reliable circuit/system design especially in terms of noise performance since most of communication systems operate in noisy environments. Furthermore, to keep low-noise amplification over a wide frequency band, the transistor noise resistance R_n must be substantially reduced to make the system insensitive to impedance matching [1]. Since this can be realized through large gate-width devices, the noise behavior of such particular devices at millimeter-wave frequencies should be efficiently modeled [2–4]. Targeting this class of FETs is also due to the fact that at mm-wave frequencies, the gate width to wavelength ratio is higher than 10 or 20% favoring large-gate-width transistors [5].

Among existing FET modeling techniques, the full-wave modeling approach can be considered as the most reliable but is computationally expensive in terms of CPU time and memory [6]. On the other side, circuit equivalent models are fast but cannot accurately integrate EM effects. Therefore, a hybrid transistor model, called the semi-distributed model (Sliced model) has been proposed [7]. With the assumption of a quasi transverse electromagnetic (TEM) approximation, this model can be seen as a finite number of cascaded cells, each of them representing a unit transistor equivalent circuit. However, this model presents some limitations. In fact, in mm-wave frequencies, it cannot precisely take into account some EM effects that can significantly degrade the overall device behavior, like the wave propagation and the phase cancellation phenomena. To efficiently include such effects more general distributed models need to be developed. In this paper, a new distributed FET model is proposed. In this model [8], each infinitely unit segment of the device electrodes was divided into two parts namely, active and passive. The passive part describes the behavior of the transistor as a set of three coupled transmission lines while the active part that can be modeled by an electrical equivalent distributed circuit whose elements are all per-unit length.

To demonstrate the efficiency of our model in terms of noise, we applied the Laplace transformation to the device as an active multi-conductor transmission line structure and

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successfully compared its simulated response to measurements. Furthermore, by easily including the effects of scaling, the proposed algorithm is suitable for integration in computer-aided-design (CAD) packages for MMIC design.

2 Proposed FET noise model

An infinitely small element of the proposed transistor is shown in Fig. 1. In this figure, the element is represented by a six-port equivalent circuit which combines a distributed FET small-signal circuit model with a distributed network to account for the coupled transmission line effect of the electrode structure. In fact, in the proposed model, intrinsic/extrinsic parameters are all per unit length.

Based on the transmission line circuit theory, the model impedance and admittance matrices can be expressed as

$$\begin{aligned}[Z(\omega)] &= [R(\omega)] + j\omega[L(\omega)] \\ [Y(\omega)] &= [G(\omega)] + j\omega[C(\omega)] + [Y_{tr}]\end{aligned} \tag{1}$$

where $[R]$, $[L]$, $[C]$, and $[G]$ refer to the matrix representation of the well-known distributed circuit parameters of a transmission line namely, the resistance R, the inductance L, the capacitance C, and the conductance G, respectively. $[Y_{tr}]$ is accounted for the active parallel sub-section of the model. By solving the second-order differential equations of the model, its voltage and current vectors can be written as [9, 10]

$$[V(x)] = [S_v]\exp(-[\Gamma x])V^+ + [S_v]\exp(+[\Gamma x])V^- \tag{2}$$

$$[I(x)] = [S_i]\exp(-[\Gamma x])I^+ - [S_i]\exp(+[\Gamma x])I^- \tag{3}$$

where $[V(x)] = [V^d(x) \quad V^g(x) \quad V^s(x)]^t$ and $[I(x)] = [I^d(x) \quad I^g(x) \quad I^s(x)]^t$ represent the voltage and current vectors at the transistor terminals, respectively (Here d, g, and s stand for drain, gate and source, respectively). The superscript "t" refers to the vector transpose. Let the elements of matrix $[\Gamma]$ be the eigenvalues of $[Z]\cdot[Y]$ (or $[Y]\cdot[Z]$) and the elements of matrices $[S_v]$ and $[S_i]$ be the eigenvectors of $[Z]\cdot[Y]$ and $[Y]\cdot[Z]$, respectively [6]. By considering the boundary conditions of the six-port model, the unknown coefficients V^+ and V^- can be determined. Then, applying (2) and (3) for $x = 0$ and $x = w$, w being the gate width, the voltages and currents of each port can be obtained, leading to the 6*6 impedance ($[Z_l]_{6*6}$) and admittance ($[Y_l]_{6*6}$) matrices of the model, which can be easily transformed to the scattering matrix form.

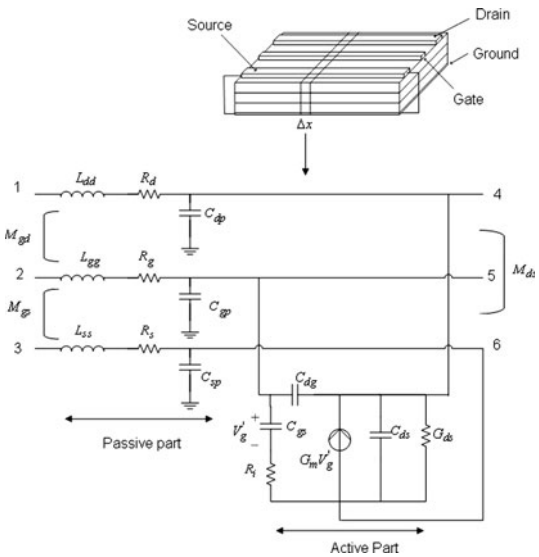

Fig. 1 Proposed model: representation of an infinitely small element

2.1 Three coupled excited transmission lines (distributed noise model)

By considering, for each unit element, both distributed voltage and current noise sources, the distributed noise FET model can be introduced, as shown in Fig. 2. Note that the sources are function of the x dimension to state for the distributed behavior. This model leads to the following set of partial equations

$$\begin{cases} \dfrac{d^2[V(x)]}{dx^2} - [Z(\omega)][Y(\omega)][V(x)] = [Z(\omega)][j] - \dfrac{d[v]}{dx} \\ \dfrac{d^2[I(x)]}{dx^2} - [Y(\omega)][Z(\omega)][I(x)] = [Y(\omega)][v] - \dfrac{d[j]}{dx} \end{cases} \tag{4}$$

Note that vectors $[v]$ and $[j]$ are the linear density of exciting voltage and current noise sources, respectively, while $[Z]$ ($[Y]$) represents the per-unit length impedance (admittance) matrix of the transmission line. By applying the Laplace transform to both sides of (4), this set of equations can be written as

$$s^2[V(s)] - [Z][Y][V(s)] = L\left\{[Z]\,[j] - \frac{d[v]}{dx}\right\} \tag{5}$$

The particular response for these equations is due to three modes of propagation coefficients γ_i and constant coefficients $[V_0^i]$ ($i = 1, 2, 3$), where $\gamma_i^2$are the eigenvalues

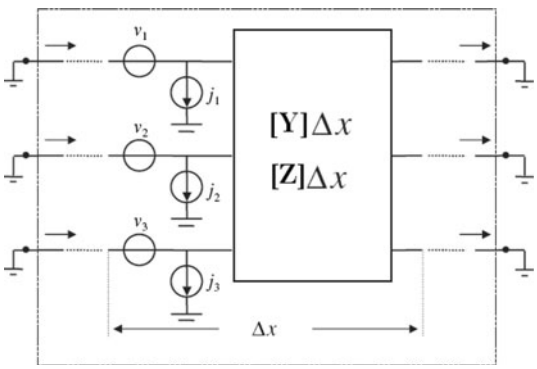

Fig. 2 The differential subsection of the excited transmission line

of the $[Z][Y]$ matrix and $[V_0^i]$ the eigenvectors. According to the single transmission line response, the particular response for the three coupled transmission lines can expressed as

$$[V_p(x)] = -[\Gamma^{-1}]\sinh([\Gamma x]) * ([Z][j]) + [\Gamma^{-1}]\sinh([\Gamma x]) * \frac{d[v]}{dx} \quad (6)$$

with

$$\sinh([\Gamma x]) = \begin{bmatrix} \sinh(\gamma_1 x) & 0 & 0 \\ 0 & \sinh(\gamma_2 x) & 0 \\ 0 & 0 & \sinh(\gamma_3 x) \end{bmatrix} \quad (7)$$

The total responses are then expressed as,

$$\begin{aligned}[V(x)] &= [S_v]\exp(-[\Gamma x])V^+ + [S_v]\exp(+[\Gamma x])V^- \\ &\quad - [\Gamma^{-1}]\sinh([\Gamma x]) * ([Z][j]) \\ &\quad + [\Gamma^{-1}]\sinh([\Gamma x]) * \frac{d[v]}{dx} \\ [I(x)] &= [S_i]\exp(-[\Gamma x])I^+ \\ &\quad + [S_i]\exp(+[\Gamma x])I^- - [\Gamma^{-1}]\sinh([\Gamma x]) * ([Y][[v]) \\ &\quad + [\Gamma^{-1}]\sinh([\Gamma x]) * \frac{d[j]}{dx} \end{aligned} \quad (8)$$

here "*" denotes the convolution operator (showing the superposition of all internal noise sources) while sinh ($[\Gamma x]$)is a square matrix which elements are the hyperbolic sine of those of $[\Gamma x]$.

2.2 Transistor internal noise sources

Referring to Fig. 3, let us consider a noisy infinitesimal subsection with gate width $\Delta x \to 0$. For each subsection, in fact a noisy six-port, a circuit model can be then assigned in the form of a noiseless six-port circuit with external equivalent noise sources at its inputs. In [6], a method to determine the density of these equivalent noise sources in the form of vectors of $[v]$ and $[j]$ was introduced. Therefore, (8) can be expressed as

$$\begin{aligned}[V(x)] &= [S_v]\exp(-[\Gamma x])V^+ + [S_v]\exp(+[\Gamma x])V^- \\ &\quad - [\Gamma^{-1}]\sinh([\Gamma x]) * ([Z][j]) \\ [I(x)] &= [S_i]\exp(-[\Gamma x])I^+ + [S_i]\exp(+[\Gamma x])I^- \\ &\quad - [\Gamma^{-1}]\sinh([\Gamma x]) * ([Y][v]) \end{aligned} \quad (9)$$

The above equations have been used to analyze the noise behavior of the transistor.

2.3 Transistor noise correlation matrix

The transistor noise performance can be fully determined through its noise correlation matrix, which, in turn, can be obtained by knowing the currents at external ports. The

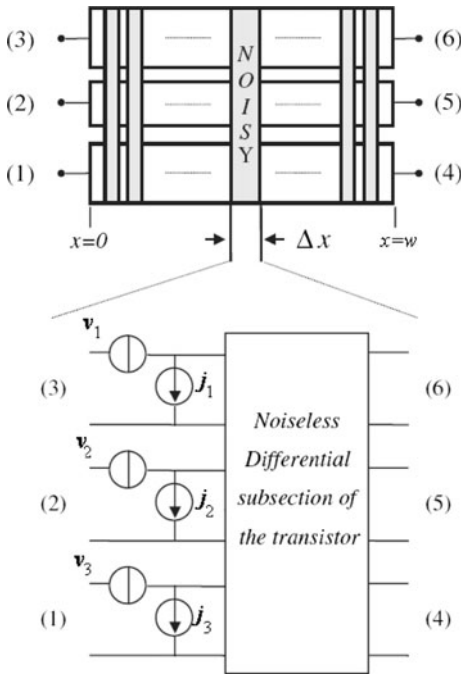

Fig. 3 Noise equivalent voltage and current sources

unit-per-length noise correlation matrix $[CA_{UPL}]$ of the transistor can be expressed as [10–12],

$$[CA_{UPL}] = \left\langle \begin{bmatrix} v \\ j \end{bmatrix} \begin{bmatrix} v \\ j \end{bmatrix}^+ \right\rangle = \left\langle \begin{matrix} [C_{11}] & [C_{12}] \\ [C_{21}] & [C_{22}] \end{matrix} \right\rangle \quad (10)$$

where "$\langle\rangle$"denotes the operator average and "+" the transpose complex conjugate. Now, let us assume first that $[v]$ and $[j]$ are known. Therefore, the unknown coefficients of (9) can be determined using the boundary conditions at short-circuited terminals:

$$\begin{cases} [V(x=w)] = [S_v]\exp(-[\Gamma w])V^+ + [S_v]\exp(+[\Gamma w])V^- \\ \quad - [\Gamma^{-1}]\left(\int_{x'=0}^{w} \sinh([\Gamma x'])dx'\right)[Z]\,[j] = [0_{3\times 1}] \\ [V(x=0)] = [S_v]V^+ + [S_v]V^- - [\Gamma^{-1}] \\ \quad \times \left(\int_{x''}^{w} \sinh([\Gamma x'])dx'\right)[Z]\,[j] = [0_{3\times 1}] \end{cases} \quad (11)$$

$$\begin{cases} [I(x=w)] = [S_i]\exp(-[\Gamma w])V^+ + [S_i]\exp(+[\Gamma w])V^- \\ \quad - (\cosh([\Gamma w]) - [U_{3\times 3}])([Z^{-1}][\,v]) \\ [I(x=0)] = [S_i]V^+ + [S_i]V^- - (\cosh([\Gamma w]) \\ \quad - [U_{3\times 3}])[Z^{-1}]\,[v] \end{cases} \quad (12)$$

where $[0_{3\times1}]$is a 3*1 vector of zeros. Using the above equations, the noise currents at the output ports can be written in a matrix form as

$$\begin{bmatrix} I_{no} \\ I_{nw} \end{bmatrix} = \begin{bmatrix} -[S_i] & [S_i] \\ [S_i]\exp(-[\Gamma w]) & -[S_i]\exp(+[\Gamma w]) \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \end{bmatrix} - \begin{bmatrix} -(\cosh([\Gamma w]) - [U_{3\times3}])[Z^{-1}][v] \\ (\cosh([\Gamma w]) - [U_{3\times3}])[Z^{-1}][v] \end{bmatrix} \tag{13}$$

Finally, the correlation admittance matrix of the noisy six-port FET can be written as

$$[CY_w] = \left\langle \begin{bmatrix} I_{n0} \\ I_{nw} \end{bmatrix} \begin{bmatrix} I_{n0} \\ I_{nw} \end{bmatrix}^+ \right\rangle \tag{14}$$

or

$$[CY_w] = \left\langle \left\{ ([M][K^{-1}][N_y]) \begin{bmatrix} j \\ j \end{bmatrix} - [N_z] \begin{bmatrix} v \\ v \end{bmatrix} \right\} \left\{ ([M][K^{-1}][N_y]) \begin{bmatrix} j \\ j \end{bmatrix} - [N_z] \begin{bmatrix} v \\ v \end{bmatrix} \right\}^+ \right\rangle \tag{15}$$

with

$$[N_y] = \begin{bmatrix} (\cosh([\Gamma w]) - [U_{3\times3}])[Y^{-1}] & [0_{3\times3}] \\ [0_{3\times3}] & (\cosh([\Gamma w]) - [U_{3\times3}])[Y^{-1}] \end{bmatrix}$$

$$[N_z] = \begin{bmatrix} (\cosh([\Gamma w]) - [U_{3\times3}])[Z^{-1}] & [0_{3\times3}] \\ [0_{3\times3}] & (\cosh([\Gamma w]) - [U_{3\times3}])[Z^{-1}] \end{bmatrix} \tag{16}$$

After some algebraic manipulations, we obtain

$$[CY_{tr}] = ([M][K^{-1}][N_y]) \left\langle \begin{bmatrix} j \\ j \end{bmatrix} \begin{bmatrix} j \\ j \end{bmatrix}^+ \right\rangle ([M][K^{-1}][N_y])^+ - ([M][K^{-1}][N_y]) \left\langle \begin{bmatrix} j \\ j \end{bmatrix} \begin{bmatrix} v \\ v \end{bmatrix}^+ \right\rangle ([N_z])^+ - ([N_z]) \left\langle \begin{bmatrix} v \\ v \end{bmatrix} \begin{bmatrix} j \\ j \end{bmatrix}^+ \right\rangle ([M][K^{-1}][N_y])^{-1} + [N_z] \left\langle \begin{bmatrix} v \\ v \end{bmatrix} \begin{bmatrix} v \\ v \end{bmatrix}^+ \right\rangle ([N_z])^+ \tag{17}$$

which can be reformulated as

$$[CY_{tr}] = ([M][K^{-1}][N_y]) \begin{bmatrix} CA^{22}_{U.P.L} & CA^{22}_{U.P.L} \\ CA^{22}_{U.P.L} & CA^{22}_{U.P.L} \end{bmatrix} ([M][K^{-1}][N_y])^+ - ([M][K^{-1}][N_y]) \begin{bmatrix} CA^{21}_{U.P.L} & CA^{21}_{U.P.L} \\ CA^{21}_{U.P.L} & CA^{21}_{U.P.L} \end{bmatrix} ([N_z])^+ - ([N_z]) \begin{bmatrix} CA^{12}_{U.P.L} & CA^{12}_{U.P.L} \\ CA^{12}_{U.P.L} & CA^{12}_{U.P.L} \end{bmatrix} ([M][K^{-1}][N_y])^{-1} + [N_z] \begin{bmatrix} CA^{11}_{U.P.L} & CA^{11}_{U.P.L} \\ CA^{11}_{U.P.L} & CA^{11}_{U.P.L} \end{bmatrix} ([N_z])^+ \tag{18}$$

Equation (18) shows that by having the per-unit length correlation matrix, the correlation matrix of the whole FET structure can be obtained.

3 CAD algorithms for noise analysis of mm-wave FETs

3.1 Multi-port network connection

In Fig. 4, a noisy multiport sub-network S of scattering matrix [*S*] is embedded in a noisy sub-network T of scattering matrix [*T*], with respective noise wave correlation matrices noted $[C_s]$ and $[C_t]$. Let $[S_{net}]$ and $[C_{net}]$ be the scattering and noise wave correlation matrices of the total network called N. The scattering matrix [*T*] of the embedding network T can be partitioned into sub-matrices that satisfy

$$\begin{bmatrix} b_e \\ b_i \end{bmatrix} = \begin{bmatrix} [T_{ee}] & [T_{ei}] \\ [T_{ie}] & [T_{ii}] \end{bmatrix} \begin{bmatrix} a_e \\ a_i \end{bmatrix} + \begin{bmatrix} c_e \\ c_i \end{bmatrix} \tag{19}$$

where subscript *i* designates the internal waves at the connections between the two-networks S and T while subscript *e* designates the external waves at the S_{net} terminals. The noise wave correlation matrix of network T is similarly partitioned such that

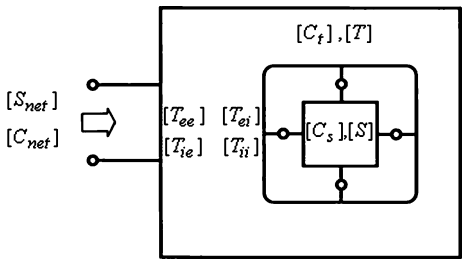

Fig. 4 A multiport sub-network S is embedded into a sub-network T. The resulted network N is characterized by the scattering and correlation matrices $[S_{net}]$ and $[C_{net}]$, respectively

$$[C_t] = \begin{bmatrix} \overline{c_e c_e^*} & \overline{c_e c_i^*} \\ \overline{c_i c_e^*} & \overline{c_i c_i^*} \end{bmatrix} \tag{20}$$

The resulting noise wave correlation matrix is then given by [12]:

$$[C_{net}] = \left[[I]|T_{ei}([\Gamma] - T_{ii})^{-1}\right][C_s]\left[[I]|T_{ei}([\Gamma] - T_{ii})^{-1}\right]^{+} \tag{21}$$

where $[I]$ is the identity matrix and $[\Gamma]$ the connection matrix expressed as

$$[b_i] = [\Gamma][a_i] \tag{22}$$

The scattering matrix of the total network N is then given by the well known expression [11]

$$[S_{net}] = [T_{ee}] + [T_{ei}]([\Gamma] - [T_{ii}])^{-1}[T_{ie}] \tag{23}$$

Note that this result gives a complete noise characterization of the network. A direct calculation of the new scattering matrix is now possible using (23). Note that the order of the matrix to be inverted was reduced by an amount equals to the number of the external ports.

3.2 Scattering and correlation noise matrices

According to the algorithm described above, let us consider the network shown in Fig. 5. In this figure, the ports of the transistor model are numbered from 1 to 24. Ports 23 and 24 are external ports while the rest are internal ports. Since most of the FETs are symmetrical, we can split their geometry into two identical parts. Figure 5 can be then decomposed into two equal parts of $w/2$ each (where w is the gate width) of respective scattering matrix $[S^{(1)}]$ and $[S^{(2)}]$.

Ports 13, 14 and 15 (the drain, the gate and the source) are terminated by the respective impedances Z_d, Z_g, and Z_s, whose reflection coefficients can be expressed as

$$S^{(3)} = \frac{Z_d - 1}{Z_d + 1} \tag{24}$$

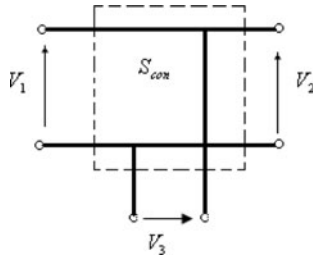

Fig. 6 Connection of the series network

Fig. 7 Load-pull bench used to characterize the device

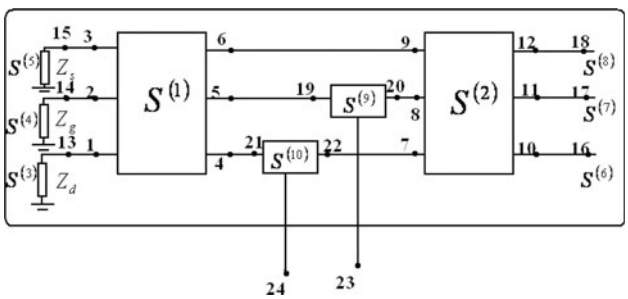

Fig. 5 Circuit model of the half structure of a FET with specific internal and external ports

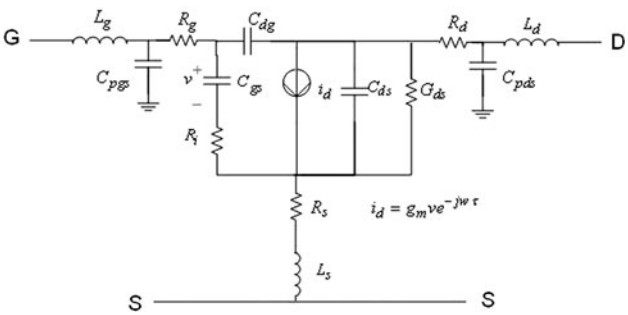

Fig. 8 Small-signal equivalent circuit of a FET

$$S^{(4)} = \frac{Z_g - 1}{Z_g + 1} \tag{25}$$

$$S^{(5)} = \frac{Z_s - 1}{Z_s + 1} = -1$$

(Source grounded at the end of the source electrode) (26)

described in [9] and [10]. As a result, we can use the proposed CAD algorithm to obtain the scattering and noise correlation matrices of the half-circuit structure.

The scattering matrix of a device is usually computed by partitioning its ports into two groups namely, external and internal ports. Thus, by separating the incoming and outgoing waves in (21), the computation of the connection matrix leads to the resulting scattering matrix

$$[S] = \begin{bmatrix}
\overset{23}{[s_{33}^{(9)}]} & \overset{24}{0} & \overset{1-6}{0} & \overset{7-12}{0} & \overset{13}{0} & \overset{14}{0} & \overset{15}{0} & \overset{16}{0} & \overset{17}{0} & \overset{18}{0} & \overset{19}{[s_{31}^{(9)}]} & \overset{20}{[s_{32}^{(9)}]} & \overset{21}{0} & \overset{22}{0} \\
[0_{6\times6}] & [s_{33}^{(10)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [s_{31}^{(10)}] & [s_{32}^{(10)}] \\
[0_{6\times6}] & [0_{6\times6}] & [S^{(1)}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] \\
0 & [0_{6\times6}] & [0_{6\times6}] & [S^{(2)}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] & [0_{6\times6}] \\
0 & 0 & 0 & 0 & [S^{(3)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & [S^{(4)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & [S^{(5)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & [S^{(6)}] & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [S^{(7)}] & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [S^{(8)}] & 0 & 0 & 0 & 0 \\
[s_{13}^{(9)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [s_{11}^{(9)}] & [s_{12}^{(9)}] & 0 & 0 \\
[s_{23}^{(9)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [s_{21}^{(9)}] & [s_{22}^{(9)}] & 0 & 0 \\
0 & [s_{13}^{(10)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [s_{11}^{(10)}] & [s_{12}^{(10)}] \\
0 & [s_{13}^{(10)}] & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & [s_{12}^{(10)}] & [s_{22}^{(10)}]
\end{bmatrix} \tag{29}$$

Let us now consider open circuit ports at $x = w/2$. We have then,

$$S^{(6)} = S^{(7)} = S^{(8)} = 1 \tag{27}$$

The only remaining components in Fig. 5 are the 3-port elements $S^{(9)}$ and $S^{(10)}$. Referring to that figure, we can observe that these components basically form the gate line and the drain line which form the series network (Fig. 6), respectively, in the transmission line model. Based on [12], their scattering matrix can be written as

$$[S^{(9)}] = [S^{(10)}] = [S_{con}] = \frac{1}{3}\begin{bmatrix} -1 & 2 & 2 \\ 2 & -1 & 2 \\ 2 & 2 & -1 \end{bmatrix} \tag{28}$$

In order to define $[C_s]$, we need to know the noise correlation matrices in the form of scattering matrices for all circuit elements. The correlation noise matrix for the six-port network representing half of the transistor gate width, i.e., $w/2$, can be computed using the techniques

Table 1 Values of the lumped elements (The transistor was biased at $V_{ds} = 3$ V and $I_{ds} = 10$ mA)

Lumped model values	Numerical values
L_g	0.383 nH
L_d	0.434 nH
Ls	0.094 nH
R_d	1.77 ohm
Rs	1.74 ohm
R_g	3.29 ohm
C_{pgs}	0.078 pF
C_{pds}	0.092 pF
C_{ds}	0.005 pF
C_{gd}	0.033 pF
g_m	41 mS
R_i	7.3 ohm
R_{ds}	231 ohm
C_{gs}	0.216 pF

Then, $[C_s]$ can be written as

$$[C_s] = \begin{bmatrix} [0_{2\times2}] & [0_{2\times6}] & [0_{2\times6}] & [0_{2\times10}] \\ [0_{6\times2}] & [C_s^{(1)}] & [0_{6\times6}] & [0_{6\times10}] \\ [0_{6\times2}] & [0_{6\times6}] & [C_s^{(2)}] & [0_6^{(10)}] \\ [0_{10\times2}] & [0_{10\times6}] & [0_{10\times6}] & [0_{10\times10}] \end{bmatrix} \quad (30)$$

Note that based on the proposed algorithm, a designer can easily obtain the scattering matrices of any microwave transistor, highlighting the ease of implementation of the proposed model into existing commercial simulators.

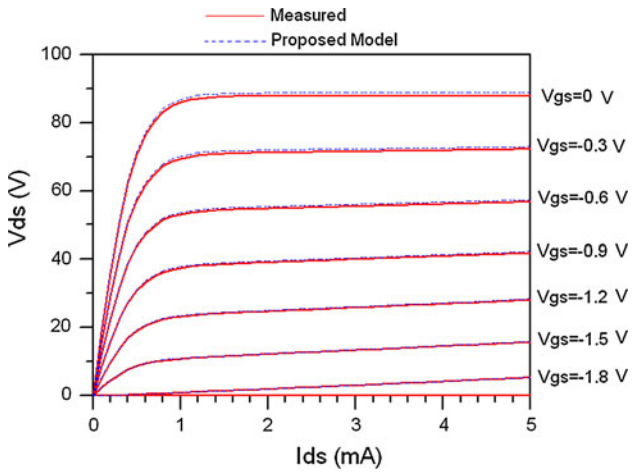

Fig. 9 I–V curves for the NE710

4 Numerical results

The proposed approach was used to model a sub micrometer-gate GaAs transistor (NE710) [14]. The device has a 0.3 μm × 280 μm gate. The first step consisted to characterize the transistor. In this work, we used a bench from Focus microwave that consists on a probing station, the HP 8340B synthesized signal generator, the Agilent 8565EC spectrum analyzer, the CMMT1808 tuners, the Anritsu ML2438A power meter, and the Agilent ML2438A power supplies (Fig. 7).

The intrinsic equivalent circuit model (Fig. 8) was obtained using well-known hot and cold modeling techniques [13]. After removing the extrinsic components via de-embedding methods, a hot modeling technique was utilized to obtain the intrinsic elements. Then, an optimization was performed by varying the values of the intrinsic FET elements in the vicinity of 10% of their mean value until the error between measured and modeled S-parameters was found acceptable (i.e., less than 2%). The obtained values of the extrinsic and intrinsic elements are summarized in Table 1.

Figure 9 shows a good fitting between measured and modeled data for various dc and pulsed voltages while Fig. 10 shows the experimental load-pull characteristics of the transistor. When matched, it has an output power of 16 dBm with a 10% PAE at 10 GHz. In Fig. 10, the output RF power is shown as a function of the complex output impedance matching conditions of the device. The transistor S-parameters over a frequency range of 1–26 GHz are plotted in Fig. 11. As expected, compared to measurements, our proposed model is more accurate than the slice model [7], especially at the upper part of the frequency spectrum, when the device physical dimensions are

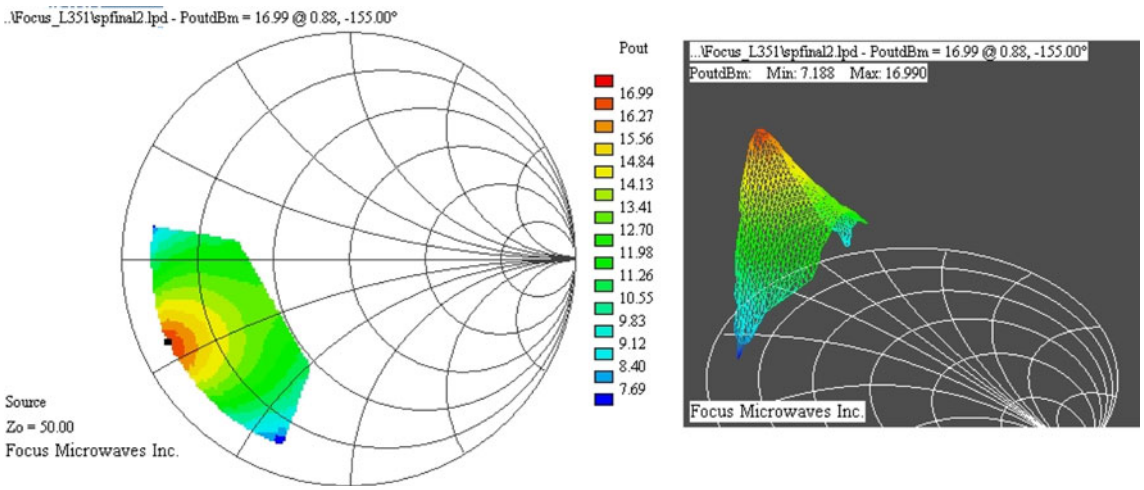

Fig. 10 Output power as function of load impedance for an optimized structure at 10 GHz

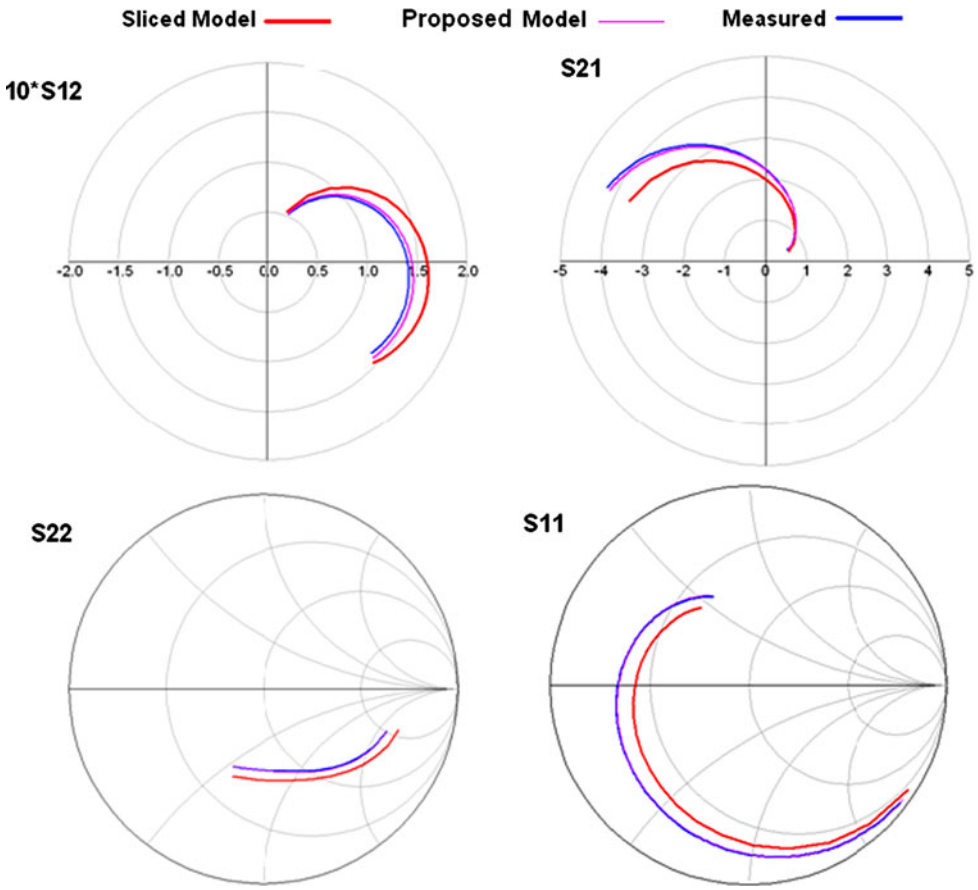

Fig. 11 NE710: Comparison between the measured S-parameters and those generated by the sliced and the proposed model

comparable to the wavelength. This is due to the fact that our model is based on the full-wave equation while the slice model is based on an electrical equivalent circuit model. Figure 12 shows the noise figure obtained for three different frequencies. Thus, the proposed wave analysis can be applied for accurate noise analysis of FET circuits. To further prove the accuracy of the proposed wave approach in noise analysis, our results were successfully compared to measurements (Fig. 13).

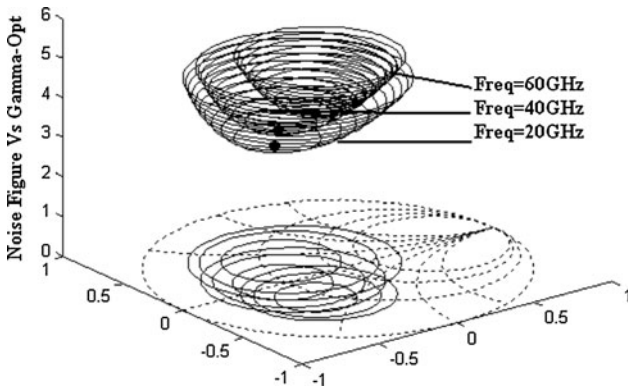

Fig. 12 Noise figure circles for three different frequencies versus the source admittance

For larger widths, the thermal noise of the gate increases due to the higher gate resistance while for smaller gate widths, the minimum noise figure increases as the capacitances do not scale proportionally with the gate width due to an offset in capacitance at gate width zero [2]. Therefore, we highlighted these effects of gate width on a transistor noise performance by simulating the minimum noise figure and the normalized equivalent noise admittance for three values of the gate width, e.g., 140, 280 and 560 μm (Fig. 14). These values were selected based on the device we modeled. In fact, the NE710 has a gate width of 280 μm, so we took half of that value as well as its double to bound the device behavior and highlight the effect of gate width on a FET performance.

5 Discussions

The transistor modeling approach presented in this paper is mainly developed for computer-aided design implementation, making it suitable for any FET circuit topology up to

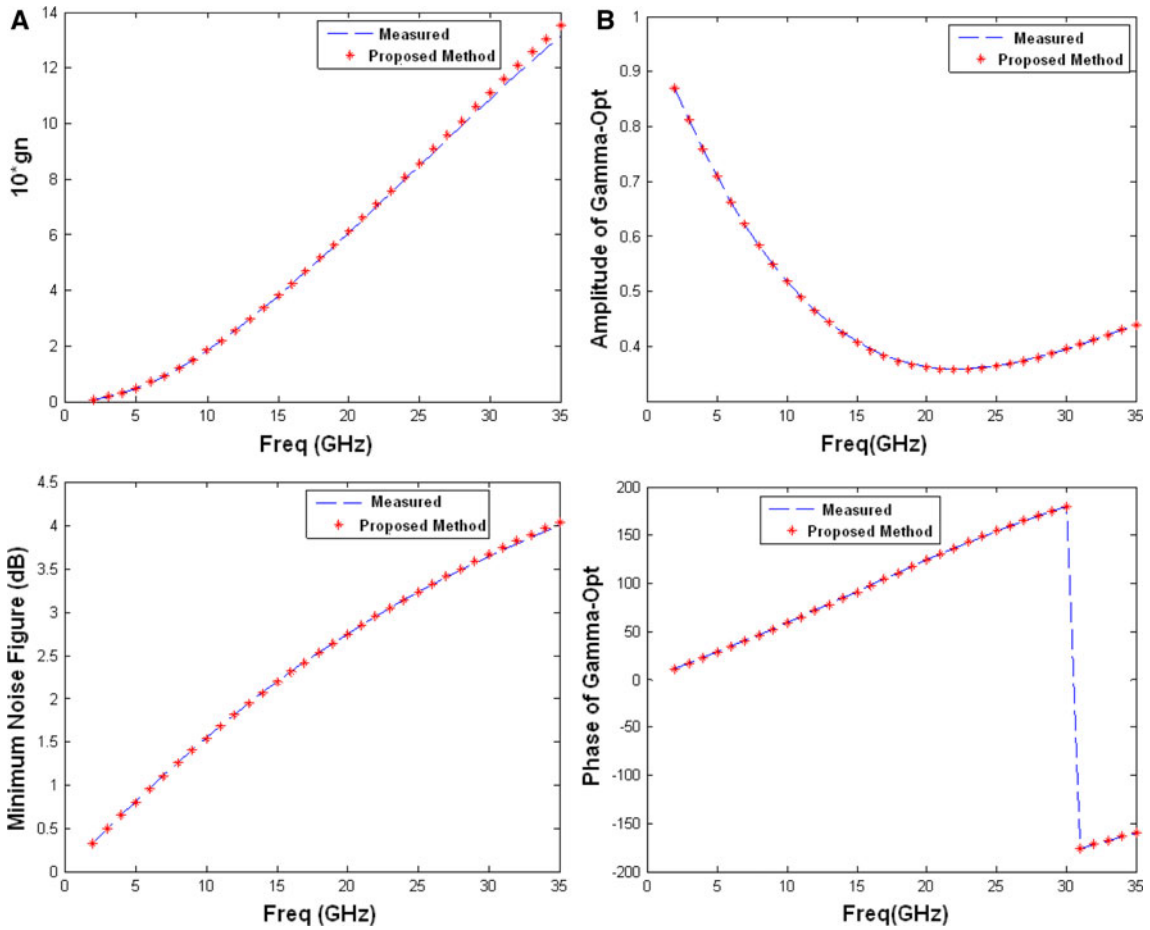

Fig. 13 **a** Normalized equivalent noise admittance and noise figure: Comparison between the proposed method and measurements. **b** Amplitude and phase of the optimum reflection coefficient: Comparison between the proposed method and measurements

the millimeter-wave range and thus, can be easily implemented and used in commercial software. As illustrated in Fig. 15, the proposed model was implemented in ADS [15] and the results obtained from the code we developed have been successfully compared with those obtained by the same model after being implemented in the ADS library and used as an internal device. This step shows that the proposed model can be used in any microwave integrated circuit design performed by a commercial simulator.

It has also to be noted that even if the proposed model is suitable for any FET structure, large-gate width devices have been targeted in the present work. In fact, this specific type of transistors can handle high output power levels, making them suitable for power amplifier design.

6 Conclusion

Using a new CAD algorithm, the noise modeling and analysis of microwave FET have efficiently been studied. In fact, since only half of a FET length is used, instead of the whole structure, the computation time will be significantly affected. Besides, the implementation of this CAD technique in modern microwave and mm-wave simulators is straightforward and will give more reliable results for circuit performance like low-noise amplifiers. Also, as for practical applications, large gate periphery devices are used to generate sufficient output power levels. With the increase of the device gate periphery, the self-heating effect and the defect trapping effect will both be more profound.

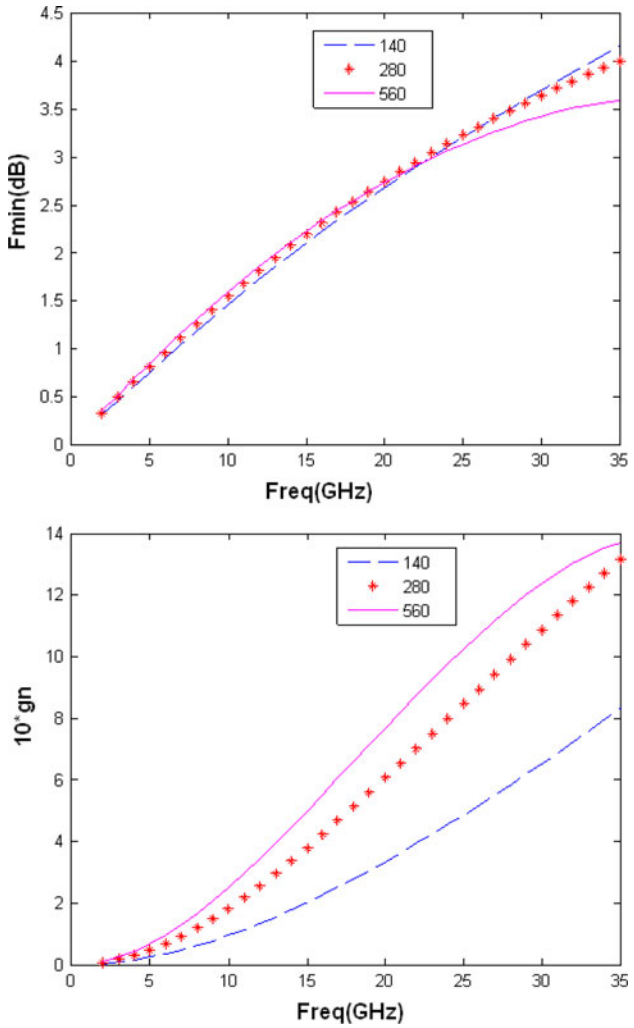

Fig. 14 Minimum noise figure and normalized equivalent noise admittance of the transistor for three different values of gate width (μm)

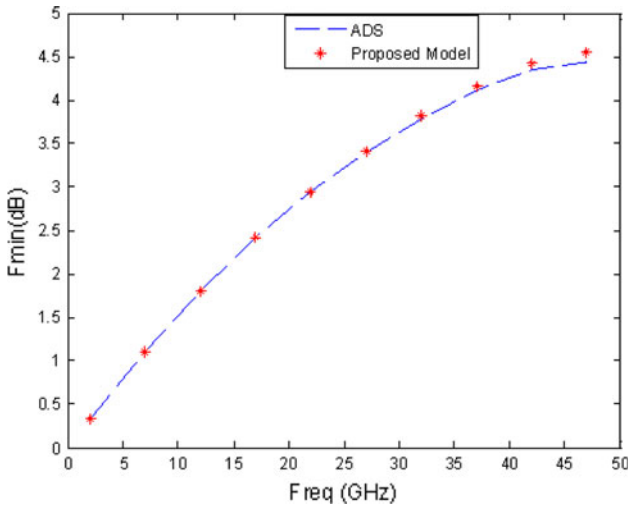

Fig. 15 Comparison between simulated minimum noise figure obtained from our developed code and from ADS using our model

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