Integrated Single-Inductor Buck-Boost or Boost-Boost DC-DC Converter with Power-Distributive Control

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***Abstract*—This paper presents a fully integrated single-inductor dual-output (SIDO) buck-boost or boost-boost DC-DC converter with power-distributive control. This converter works under voltage mode control to have better noise immunity, uses fewer power switches/external compensation components to reduce cost, and is thus suitable for system on chip (SoC) applications. The proposed SIDO converter was fabricated in TSMC 0.35 μ m 2P4M CMOS technology with input supply voltage 2.7-3.3 V. The first output V_{O1} can operates either at buck mode or boost mode (output voltage in between 2.5V to 5V), while the second output V_{O2} can only operates at boost mode (output voltage 3.6V).**

Keywords-component; buck/boost-boost converter; single inductor; power distributive convtrol

I. INTRODUCTION

Today's modern battery-operated portable products demands for advanced power management integration in SoC chips [1]. To minimize power consumption, multiple supply voltages and dynamic voltage scaling schemes are widely adopted [2]. Recently, several single-inductor multiple-output (SIMO) DC-DC converters [3-10] have been proposed as the most promising solution to minimize component (inductor and power switch) counts/footprints and production cost. However, there exists many design challenges for the SIMO converters, such as cross-regulation, efficiency, system stability, and flexibility, for achieving better step-down and step-up conversion.

The operational principles of SIMO DC-DC converters are based on time-multiplexing approaches [11], which deliver energy stored in the inductor to each output in every switching cycle by means of different feedback control mechanisms. They can be classified as voltage control [3-5], peak current control [6-7] [10], and charge control [8-9]. In terms of inductor current waves, converters are divided into discontinuous conduction mode (DCM) [3] [7], pseudo-continuous conduction mode (PCCM) [4] [8-9], continuous conduction mode (CCM) [5], and DCM/CCM [6]. They also can be sorted into boost/boost converters [3-4] [6-7], buck/buck converters [5], and hybrid buck/boost converters [8-10] by using output voltage types. For the embedded SIMO DC-DC converter in SoC application, although voltage control is slower than current mode control, it has no external current sensors and good noise immunity. Hence, voltage control is more suitable than current control in embedded SoC environments. Converters operated in DCM or PCCM of the conventional time-multiplexing approaches [3-4] will avoid cross-regulation, but DCM suffers large current ripples and has current driving problems. Although PCCM overcomes limitations of DCM, it dissipates unnecessary power due to non-zero current in resistance of inductor and the freewheel-switch. Converters operating in CCM suffer serious cross-regulation problems and are difficult to consider stability analysis [4]. In general, SIMO converters have to combine several compensators which have the same number of output voltage. Recently, there is a reference [6] proposes ordered power-distributive control (OPDC), which can operate in DCM/CCM, and using only one compensator. Besides, compared with familiar SIMO converters [3-4], this time-multiplexing power-distributive approach of [5-9] has less switching number in one cycle, therefore it increase efficiency.

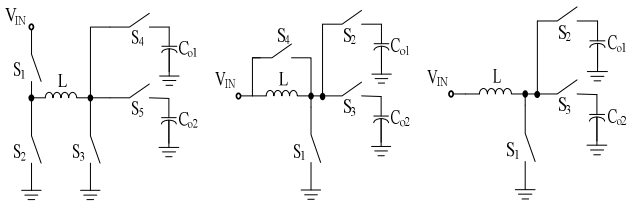

Fig. 1. Architecture of the buck-boost dc-dc converter.

In many applications, there are need for a single-inductor dual-output DC-DC converter with one output voltage set to be lower (buck) and another higher (boost) than the supply voltage. In traditional SIDO buck/boost converters shown in Fig.1 (a), there are five power switches [10]. Fig.1 (b) is another implementation of four power switches [8-9]. This paper adopts the Fig.1 (c) (reduce freewheel-switch S_4 of Fig.1 (b)) topology which has three power switches, and it uses power-distributive control from [6] and applies them to voltage control. Thus, there needs only one output compensation loop, which reduce the amount of external

compensated components used, such as [6]. Moreover, this paper also extends the availability of Fig.1(c) topology to implement Buck-Boost or Boost-Boost converter according to different demands.

In this paper, operation and control of the proposed SIDO converter and the effect of cross regulation are discussed in Section II. Section III presents circuit design and implementation issues. Post-layout simulation and results are shown in Section IV. The conclusions are given in Section IV.

II. OPERATION OF SIDO BUCK-BOOST CONVERTER

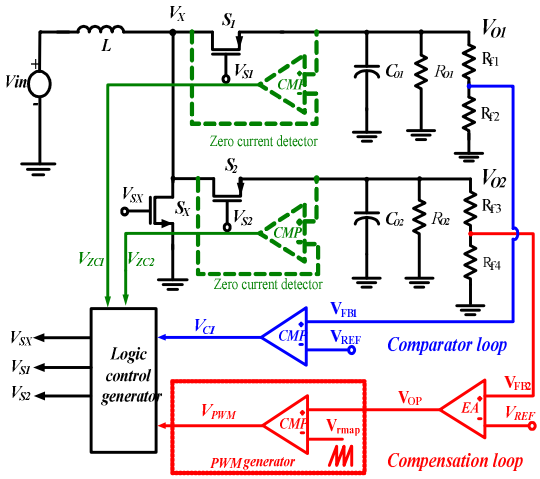

Fig. 2. Architecture of the proposed buck-boost or boost-boost dc-dc converter.

A. Architecture and Control Strategy

The architecture of the SIDO buck-boost or boost-boost DC-DC converter in power-distributive control with one compensator is shown Fig. 2. The output V_{O1} is controlled by the comparator loop, which determines the switching from V_{O1} to V_{O2}. The output V_{O2} is controlled by compensation loop that is responsible for compensating the total control loop. The logic control generator is used to control the timing of the converter. The zero current detectors prevent the reversed inductor current.

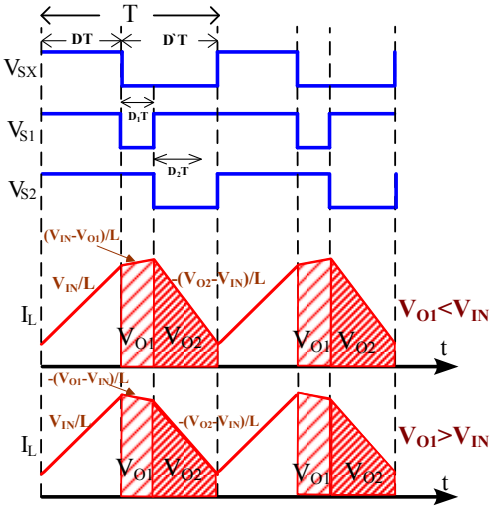

Fig. 3. Timing diagram of buck-boost or boost-boost dc-dc converter.

The operational principle is explained in the timing diagram shown in Fig. 3. The duty-cycle D is determined by PWM generator. During the DT period, the S_X is turned ON, and all other switches are turned OFF. The inductor current ramps up with the slope of Vin/L until the output of the error amplifier V_{OP} is equal to the ramp signal. S_X is then turned OFF, and the inductor is connected to V_{O1} by turning ON S_1. During the D_1T, as soon as the comparator detects V_{O1} is larger than its target voltage, S_1 is turned OFF and the inductor is switched to V_{O2}. If V_{O1} is lower than Vin, the inductor current ramps up with the slope of (Vin-V_{O1}/L), otherwise ramps down with the slope of V_{O1}/L. That is to say V_{O1} can be buck or boost output During the D_2T, the inductor current ramps down with the slope of (V_{O2}-Vin/L) until the next DT starts.

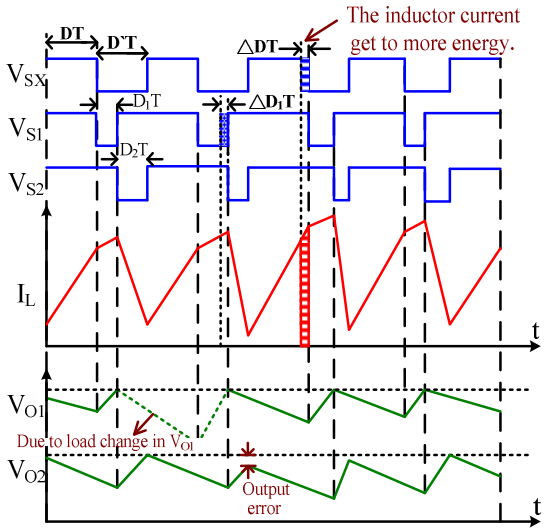

Fig. 4. Timing diagram of the proposed converter encounter cross regulation due to load change in V_{O1}.

B. Cross Regulation

The outputs of the SIMO DC-DC converter control by time-multiplexing power-distributive approaches will cross regulate among themselves, no matter in DCM or in CCM, because they are coupled together and influenced the duty cycles mutually. Our proposed converter can maintain desirable low cross-regulation which is explained in Fig. 4. Suppose that the load current suddenly increases in V_{O1}, which makes V_{O1} drop below the predetermined voltage. While detecting that, the comparator loop increases the duration, $\triangle D_1T$, to deliver more energy of inductor current to V_{O1} until V_{O1} is larger than its required voltage. Then, due to increasing external energy abruptly in V_{O1}, remainder energy of inductor current delivered to V_{O2} is decreased so that V_{O2} drops. In other words, the output error of the comparator-controlled V_{O1} is transferred and accumulated to V_{O2}. Receiving the voltage error of V_{O2}, PWM generator of the compensation loop extends the duty DT to get more energy from the inductor. At the same time, D_1T is reduced by the comparator to maintain V_{O1}. Finally, V_{O1} and V_{O2} return their required voltages levels, and the proposed converter achieved low cross-regulation by

comparator's fast response property.

III. CIRCUIT IMPLEMENTATION

A. Logic control generator

The block diagram of the logic control generator in proposed buck-boost or boost-boost DC-DC converter is shown in Fig. 5. The logic control generator is constructed of one S-R latch and two three-input NAND logic gates. When the comparator detects the feedback voltage V_{FB1} of V_{O1} is larger than the V_{REF}, the signal V_{C1} is hold on by S-R latch during the duration D'T. The output signal of S-R latch Q_1 and Q_1_b relative to the signals V_{S2} and V_{S1} which are control output switch S_2 and S_1, respectively. Therefore, the comparator determines the inductor connected from V_{O1} to V_{O2}. The signal V_{pluse} reset the S-R latch every switching cycle. The signal V_{PWM} is generated by PWM generator. When V_{PWM} is active, both V_{S1} and V_{S2} are at high level so that the switch S_1 and S_2 are turned OFF. Similarly, when the inductor current is zero, the signal V_{ZC1} or V_{ZC2} is active so that the switch S_1 or S_2 is turned OFF, respectively.

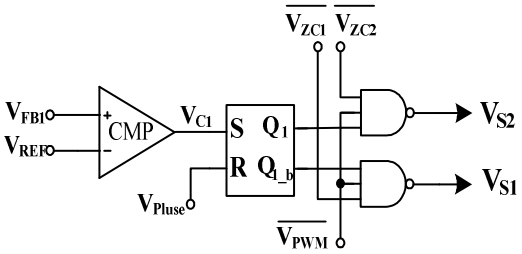

Fig. 5 Block diagram of the logic controller generator.

B. Zero-current detector

The zero-current detector applies CMOS-Control Rectifier (CCR) technique [12] presented in this paper. The block diagram of CCR is shown in Fig. 6. It composes of crossed-coupled comparators and a coupling-capacitor C_c. In our proposed converter, the variation of output voltage can be large in range. The comparator solves the common-mode voltage limitation in differential-input comparators with current bias. When the inductor current goes to zero, the comparator detect that the V_{OUT} is larger than V_X. Therefore, the signal V_{ZC} is activated to prevent the reversed inductor current from V_{OUT} to V_X.

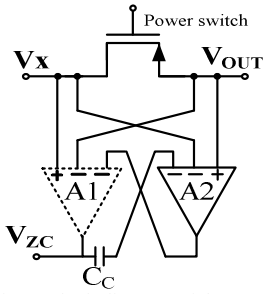

Fig. 6 Block diagram of the CCR.

IV. POST-LAYOUT SIMULATION RESULTS

The single-inductor dual-output buck-boost or boost-boost DC-DC converter is implemented with a TSMC 0.35µm 2P4M CMOS process. The overall layout view of SIDO converter is shown in Fig. 12. The performance is summarized in Table I. The supply voltage of converter can range from 2.7V to 3.3V. The switching frequency is 400 KHz with single inductor of 10uH. Both outputs use filtering capacitors of 4.7uF.

Fig. 8 shows the simulated output voltage of the buck-boost converter regulated at 2.5V, and 3.6V, with voltage ripple V_{OUT1}=50mV and V_{OUT2}=50mV, respectively. The output currents are I_{out1}=50mA, I_{out2}=90mA. Fig. 9 shows the simulated output voltage of the boost-boost converter regulated at 5V, and 3.6V, with voltage ripple V_{OUT1}=50mV and V_{OUT2}=40mV, respectively. The output currents are I_{out1}=60mA, I_{out2}=200mA. Fig.10 shows the results of a cross-regulation test with a supply voltage of 3V. V_{OUT2} is set to 3.6V, driving 90mA to its load. V_{OUT1} present a variation from buck output voltage of 2.5V to boost voltage of 3.3V with I_{OUT1} rise up from 50 to 66mA. The output voltage of V_{O2} drop due to the cross-regulation is less then 200mV.

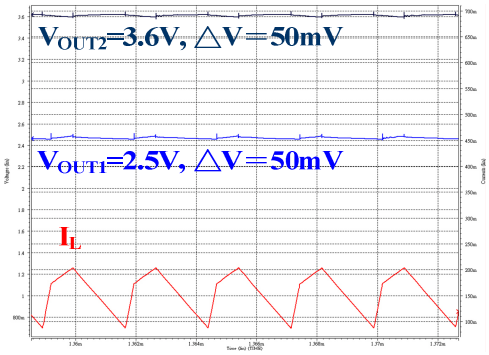

Fig. 8 Simulated output voltage.

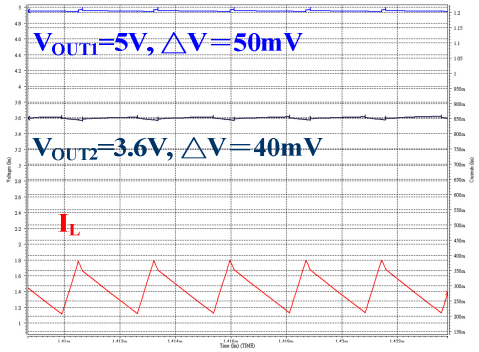

Fig. 9 Simulated output voltage.

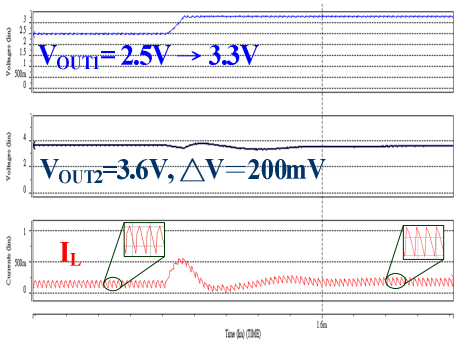

Fig. 10 Cross-regulation simulations.

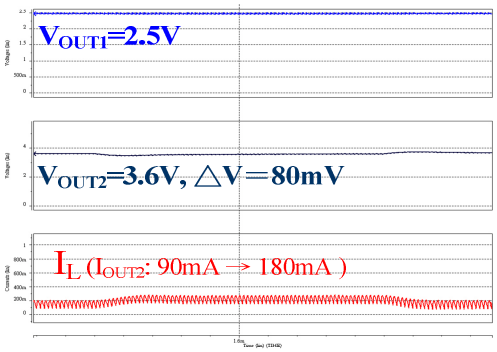

Fig. 11 Load-regulation simulated results.

Fig. 11 shows the simulation results of a load-regulation test. The two output voltages are set to 2.5V and 3.6V. I_{OUT2} has a step-up from 90mA to 180mA and vice versa while I_{OUT1} is fixed at 50mA.The V_{OUT2} voltage drop is of about 100mV. Load regulation standards for commercial products are satisfied.

TABLE I
SUMMARY OF THE CONVERTER PERFORMANCE

Input voltage range	2.7～3.3V			
Inductor	10uH			
Capacitor/ESR	4.7uF/50mΩ			
Oscillator frequency	400kHz			
Chip area	1.7x1.1 mm^2			
Process	TSMC 0.35m CMOS			
Efficiency (max)	90.6%*			
Type of Output	Boost-Boost		Buck-Boost	
Output voltages	5V	3.6V	2.5V	3.6V
Output ripple(max)	50mV	40mV	50mV	50mV
Load current	60mA	200mA	50mA	90mA
Cross regulation	0.6V/A	0.6V/A	0.6V/A	0.7V/A

*@ V_{IN}=3V,V_{OUT1}=2.5V,V_{OUT2}=3.6V,I_{OUT1}=50mA,I_{OUT2}=90mA

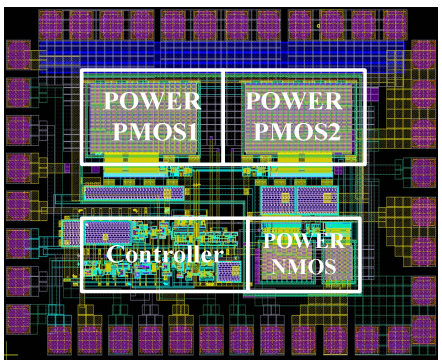

Fig. 12 The layout view of the SIDO buck-boost converter.

V. CONCLUSIONS

This paper presents a single-inductor dual-output buck-boost or boost-boost DC-DC converter in power-distributive control using only one compensator. In this work, the conventional dual-output boost converter can be extended to the buck-boost converter by substituting the voltage comparator to the error amplifier. There is no need to alter internal circuit and compensator. Furthermore, the proposed converter requires fewer switches, uses one compensator only and reduces the circuit complexity. Compared to prior buck-boost converters, the proposed converter is more suitable for a SoC application.

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