20-Mb/s Erase/Record Flash Memory by Asymmetrical Operation

Takayuki Kawahara, *Member, IEEE,* Yusuke Jyouno, Syun-ichi Saeki, Naoki Miyamoto, and Katsutaka Kimura, *Member, IEEE*

***Abstract*—An asymmetrical recording and erasing operation of Flash memory is proposed where the threshold voltage of erase and record states are set above the thermal equilibrium threshold voltage. The recording rate is made ten times faster by using this method along with two other proposed methods: accurate control of the fastest bit and continuous recording using two memory banks. The erasing rate is also made ten times faster by using large-scale parallel operation made practical by a proposed multiphase word-driving scheme. These proposed circuit technologies will enable 20-Mb/s erase/record Flash memories for use in personal high-definition television (HDTV) movie cameras.**

***Index Terms*—Asymmetrical operation, Flash memory, HDTV, movie camera.**

I. Introduction

RAPID advances are being made in digital camera technology. The pixel density of the charge-coupled devices used in low-end still cameras is expected to increase from 400k to 800k over the next few years. Digital movie cameras are also being developed. This trend requires increasing the large file memory in such cameras. Because the file memory should be removable, magnetic tape, hard-disk drives, digital-video-disk RAM, and nonvolatile semiconductor memory are potential solutions.

Flash memory densities of 64 Mb [2], [3] and 128 Mb [4], [5] have been reported. These memories are designed to be erased and programmed (recorded) by Fowler–Nordheim (F–N) tunneling and store binary or multivalue information, respectively, in each cell. They are highly resistant to mechanical shock and vibration and have low power consumption. They are thus attractive for use as file memory in digital still and movie camera applications (Fig. 1). The captured images are stored in a Flash memory card in a standard format, such as JPEG, MPEG-1, or MPEG-2. The images in the Flash memory can be used for various purposes. They can be downloaded to a storage device. They can be printed out. And they can be taken in PC's. Digital cameras are thus expected to gain wide-spread use.

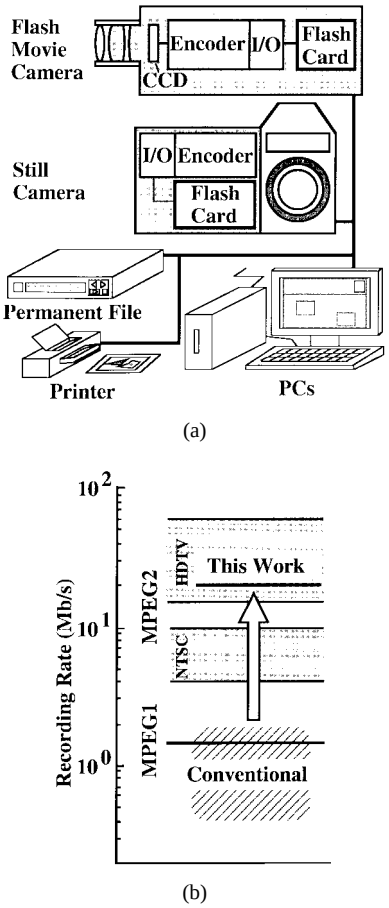


Fig. 1. Flash memory for camera applications: (a) camera systems and (b) recording rate.

Future advances in technology will bring about personal hihg-definition television (HDTV) movie cameras with MPEG-2 encoders. The target recording rate for such cameras is 20 Mb/s, one order of magnitude faster than that of conventional Flash memory. To attain this target, we propose high-speed erase/record circuit technologies based on asymmetrical operation, in which the thermal equilibrium threshold voltage is set below the threshold voltage of the recording state. This scheme along with accurate fastest-bit control, continuous recording, and multiphase word driving, should make 20-Mb/s erase/record Flash memory with the features shown in Table I attainable.

Manuscript received February 10, 1997; revised May 16, 1997. This paper was presented in part at 1996 Symposium of VLSI Circuits [1].

T. Kawahara is with Electronics Laboratory (LEG), Swiss Federal Institute of Technology Lausanne (EPFL), CH-1015 Lausanne, Switzerland on leave from Central Research Laboratory, Hitachi Ltd., Tokyo, Japan.

Y. Jyouno is with Semiconductor and Integrated Circuits Division, Hitachi Ltd., Tokyo, Japan.

S. Saeki and N. Miyamoto are with Hitachi Device Engineering Company Ltd., Chiba, Japan.

K. Kimura is with the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan.

Publisher Item Identifier S 0018-9200(98)00376-X.

TABLE I
FEATURES OF MOVIE CAMERA APPLICATION

Recording rate	**20 Mb/s (MPEG2, HDTV)**
Recording time	**60 min. (9 GB)**
Maximum interval between down loads to permanent file	**1 month**
Total number of complete uses (60 min.)	**10^4**

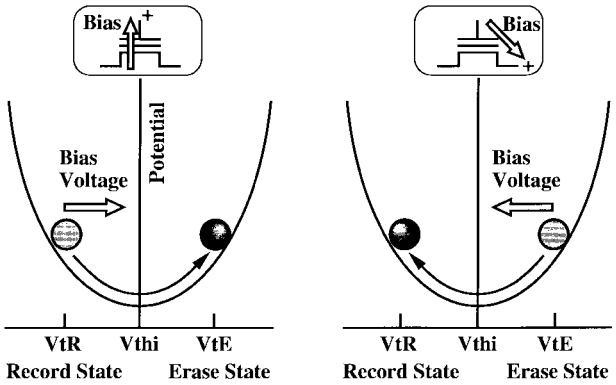


Fig. 2. Conventional symmetrical operation: (a) erasing and (b) recording.

In Section II we describe the concept of asymmetrical erasing and recording, and in Section III we discuss its operation and performance. High-efficiency recording is described in Section IV, high-speed erasing is described in Section V, and the disturbance and retention of our proposed and the conventional schemes are compared in Section VI.

II. CONCEPT OF ASYMMETRICAL ERASE/RECORD OPERATION

In this paper, the threshold voltage of a memory cell is assumed to be changed by using F–N tunneling and recording operation to be done to plural memory cells (e.g., 512B) by parallel using data latch circuits. The example of this type of memory cell is known as AND [2] or NAND [4] type, which also has an advantage of its smaller cell size compared to the conventional NOR type memory cell.

A. Conventional Erasing and Recording

A Flash memory cell has a thermal equilibrium state where the tunneling current flowing in and out of the floating gate is balanced around the entire surrounding insulator region, as shown schematically in Fig. 2. This state is approximately achieved by irradiating an ultraviolet light on the cell. This state is expressed using a threshold voltage of V_{thi}. The erase and record states are on either side of the thermal equilibrium state and are in the potential field toward the equilibrium state. In the conventional scheme, V_{thi} is set near the midpoint between the erase and record states to achieve symmetrical erase/record operation. When the Flash memory is shut down, both states slowly move toward the thermal equilibrium state over many years.

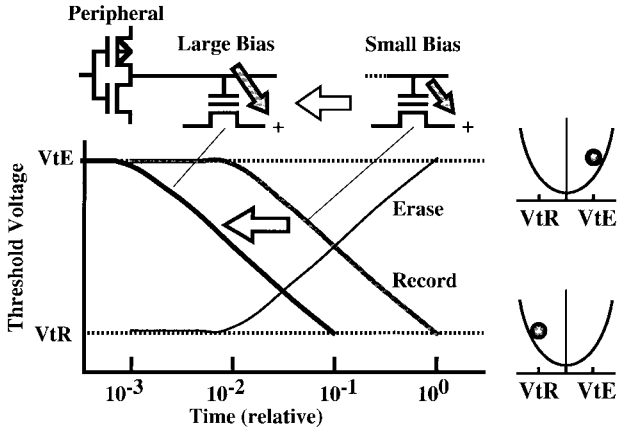


Fig. 3. Fast recording in conventional method.

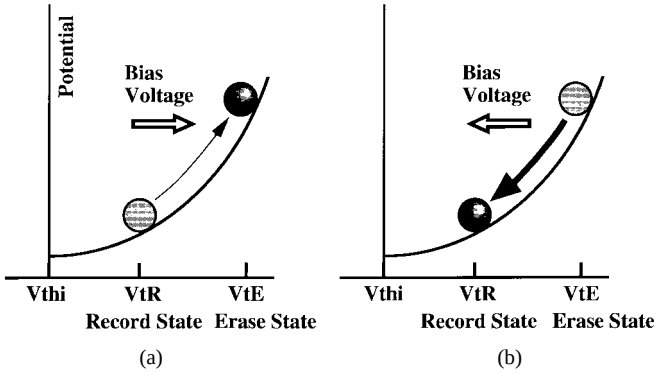


Fig. 4. Proposed asymmetrical operation: (a) erasing and (b) recording.

To change the state, a bias voltage is applied through the external terminal of the target memory cell transistors. Here, we assume an AND-type memory cell. To erase, a bias voltage is applied to the control gate and to the substrate of the target memory cell [Fig. 2(a)]. After applying the bias voltage, all of the cells in the selected sector are thereby transferred to the erased state. To record, a bias voltage is applied to the control gate and to the selected drain terminal of the target memory cell transistors [Fig. 2(b)]. The state of selected memory cells is thereby changed from the erased state to the recorded state through the V_{thi} state.

In the conventional method, the erase and record characteristics are symmetrical, as shown in Fig. 3. The bias voltage is set as high as possible within the breakdown margin of the MOS transistors in the peripheral. In other words, these transistors can be designed to have only the necessities, and not a generous breakdown margin. Therefore, recording cannot be accelerated by applying a large bias voltage in the actual chip. Another approach is to increase the number of parallel operations. However, this is no longer practical because it requires increasing the number of latch circuits, and thus the chip area overhead.

B. Asymmetrical Erasing and Recording

The concept of our proposed asymmetrical operation is simple and shown schematically in Fig. 4. In this scheme, the thermal equilibrium threshold voltage V_{thi} is set below the threshold voltage of the record state, thus increasing the voltage field distance between the record state and the V_{thi}.

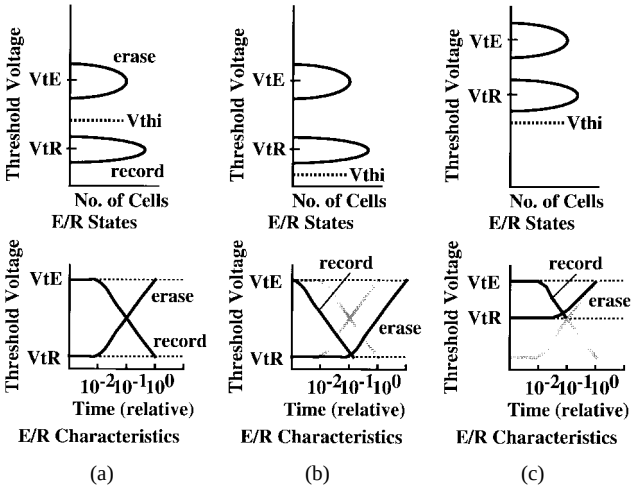


Fig. 5. Schematic cell threshold voltage distribution and erase/record (E/R) characteristics: (a) conventional, (b) proposed 1, and (c) proposed 2.

Therefore, during recording, the potential helps to accelerate the recording. During erasing, the bias voltage is always against the potential. Erasing and recording are thus asymmetrical, and recording becomes faster.

III. Operation and Performance

The schematic threshold voltage distribution and the erase and record characteristics are compared in Fig. 5.

The conventional method [Fig. 5(a)] permits symmetrical erasing and recording. The thermal equilibrium threshold voltage is set near the midpoint between the erase and record states to allow symmetrical operation with a typical time of 1 ms. This method with symmetrical block size (512 B) of erasing and recording is suitable for conventional file memory applications.

In our proposed schemes, V_{thi} is set below the threshold voltage of the record state. This is done by either keeping the same erase and record states and moving V_{thi} below the record state by the process condition [Fig. 5(b)], or by setting the threshold voltage of both the erased state (V_{tE}) and the recorded state (V_{tR}) higher than the conventional V_{thi} [Fig. 5(c)]. Recording using either of these schemes reaches the threshold voltage ten times faster than with the conventional method under same bias condition to external terminals of the memory cell because the electric field for tunneling is increased as explained above using Figs. 2 and 4.

In our first method, accurate control of the threshold voltage is essential to prevent the depletion of recorded states. That results in a large number of verify operations, each with a small shift in the threshold voltage for each bias voltage application. These additional operations reduce recording efficiency. In our second method, the threshold voltage of the record state does not need to be controlled as accurately because of its large depletion margin. This means fewer verify operations and much faster recording. The drawback of this method is its high word-line voltage for read operations. A boosted word voltage is thus needed to read the recorded state when the external supply voltage is reduced.

The simulated asymmetrical erase/record characteristics of a typical bit are shown in Fig. 6. In this simulation, the

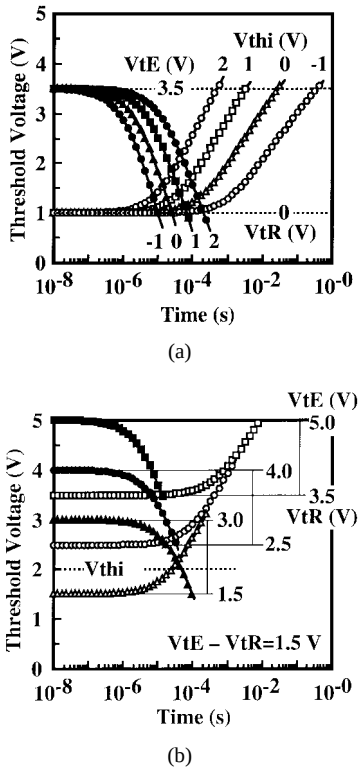


Fig. 6. Simulated asymmetrical characteristics: (a) erase/record characteristics versus V_{thi} and (b) erase/record characteristics versus V_{tE}, V_{tR}.

tunneling current was approximated by the F–N equation; and capacitive elements, which determine voltage conditions in ac analysis, were calculated considering the actual structure and shape of memory cell transistor. In erasing operation, bias voltage from word-line to substrate is 16 V, and in recording operation, bias voltage from drain to word-line is 16/12 V. Fig. 6(a) shows how the characteristics depend on V_{thi} when the threshold voltages of the erase and record states are fixed. This corresponds to changing the V_{thi} by changing the process conditions. When the V_{thi} is changed from 2 V (the conventional symmetrical condition) to zero with fixed threshold voltages of V_{tE} (3.5 V) and V_{tR} (1 V), recording becomes ten times faster, while erasing becomes 60 times slower. Fig. 6(b) shows what happens when the erase and record states are changed with a fixed V_{thi}. This corresponds to setting the threshold voltage of both the erase state and the record state higher than V_{thi}. Changing V_{tE} and V_{tR} ($V_{tE} - V_{tR} = 1.5$ V) with V_{thi} fixed at 2 V results in recording that is ten times faster with the same erase time, as at $V_{tE} = 4$ V and $V_{tW} = 2.5$ V. The resultant intrinsic recording time of the proposed scheme is 200 μs/512 B for the slowest bit, which is 20 Mb/s.

IV. High-Efficiency Recording

We propose the following circuit technologies based on asymmetrical operation to improve recording efficiency.

Because the memory cell characteristics in a chip can vary over a range of values two orders of magnitude wide, the recording time of the fastest bit is too short (2 μs) to control, while that of the slowest bit is 200 μs under asymmetrical operation [Fig. 7(a)]. Accurate control of the threshold voltage

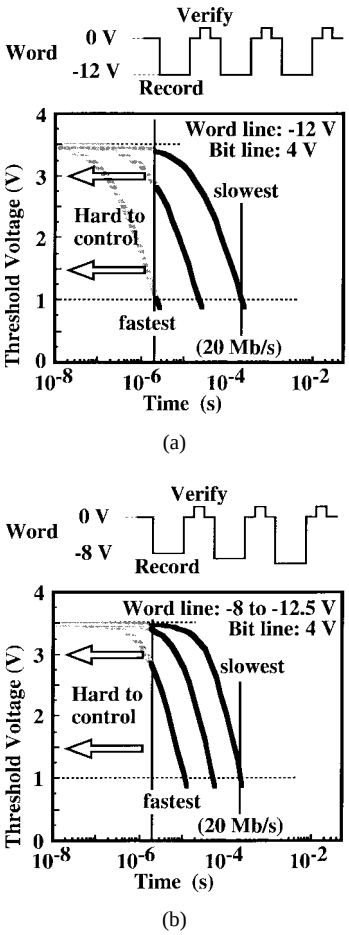


Fig. 7. Accurate control of fastest bit using variable word-voltage method: (a) constant word voltage and (b) variable word voltage.

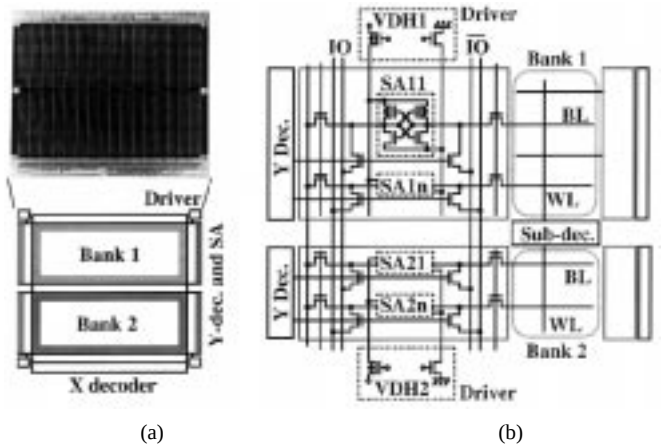


Fig. 8. Multibank Flash memory for continuous recording: (a) multibank chip and (b) circuit schematic.

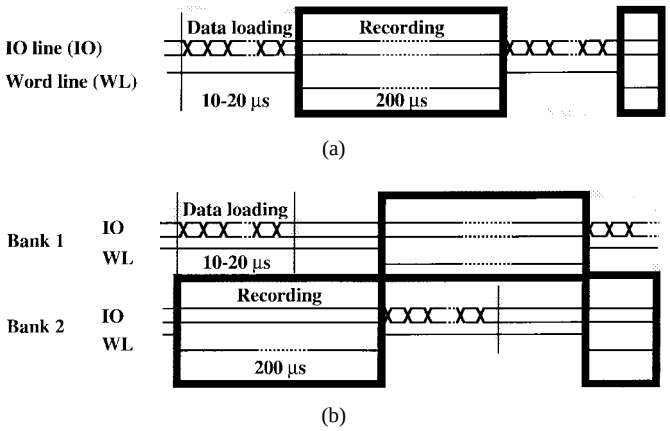


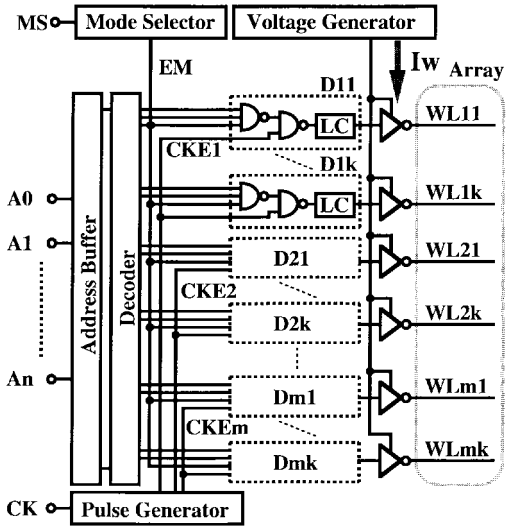
Fig. 9. Parallel recording and data loading: (a) serial operation and (b) parallel operation.

of the fastest bit requires at least 200 ns of voltage supply plus time to verify the threshold voltage if the total recording time is 2 μs. However, since the same time of 200 ns is needed to drive the word-line to a sufficient voltage, accurate threshold voltage control of the fastest bit is impossible.

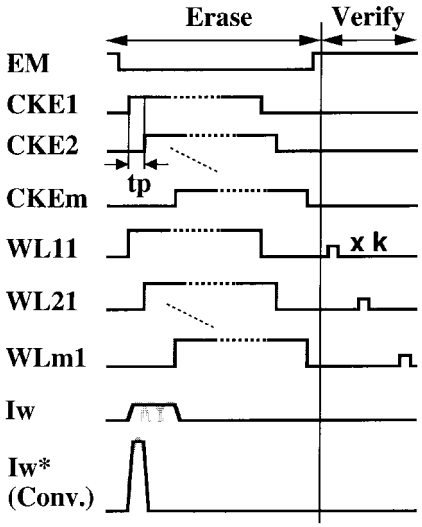
The threshold voltage of the fastest bit can be controlled accurately by using the variable word-voltage method [6]. In this scheme, the absolute value of the initial word voltage is set at 8 V (compared to 12 V for the conventional approach). Fig. 7(b) shows ideal operation, where the voltage is increased by 0.25 V every half order time. The recording time of the fastest bit is relaxed to 10 μs even though that of the slowest bit remains at 200 μs. Therefore, accurate control of the fastest bit becomes easy.

Another recording overhead is the time needed to load data into the latch circuits. Since the recording time itself is improved to 200 μs, a loading time of 10 to 25 μs is quite large because it would make the actual total recording time 225 μs. This overhead can be cut by using continuous recording with a multibank scheme. Fig. 8(a) shows a Flash memory chip with two banks of memory. The key to achieving this method is using circuit blocks to individually control the sense and latch circuits, SA11 to SA1n and SA21 to SA2n, as shown in Fig. 8(b). Two drivers supply the different high-level voltage to each sense and latch block, VDH1 to one block, VDH2 to another block. For recording in bank 1, recording voltage VDH1 is set sufficiently high for recording, while applying voltage VDH2 is set the same as that of the peripheral on the IO line so that the data is quickly sent to the circuits. For recording in bank 2, VDH1 is the applying voltage of the peripheral, and VDH2 is the recording voltage. Using this scheme, we can achieve parallel recording and data loading. Since the two drivers and two sets of sense and latch circuits are needed for 512 B operation itself, the chip area penalty of this scheme is for individual operation of them. That is, power supply lines, changeover means for recoding and data-load, and insignificant increase of control circuits. The chip size increase never exceeds 0.5% of the conventional. This scheme is simple compared to the byte programming for NOR-type cell [7]. In NOR-type parallel operation, the programming algorithm is complicated because there needs repeating a) addressing one byte in the page buffer, b) transferring to the array, and c) supplying the bias voltage and verification. In NOR-type memory, operation of data-load to another page buffer must be controlled parallel to these series of operations. On the contrary, our chip needs only to be supplied the bias voltage and verification. Necessary components are individually controlled sense and latch circuits explained above.

The conventional method and the proposed multibank method are compared in Fig. 9. Conventionally, data loading



(a)



(b)

Fig. 10. High-speed erasing using multiphase word-driving scheme: (a) circuits schematic and (b) timing.

and recording operate serially. Although the recording time itself is improved to 200 μs by using the proposed asymmetrical operation, the loading time of 10–25 μs is still quite large. In parallel operation using two banks, while data is being loaded into bank 1, recording is being performed in bank 2. Then, while recording is being performed in bank 1, the next data is being loaded into bank 2. With this parallel operation, the data-loading time becomes insignificant, so continuous recording using two banks can cut overhead compared to serial operation and 200-μs recording can be achieved.

V. High-Speed Erasing

Although recording speed is improved by an order of ten due to asymmetrical and parallel operations, the asymmetrical operation makes erasing 60 times slower. High-speed erasing is thus needed to shorten the waiting time it takes to completely erase a whole chip (or card) before recording. For simultaneously erasing and recording, the erasing speed must be the same as the improved recording speed.

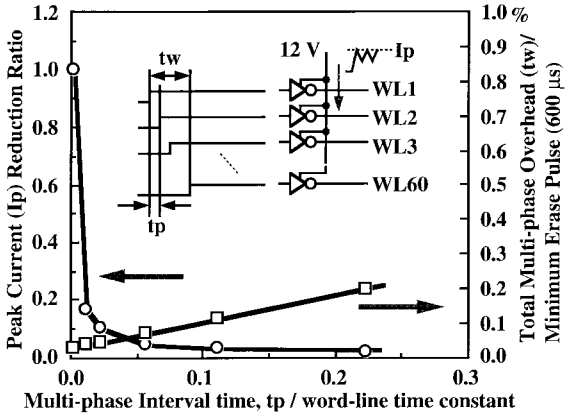


Fig. 11. Peak current in multiphase word driving.

Large-scale parallel erasing improves the erasing speed by one order of magnitude. It is reasonable to introduce a large erasing block because 256 kbytes are needed when the camera's erasing unit is 0.1 s of recording time on average, which is a sufficiently small for personal use. Of course, we can choose any size erasing block in whole chip erase before recording. However, it is impossible to simply raise the number of parallel operations because the capability of the current supply at high voltages, such as 10 to 15 V, is small when the whole internal voltage-generator circuits occupy only 3%, the value of which is the maximum for practical design, of the chip. In this situation, only ten word lines can be driven simultaneously. To drive more word lines under overload conditions does not mean having to reach the target voltage quickly. The target voltage is not guaranteed because the operation of the voltage-regulating circuit is unstable.

To overcome this difficulty, we introduce a multiphase word-driving scheme. By shifting the starting point of plural word line driving, large-scale erasing is made practical. When one word line reaches the target voltage, driving of the next word line is started. The overhead for this multiphase operation is small enough to control the threshold voltage because the time needed to reach the threshold voltage of the erase state increases by 60 due to using the asymmetrical operation shown in Fig. 6(a). Also, since the duration of the peak current is small when a MOS transistor is used to charge the load, the next word line can start before the end of the first word line.

The circuit schematic for this operation and the timing are shown in Fig. 10. During the erase mode, when the voltage of EM is low, the word line is controlled by CKE1 to CKEm instead of by the address-decoding signal. In this figure, each CKE1 – CKEm selects k word lines. Here, CKE1 first selects word lines of WL11 to WL1k and current I_w flows from the internal voltage generator. After an interval of t_p, CKE2 changes to a high level, and the corresponding word lines of WL21 – WL2k are loaded with the same current I_w. Because one signal can typically select ten word lines, a 60-phase operation can select 600 word lines under a small current from the internal generator.

The simulated peak-current reduction in a 60-phase word scheme is shown in Fig. 11. The horizontal axis shows the multiphase shift interval time of t_p normalized by the word-

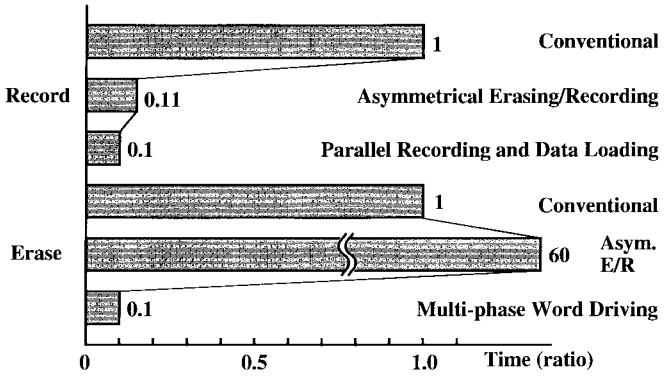


Fig. 12. Effect of high-speed erasing and recording.

line time constant. The left vertical axis shows the peak current reduction ratio, and the right vertical axis shows the total multiphase overhead time normalized by the minimum erase-pulse width. This simulated data shows that if t_p is set to 10% of the time constant of the word line, the peak current will be reduced to less than 10% of the simultaneous driving current. The time overhead is only 0.1% of the minimum erase time. The verify operation follows the erase-voltage supply. The time overhead per 600-word-line verification is only 1% of the total erase time, which is enough to ensure accurate control of the threshold voltage.

The effects of high-speed recording and erasing are summarized in Fig. 12. Recording is improved by about one order of magnitude by using asymmetrical operation. Parallel recording and data loading reduce the overhead. Therefore, the recording rate is improved to 20 Mb/s.

Erasing is also improved. Although asymmetrical operation makes erasing 60 times slower, the multiphase word-driving scheme enables large-scale parallel erasing. The erasing speed is thereby increased to that for recording.

VI. Disturbances and Retention

In Flash memory, data is stored in the memory cell whether the threshold voltage of the memory cell is higher than V_{read} (erase state) or not (record state). In actual practice, a sufficient voltage difference (cell window) is needed between the two states because of the sensing characteristics and because of the voltage margin needed against changes in the threshold voltage in the read disturbance and retention modes, as shown in Fig. 13. During read operations, a voltage of V_{read} is applied to the control gate. However, this voltage causes electron injection into the floating gate of the memory cell. When the accumulated read time increases due to repeated read operations, the threshold voltage of the record state is increased (read disturbance mode). This reduces the cell window. During shutdown mode, the floating gate has a potential due to its stored charges. Therefore, electrons are ejected from the floating gate, and the threshold voltage of the memory cell is decreased to V_{thi} (retention mode). The cell window is also narrowed.

Here, we assume the asymmetrical scheme is accomplished by setting the threshold voltage of both the erase state (V_{tE}) and the record state (V_{tR}) higher than the conventional V_{thi},

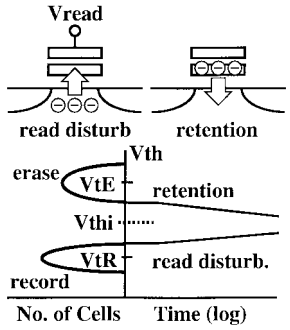


Fig. 13. Read disturbance and retention.

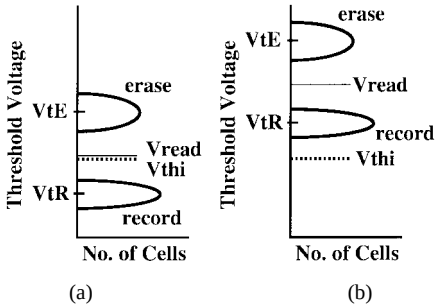


Fig. 14. Voltage relation of conventional and proposed asymmetrical schemes: (a) conventional and (b) proposed asymmetical.

as shown in Fig. 14. Since the $V_{\text{read}} - V_{tR}$ is determined by the sensing characteristics, $V_{\text{read}} - V_{tR}$ is the same in both schemes.

The leakage current due to read disturbances or retention is approximately expressed (F–N approximation) as

$$I_{\text{leak}} = A \cdot E_{ox}^2 \cdot \exp\left(-\frac{B}{E_{ox}}\right) \tag{1}$$

where E_{ox} is the electrical field through the dielectric film during read disturbances or retention, and A and B are constants determined by the physical characteristic of the film.

E_{ox} during reading (read disturbance) is expressed as

$$E_{ox_{\text{read disturb}}} = C \cdot (V_{thi} + V_{\text{read}} - V_{tR}) \tag{2}$$

where C is the constant determined by the cell structure.

E_{ox} during shutdown (retention) is expressed as

$$E_{ox_{\text{retention}}} = C \cdot (V_{tE} - V_{thi}). \tag{3}$$

By (1) and (2), the read disturbances are the same for the conventional and proposed schemes because V_{thi} was set the same for both the schemes, and $V_{\text{read}} - V_{tR}$ was also set equal by the sensing characteristics. However, the retention time is worse in the proposed scheme, because $V_{tE}-V_{thi}$ in the proposed scheme is larger than in the conventional scheme. For example, in Fig. 6(b), when the recording time improves by one order of magnitude with the same V_{thi} (2 V), the V_{tE} in the proposed scheme is 4 V, while that in the conventional scheme is 3 V. The $V_{tE}-V_{thi}$ in the conventional scheme is 1 V, and that in the proposed one is 2 V. This causes a large leakage current in the shutdown mode based on (1) and (3). Generally, a 1-V difference increases the leakage current by

one order of magnitude. This leakage current increases as the erase and record cycle is repeated.

However, because images recorded in a Flash movie camera are likely to be downloaded to a permanent file within a month, the total number of times that each memory card will be used is probably less than 10^4 (average 60 min use per week over ten years), as shown in Table I. This means the retention time and duration of an erase-and-record cycle are reduced by two orders of magnitude. Therefore, the retention problem with the proposed scheme is less than or the same as that with the conventional scheme.

In movie camera application, the read cycle itself is also drastically decreased. Reading occurs during image checking and downloading. Checking before downloading will not exceed a thousand scans per 512-B sector: it is ordinarily within a hundred, with a virtual maximum of a thousand. In conventional file applications, ten-year continuous reading must be guaranteed. This means the reading cycle is reduced by ten orders of magnitude.

VII. Conclusion

An asymmetrical recording and erasing operation of Flash memory is proposed. Setting V_{thi} below the recording state, along with accurate control of the fastest bit and continuous recording using two banks, increases the recording speed to ten times that of the conventional method. The erasing speed is also increased ten times by using large-scale parallel operation that is made practical by the multiphase word-driving scheme. With these circuit technologies, 20-Mb/s erase/record Flash memories are attainable for use in future personal HDTV movie cameras.

Acknowledgment

The authors thank S. Shimizu, K. Miyazawa, and K. Seki for their steady encouragement. They would also like to thank K. Furusawa, H. Kotani, H. Kume, M. Kato, and T. Kobayashi for their suggestions.

References

[1] T. Kawahara *et al.*, "20 Mb/s erase/record Flash memory by asymmetric operation," in *1996 Symp. VLSI Circuits, Dig. Tech. Papers*, June 1996, pp. 174–175.

[2] H. Miwa *et al.*, "A 140 mm^2 64Mb and Flash memory with 0.4 μm technology," in *1996 ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 34–35.

[3] M. Ohkawa *et al.*, "A 98 mm^2 3.3V 64Mb Flash memory with FN-NOR type 4-level cell," in *1996 ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 36–37.

[4] T.-S. Jung *et al.*, "A 3.3V 128Mb multi-level NAND Flash memory for mass storage applications," in *1996 ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 32–33.

[5] T. Kawahara *et al.*, "Bit-line clamped sensing multiplex and accurate high-voltage generator for 0.25 μm Flash memories," in *1996 ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 38–39.

[6] T. Kawahara *et al.*, "High reliability electron-ejection method for high density Flash memory," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1554–1562, Dec. 1995.

[7] A. Baker *et al.*, "A 3.3V 16Mb Flash memory with advanced write automation," in *1994 ISSCC Dig. Tech. Papers*, Feb. 1994, pp. 146–147.

Takayuki Kawahara (M'91) was born in Kumamoto, Japan, on June 10, 1960. He received the B.S. and M.S. degrees in physics and the Ph.D. degree in electronic engineering from Kyusyu University, Fukuoka, Japan, in 1983, 1985, and 1993, respectively.

In 1985, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan. From 1985 to 1991, he was engaged in the research and development of BiCMOS DRAM's. Since 1991, he has been engaged in the research and development of circuit technologies for Gb-scale DRAM's, including dynamic termination, subthreshold-current reduction, and charge recycle schemes. Currently, his research interests are on the large scale Flash memory and its applications.

Dr. Kawahara is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.

Yusuke Jyouno was born in Tokyo, Japan, on April 5, 1968. He received the B.S. and M.S. degrees in physics from the Tokyo Institute of Technology, Tokyo, Japan, in 1992 and 1994, respectively.

In 1994, he joined the Semiconductor and Integrated Circuits Division, Hitachi, Ltd., Tokyo, Japan. He has been engaged in the development of the Flash memory.

Syun-ichi Saeki was born in Tokyo, Japan, on May 18, 1963. He received the B.S. degree in electrical engineering from Tokai University, Tokyo, Japan, in 1986.

In 1986, he joined Hitachi Device Engineering Co., Ltd., Chiba, Japan. Since 1986, he has been engaged in the research and development of Flash memory circuit.

Mr. Saeki is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.

Naoki Miyamoto was born in Hiroshima, Japan, on March 25, 1958. He received the B.S. degree in electrical engineering from Nihon University, Tokyo, Japan, in 1981.

In 1981, he joined Hitachi Device Engineering Co., Ltd., Chiba, Japan. Since 1987, he has been engaged in the research and development of Flash memory device and circuit.

Katsutaka Kimura (M'90) was born in Osaka, Japan, on January 26, 1956. He received the B.S. and M.S. degrees in electronic engineering from Kyoto University, Kyoto, Japan, in 1978 and 1980, respectively.

Since he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, in 1980, he has been engaged in the research and development of MOS memories, such as DRAM's, BORAM's, and Flash memories, as well as solid-state image sensors.

Mr. Kimura is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information, and Communications Engineers of Japan.