Available online at www.sciencedirect.com
SCIENCE DIRECT®
Sensors and Actuators B 113 (2006) 555–562
SENSORS AND ACTUATORS B CHEMICAL
www.elsevier.com/locate/snb

ISFET performance enhancement by using the improved circuit techniques

Wen-Yaw Chung [a,*], Chung-Huang Yang [a,b], Dorota G. Pijanowska [c], Piotr B. Grabiec [d], Wladyslaw Torbicz [c]

[a] *Department of Electronic Engineering, Chung Yuan Christian University, 200 Chung Pei Road, Chung Li, Taiwan 32023, ROC*
[b] *Department of Electronic Engineering, Vanung University of Science and Technology, 1 Van-Nung Road, Chung-Li, Taiwan 32061, ROC*
[c] *Institute of Biocybernetics and Biomedical Engineering, Polish Academy of Sciences, ul. Trojdena 4, 02-109 Warsaw, Poland*
[d] *Department of Silicon Microsystem and Nanostructure Technology, Institute of Electron Technology, Al. Lotnikow 32/46, 02-668 Warsaw, Poland*

Received 11 April 2005; received in revised form 5 June 2005; accepted 13 June 2005
Available online 2 August 2005

Abstract

An approach to enhance accuracy of the output signal obtained from ISFET interface electronics due to the body effect is proposed. Based on an MOS drawing the same drain current as the ISFET, the scheme allows reduction of influence of body effect. The presented readout interface improves the accuracy of pH measurements, while maintaining operation at constant drain-source voltage and current condition. Using only one ISFET with a differential output configuration, we obtained temperature-dependency and long-term drift as well as common noise compensation. The proposed technique is simple and has a universal use for different ISFETs. In addition, a voltage-controlled dc offset error compensation circuit modulates the extracted signal to the desired dc level for the A/D converter for each sensor. Simulation and experimental results show a great effect on monolithic ISFET integration in CMOS technology.

Keywords: ISFET; Body-effect reduction; Temperature-dependency; Long-term drift; CMOS

1. Introduction

The ion sensitive field effect transistor (ISFET), invented in 1970 by Bergveld [1], is a solid-state device that combines the chemically sensitive membrane with the MOS type field-effect transistor. In its extensive study over the past 30 years [2–4], ISFET has been characterized and measured [5,6], indicating drawbacks related to: thermal-dependency, long-term drift and hysteresis. These factors limit the accuracy of ISFET-based measurements systems, especially for biomedical and analytical applications. Another important parameter, the slope of characteristic (sensitivity), also characterize an ISFET.

Due to the basic characteristics of ISFET, the potentiometric method has been used to measure the change in pH through a corresponding shift in the device threshold voltage. In order to extract the relevant signal from the electrical behavior of the sensor, it is necessary for the ISFET to be accompanied by an analog readout interface [7–12]. Recent works have projected to integrate ISFET and the interface electronics on the same chip [13–17]. Due to the low drift and high mobility properties of carriers, n-channel ISFETs are generally used. In most of today's CMOS processes, the NMOS device is fabricated into a p-type substrate that is globally and constantly grounded by connection to the most negative supply in the system. Thus, the above-mentioned interface circuits suffer from the problem that the substrate potential greatly influences the device characteristics in ISFET-based integrations. Previous researches [4,5,7,12] show that the constant voltage and constant current (CVCC) biasing technique has been the most widely used method for ISFET sensing. In 2004, Morgenshtein et al. presented a novel technique, which allows body effect elimination of readout interface in CMOS

* Corresponding author. Tel.: +886 3 2654615; fax: +886 3 2654699.
E-mail address: eldanny@cycu.edu.tw (W.-Y. Chung).

0925-4005/$ – see front matter © 2005 Elsevier B.V. All rights reserved.
doi:10.1016/j.snb.2005.06.018

ISFET-based microsystems [18]. However, in order to keep the constant potential of reference electrode, the direct complementary ISFET/MOSFET pair (CIMP) circuit with gate feedback is not suitable for sensor array readout applications. In addition, indirect CIMP circuit with gate feedback can only have a constant V_{DS} bias but varying drain current.

Furthermore, many electronic circuits have been developed to compensate for the thermal-dependence and long-term drift of ISFET. In 1987, Wang et al. described a zero temperature coefficient adjustment and a temperature coefficient (TCF) compensation method to reduce the temperature coefficient of a pH-ISFET [6]. This 'zero TCF adjustment of the output voltage' would be suitable in the case of real time control or measurements where the pH value of a solution is within a certain region. However, it is necessary to find the drain current required for each ISFET individually. In 1999, Palan et al. used two identical readout circuits with two ISFETs of different gate materials (Si_3N_4 and Al_2O_3), so that these ISFETs of different sensitivity could compensate for temperature-dependency and long-term drift for biomedical applications [8]. However, in this case there is no full verification of the proposed differential configuration because that the circuit has not been fully tested during pH measurements. In 2003, Casans et al. reported a novel voltage-controlled conditioning circuit applied to the ISFETs temporary drift and thermal-dependency [19] and then in 2004 published a novel electronic compensation in ISFET drawbacks minimization [20]. This compensation method required the expense of extra electronics or miscellaneous numerical calculations.

This paper proposes a simple approach enhancing accuracy of measurements by ISFET by using a body-effect reduction technique, while maintaining constant drain-source voltage and current. With a differential configuration of amplifier circuit, this design technique generates an output signal independent of temperature and long-term drift. In addition, a voltage-controlled dc offset error compensation circuit modulates the extracted signal to the desired dc level for the A/D converter for each sensor. Simulation and experimental results demonstrate the effectiveness of the instrumentation system for monolithic ISFET integration in CMOS technology.

2. Body effect in ISFETs

An ISFET structure is similar to an MOS transistor, except that it uses an exposed gate insulator or membrane to measure a selected ion concentration in an electrolyte, e.g. changes in the pH of the electrolyte produce variations on the threshold voltage due to ionic activity at the electrolyte–insulator interface. Hence, the measurement of the threshold voltage of the ISFET directly changes with the pH concentration of the electrolyte. The device operation of an ISFET can be deduced from both the pH-dependent characteristic and the MOSFET behavior. For example, consider the circuit in Fig. 1a, first ignoring body effect. We note that as V_{in} varies, V_{out} closely

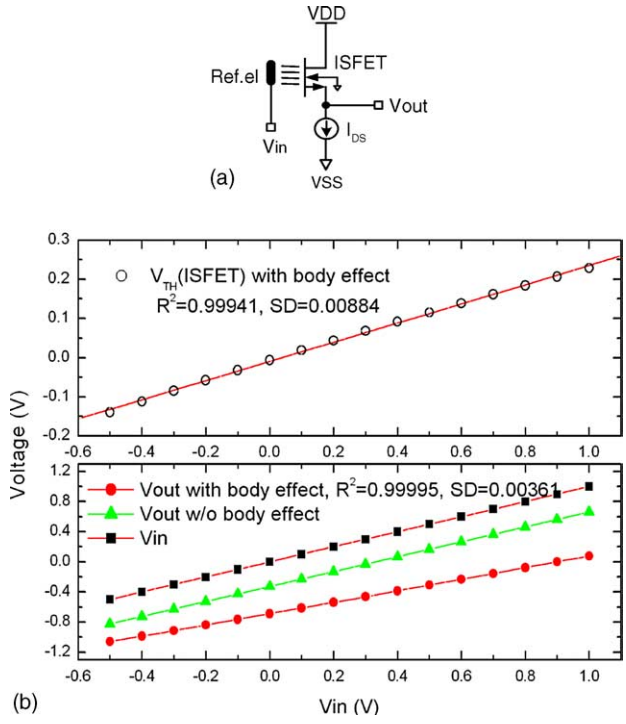

Fig. 1. (a) A n-channel depletion ISFET; (b) input and output voltages with and without (w/o) body effect.

follows the input because the drain current remains equal to I_{DS} (Fig. 1b). In fact, the ISFET devices are commonly biased in the triode region (i.e. $V_{DS} \leq V_{GS} - V_T$), where the drain current I_{DS} are expressed as follows:

$$I_{DS} = K_p \left[(V_{GS} - V_{TH}^*) - \frac{V_{DS}}{2} \right] V_{DS}$$
$$= K_p \left[(V_{in} - V_{out} - V_{TH}^*) - \frac{V_{DS}}{2} \right] V_{DS} \quad (1)$$

where K_p is the device transconductance factor, V_{DS} is a drain-source voltage and $V_{TH}^* = V_{TH} + EPH$ denotes the ISFET's threshold voltage resulting from the threshold voltage (V_{TH}) of FET and EPH is the interface potential between sensing membrane and buffer solution.

Suppose the substrate is connected to the most negative supply and body effect is significant. Then, as V_{in} and hence V_{out} become more positive, the potential difference between the source and the bulk increases, raising the value of V_{TH} as shown in Fig. 1b. Eq. (1), therefore, implies that $V_{in} - V_{out}$ must increase so as to maintain I_{DS} constant. Thus, a non-zero V_{SB} value contributes a parasitic change in V_{TH}^* that is not due to the change of ion concentration.

Fig. 2a presents an n-channel p-well depletion-mode Si_3N_4-gate ISFET sensor (W/L = 600 μm/15 μm) fabricated by the Institute of Electron Technology, Poland. Based on [21], an HSPICE-compatible macromodel has been developed to fit our depletion-mode ISFET devices. This model shown in Fig. 2b considered the ISFET as two stages: an electronic stage and an electrochemical stage, where Ref. el,

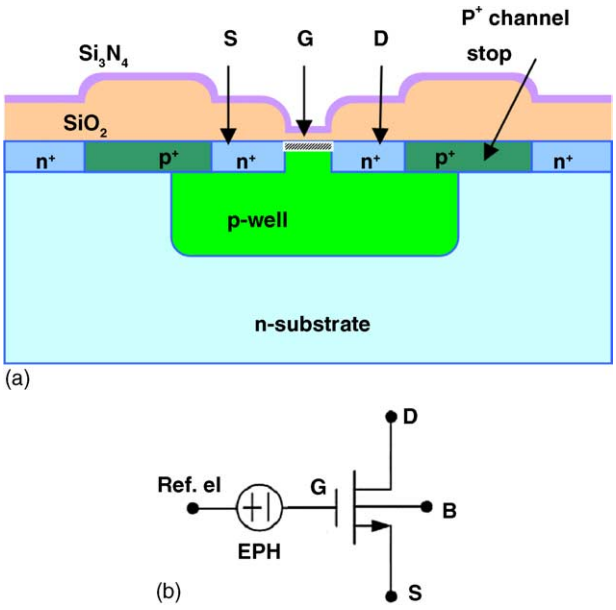

Fig. 2. (a) ISFET structure layout; (b) equivalent sub-circuit block of the ISFET macro-model.

D, S, and B stand for the reference electrode, the drain, the source, and the bulk connections, respectively.

3. Sensor interface design

3.1. Body-effect reduction technique

Fig. 3 shows the circuit diagram of the floating source bridge-type readout interface [12]. The circuit adopts a differential amplifying circuit to couple the ISFET sensor to operate in the CVCC mode, thereby detecting the accurate analyte concentration. The differential amplifying circuit constitutes a floating reference voltage drop $|V_{\text{ref}}|$ between nodes 1 and S, which are both with respect to the ground. Thus, nodes 1 and S will be tracking each other under any condition and yielding Eq. (2):

$$V(1) - V(S) = |V_{\text{ref}}| \tag{2}$$

The bridge-type ISFET interface circuit responds to the ion concentration of the solution due to the feedback loop operation of the amplifier and constant value floating reference voltage supplied. In this case, the drain-source voltage will be given by the following equation:

$$V_{\text{DS,MISFET}} = \frac{R_2}{R_1 + R_2} |V_{\text{ref}}| \tag{3}$$

and hence the constant gate-source voltage of transistor M300 constitutes a drain-source current:

$$I_{\text{DS,MISFET}} = I_{\text{DS,M300}} \tag{4}$$

thereby biases the ISFET in CVCC situation.

Since the S terminal is not constantly biased, it varies with different ion concentration. For monolithic ISFET integration, the extracted signal from S terminal presents a parasitic change due to non-zero V_{SB} term. Thus, we consider that two MOSFETs (MISFET and M313) carry equal drain currents under the influence of body effect [22]. To simplify the analysis, we employ MOSFETs in the saturation region. Hence,

$$\begin{aligned} I_{\text{DS,MISFET}} = I_{\text{DS,M313}} &\Rightarrow K_{\text{p}}(V_{\text{GS,MISFET}} - V_{\text{TH,MISFET}})^2 \\ &= K_{\text{p}}(V_{\text{GS,M313}} - V_{\text{TH,M313}})^2 \end{aligned} \tag{5}$$

Assume that both MISFET and M313 are matched in the same p-type substrate, yielding a relation:

$$\begin{aligned} &V_{\text{GS,MISFET}} - V_{\text{GS,M313}} = V_{\text{TH,MISFET}} - V_{\text{TH,M313}} \\ &\quad \Rightarrow -\text{EPH} - V_{\text{out}}S - (V_{\text{out}}T - V_{\text{out}}S) \\ &= V_{\text{TH0,MISFET}} + \gamma(\sqrt{2\phi_{\text{f}} + V_{\text{SB,MISFET}}} - \sqrt{2\phi_{\text{f}}}) \\ &\quad -[V_{\text{TH0,M313}} + \gamma(\sqrt{2\phi_{\text{f}} + V_{\text{SB,M313}}} - \sqrt{2\phi_{\text{f}}})] \\ &\quad \Rightarrow V_{\text{out}}T = -\text{EPH} \end{aligned} \tag{6}$$

The EPH modeled the potential of electrolyte-insulator interface. The extracted signal $V_{\text{out}}T$ is independent of the body effect.

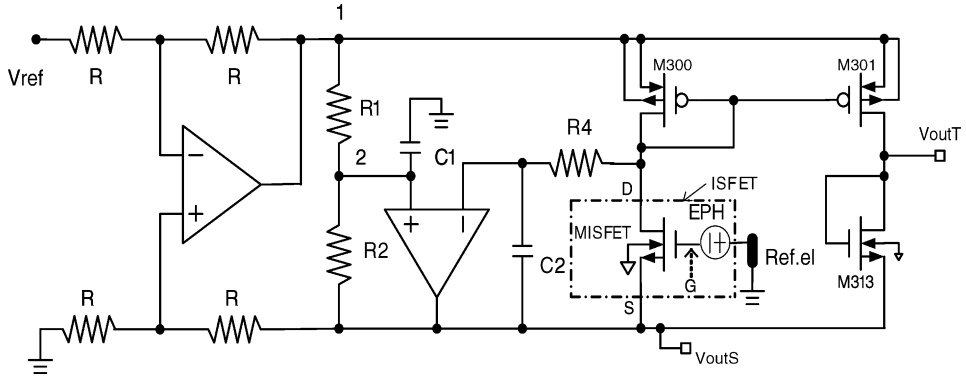

Fig. 3. Diagram of the bridge-type body-effect reduction readout interface.

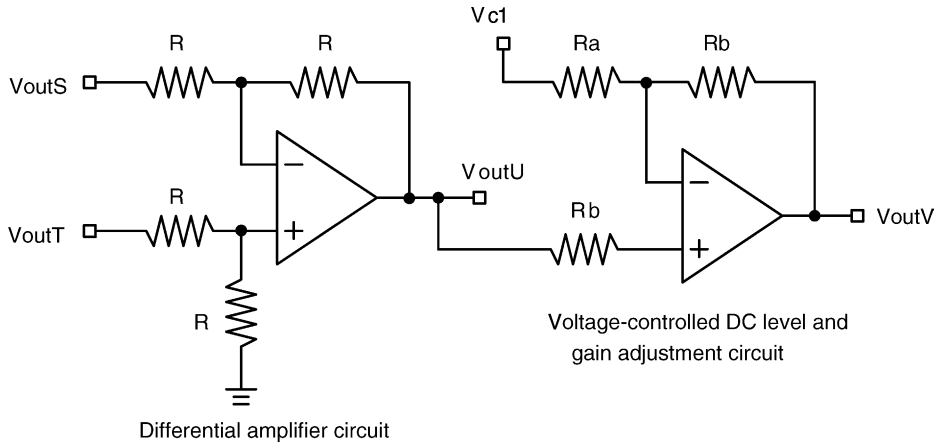

Fig. 4. Circuit for ISFET performance enhancement.

3.2. ISFET performance enhancement circuit

In general, single ISFET interface circuits do not offer any degree of compensation for temperature-dependency or long-term drift. Therefore, several ISFET differential configurations with different sensitivities have been studied [8].

In this study, only one ISFET accompanies a performance enhancement circuit is shown in Fig. 4. Since $V_{out}S$ and $V_{out}T$ carry equal instability quantities on temperature-dependency, long-term drift as well as common noise. With the differential amplifier circuit presented in Fig. 4, a perfectly mismatch between resistance R is supposed and an infinite CMRR is also assumed by the OP amplifier, then, the output signal, $V_{out}U$, given by Eq. (7) is not affected by temperature, long-term drift or common noise:

$$V_{out}U = V_{out}T - V_{out}S \tag{7}$$

Thus, the temperature-dependency, long-term drift and common noise can be effectively compensated with the proposed circuit.

The second sub-circuit shown in Fig. 4 implements a voltage-controlled dc offset error compensation and gain adjustment is determined by

$$V_{out}V = \left(1 + \frac{R_b}{R_a}\right) V_{out}U - \frac{R_b}{R_a} V_{c1} \tag{8}$$

where the first term generates a thermal and long-term drift-independent output signal, while the second term modulates the extracted signal to the desired dc level for the A/D converter for each sensor.

Simulation plots of the output signal of the proposed body-effect reduction circuit are shown in Fig. 5. The depletion-mode Si_3N_4-gate ISFET sensor was emulated by an HSPICE-compatible macro-model. For the ISFET operating point of a drain-source voltage of 0.5 V and a drain current of 100 μA, with the ISFET bulk connected to the most negative voltage, dependence levels of −41.44, −50.12 and −8.67 mV/pH have been obtained for terminals $V_{out}S$, $V_{out}T$ and $V_{out}U$ (curves (a), (b) and (c) in Fig. 5), respectively. The obtained improvement of pH sensitivity (S) for $V_{out}T$, reflects independence of the output signal of the body effect. The temperature and long-term drift compensated signal $V_{out}U$ (curve (c)), is then modulated to the desired dc level with $V_{c1} = 0.9$ V and gained to obtain signal $V_{out}V$ (curve (d)) by the voltage dc level and gain adjustment circuit shown in Fig. 4.

Fig. 6 shows the simulation results of ISFET interfacial output voltage in the pH range of 2–12 for the temperature range of 5–35 °C with increment steps of 10 °C. The corresponding temperature coefficient (TCF), before ($V_{out}S$) and after ($V_{out}U$) compensation, is −4.47 and −0.75 mV/°C, respectively. Then it has been shown that by using the proposed techniques one may obtain reduced temperature-dependence.

To investigate the improvements of the long-term drift using the proposed circuitry, the simulation tests were done using an ISFET macromodel. Fig. 7 portrays the ISFET long-term drift simulation results. The ISFET's time drift coefficients in buffer solution of pH 6 before and after com-

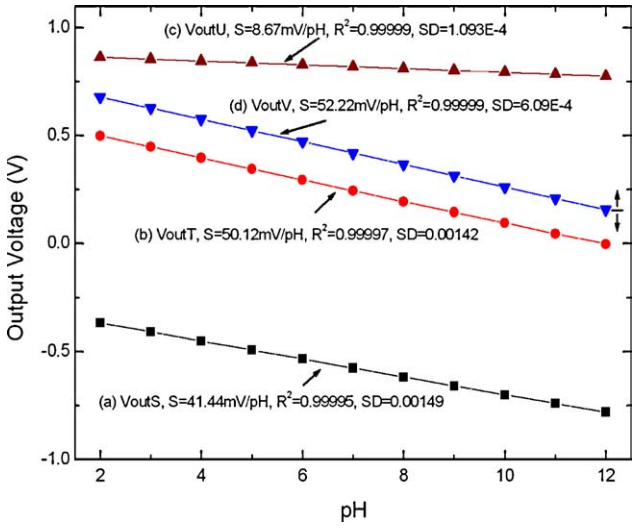

Fig. 5. Simulation plots of the output signal of the proposed body-effect reduction circuit for pH sweep.

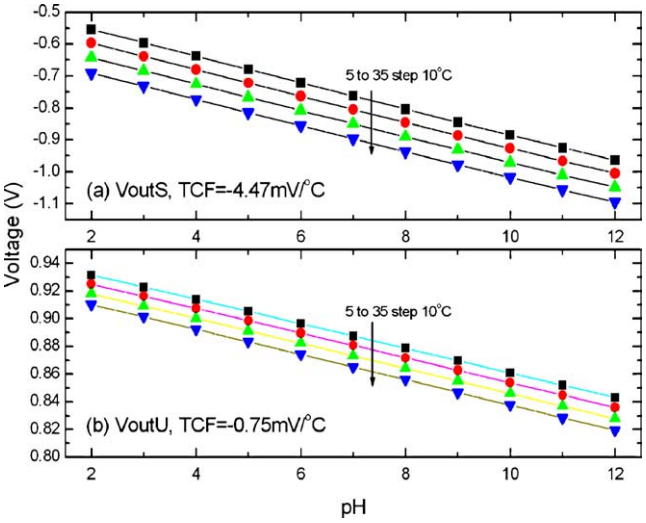

Fig. 6. Simulation of ISFET interfacial voltage in the pH range of 2–12 for the temperature range of 5–35 °C.

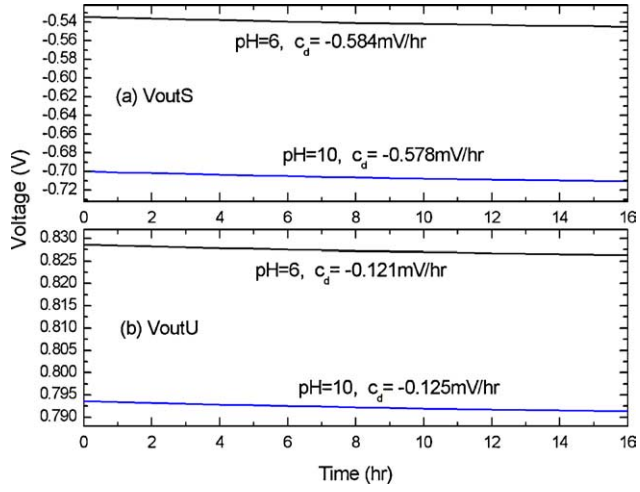

Fig. 7. Long-term drift simulation of ISFET interfacial voltage in a buffer solution of pH 6.

pensation are −0.584 and −0.121 mV/h, respectively. Also, the time drift coefficients of −0.578 and −0.125 mV/h on $V_{out}S$ and $V_{out}U$ at pH 10. The designed circuitry also reduces the ISFET time drift coefficient. A chip microphotography of the total electronics fabricated by a TSMC 0.35 μm double-poly and quadruple-metal CMOS process is shown in Fig. 8. The core die size is around 9.1 mm × 9.1 mm.

4. Results and discussion

In the following experiments, the most negative supply (VSS = −1.65 V) is applied to the ISFET bulk connection. A Si_3N_4-type depletion-mode ISFET (W/L = 600 μm/15 μm) is adopted. The ISFET is biased on a drain-source voltage of 0.45 V and a drain current of 100 μA. The experiments used standard buffer solutions at pH range from 2 to 12 purchased

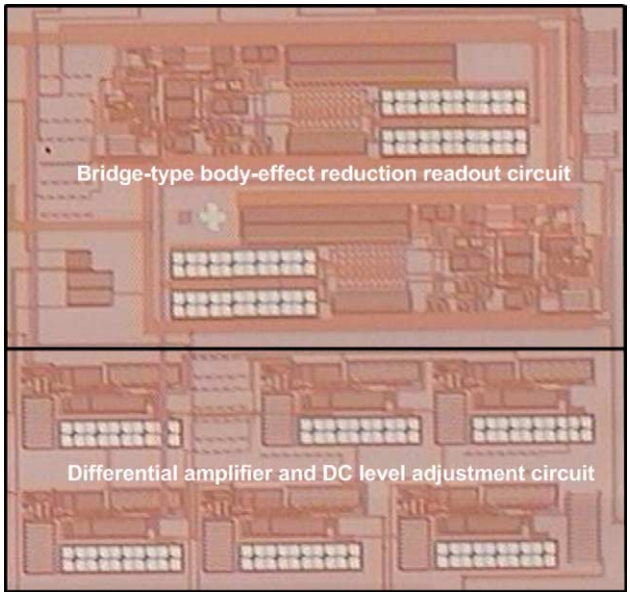

Fig. 8. Chip microphotography of the total body-effect reduction and performance enhancement circuitry.

from Riedel-de Haen (Germany). The buffer solution used for drift and temperature effect investigation was of pH 6.01, 9.95 at 25 °C (called pH 6, 10).

4.1. ISFET I–V measurement

In order to investigate the accuracy of the proposed techniques, the transient characteristics I_D–V_{GS} collected for a depletion-mode Si_3N_4-type ISFET by using HP4155B semiconductor parameter analyzer at room temperature have been taken (shown in Fig. 9). The pH sensitivity of the ISFET was around 50 mV/pH.

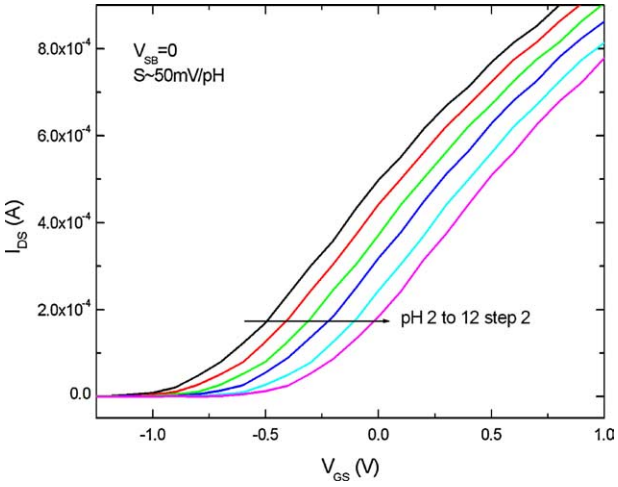

Fig. 9. I_{DS} vs. V_{GS} characteristics of an ISFET operating in the proposed circuit for buffer solutions of different pH and for $V_{SB} = 0$.

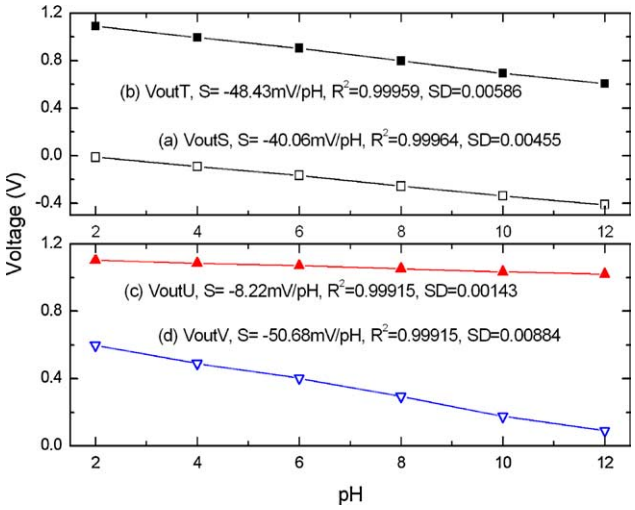

Fig. 10. pH response of ISFET operating in the body-effect reduction circuit with the ISFET bulk connected to VSS.

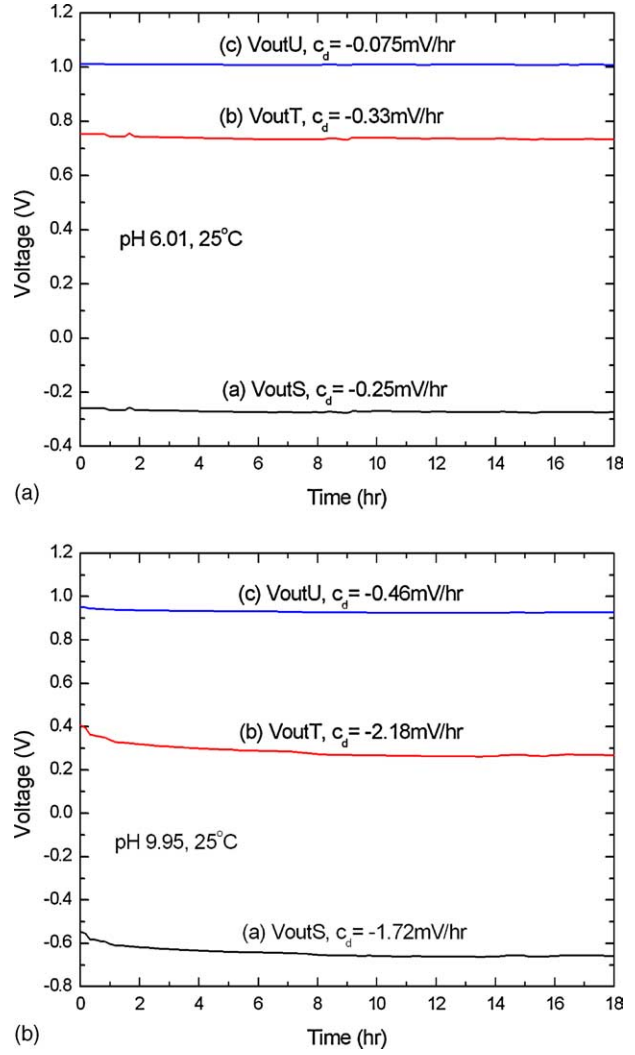

Fig. 11. Time-dependency response with and without differential compensation methods.

4.2. pH sensitivity test

The curves in Fig. 10 show dependence of potentials for four terminals in the body-effect reduction circuit (see Fig. 4) over pH range of 2–12: $V_{out}S$, $V_{out}T$, $V_{out}U$ and $V_{out}V$. The ISFET bulk was connected to the most negative supply (VSS = −1.65 V). The calculated slopes for the curves (a, b, c and d) are −40.06, −48.43, −8.22 and −50.68 mV/pH for terminals $V_{out}S$, $V_{out}T$, $V_{out}U$ and $V_{out}V$, respectively. The increase of slope for curve (b) in respect to curve (a) demonstrates an improvement resulting from the reduction of influence of body effect. The presented experimental data correlates well with the simulation data presented in Fig. 5.

4.3. Long-term drift test

The drift rates were evaluated after initial time of stabilization of ISFET as a linear change of V_{GS} per time unit, and the drift rate is called the drift coefficient, c_d (mV/h). Fig. 11 shows the time response of ISFET without and with applied compensation. The test was performed for an 18 h time period for the ISFET operating in a standard buffer solution at pH 6 and 10 at a controlled temperature of 25 ± 0.5 °C. The c_d values were calculated for experimental data after 4 h of conditioning. The calculated values of c_d of potentials measured at terminals $V_{out}S$, $V_{out}T$ and $V_{out}U$ for pH 6 and 10 are −0.25, −0.33, −0.075 and −1.72, −2.18, −0.46 mV/h, respectively. With the proposed techniques, long-term drift is reduced considerably, which is consistent with the simulated data described above (Section 3.2).

4.4. Temperature-dependency test

The voltages measured at terminals $V_{out}S$ and $V_{out}T$ without temperature compensation and the voltage measured at

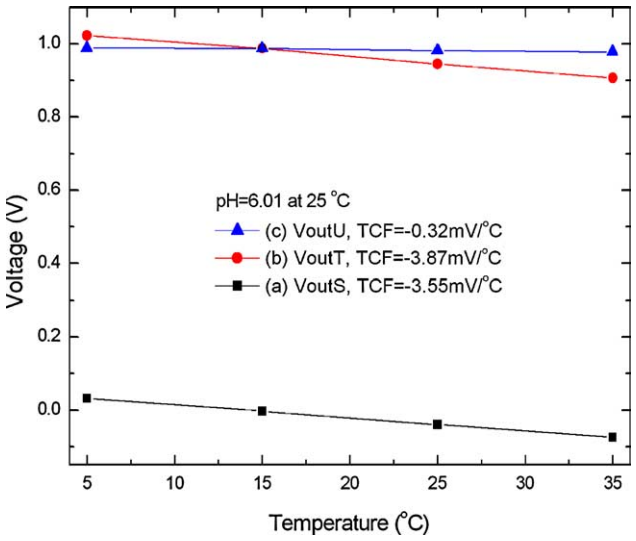

Fig. 12. Output voltage vs. temperature for ISFETs operated by a circuit with/without compensation.

terminal $V_{out}U$ with temperature compensation have been compared (Fig. 12). In this experiment, the ISFET was operating in a buffer solution at pH 6 with temperature varied in from 5 to 35 °C. The corresponding temperature coefficients (TCF) calculated for the two terminals were the following: −3.55, and −3.87 mV/°C for $V_{out}S$, $V_{out}T$, respectively. The resulting TCF for $V_{out}U$ was −0.32 mV/°C, which indicates that the temperature-dependency has been reduced to a certain extent.

5. Conclusions

A simple body-effect reduction technique presents a universal use for performance enhancement of different ISFETs. Only one ISFET with differential configuration output allows solutions for body-effect problems, temperature-dependency and long-term drift, as well as common noise compensation. The presented instrumentation with implemented body-effect reduction technique enhances the accuracy of measurements performed by ISFET, while maintaining operations at constant drain-source voltage and current mode. Layout implementation of the proposed circuit was performed in a TSMC 0.35 μm double-poly and quadruple-metal CMOS process. Furthermore, a voltage-controlled dc offset error compensation circuit modulates the extracted signal to the desired dc level to the A/D converter for each sensor. This presented technique is suitable for monolithic ISFET-based microsystems.

Acknowledgments

The National Science Council, Republic of China, under contract of NSC 93-2215-E-033-008, the Institute of Biocybernetics and Biomedical Engineering, Polish Academy of Sciences and the Institute of Electron Technology, Poland, supported this work. Moreover, the authors would like to thank the National Chip Implementation Center (CIC), Taiwan for technical support.

References

[1] P. Bergveld, Development of an ion sensitive solid-state device for neurophysiological measurements, IEEE Trans. Biomed. Eng. 17 (1970) 70–71.
[2] T. Matsuo, M. Esashi, Methods of ISFET fabrication, Sens. Actuators B: Chem. 1 (1981) 77–96.
[3] P. Bergveld, Future applications of ISFETs, Sens. Actuators B: Chem 4 (1991) 125–133.
[4] P. Bergveld, Thirty years of isfetology—what happened in the past 30 years and what may happen in the next 30 years, Sens. Actuators B: Chem. 88 (2003) 1–20.
[5] Dorota G. Pijanowska, Analysis of factors determining parameters of ion sensitive field effect transistors as the sensors of biochemical quantities, PhD Thesis, Institute of Biocybernetic and Biomedical Engineering, Polish Academy of Science, Poland, 1996.
[6] G.-H. Wang, D. Yu, Y.L. Wang, ISFET temperature characteristics, Sens. Actuators 11 (1987) 221–237.
[7] P. Bergveld, A. Sibbald, Analytical and Biomedical Applications of Ion-Selective Field-Effect Transistors, vol. XXIII, Elsevier, Amsterdam, 1988.
[8] B. Palan, F.V. Santos, J.M. Karam, B. Courtois, M. Husak, New ISFET sensor interface circuit for biomedical applications, Sens. Actuators B: Chem. 57 (1999) 63–68.
[9] S. Casans, A.E. Navarro, D. Ramirez, J. Pelegri, A. Baldi, N. Abramova, Novel constant current driver for ISFET/MEMFETs characterization, Sens. Actuators B: Chem. 76 (2001) 629–633.
[10] K. Tukkineami, Study of CHEMFET Interface Electronics, MIXDES, 2002.
[11] A. Morgenshtein, L. Sudakov-Boreysha, U.s Dinnar, G. Jakobson, Y. Nemirovsky, Wheatstone-bridge readout interface for ISFET/REFET applications, Sens. Actuators B: Chem. 98 (2004) 18–27.
[12] W.Y. Chung, C.H. Yang, G. Pijanowska, A. Krzyskow, W. Torbicz, ISFET interface circuit embedded with noise rejection capability, Electron. Lett. 40 (18) (2004) 1115–1116.
[13] H.-S. Wong, H. White, A CMOS-integrated ISFET operational amplifier, chemical sensor employing differential sensing, IEEE Trans. Electron. Devices 36 (1989) 479–487.
[14] L. Ravczzi, P. Conci, ISFET sensor coupled with CMOS read-out circuit microsystem, Electron. Lett. 34 (1998) 2234–2235.
[15] J. Bausells, J. Carrabina, A. Errachid, A. Merlos, Ion-sensitive field effect transistors fabricated in a commercial CMOS technology, Sens. Actuators B: Chem. 57 (1999) 56–62.
[16] B. Palan, F.V. Santos, B. Courtois, M. Husak, Fundamental noise limits of ISFET-based microsystems, Eurosensors 13 (1999) 169–172.
[17] Y.L. Chin, J.C. Chou, T.P. Sun, W.Y. Chung, S.K. Hsiung, A novel pH sensitive ISFET with on chip temperature sensing using CMOS standard process, Sens. Actuators B: Chem. 76 (2001) 582–593.
[18] A. Morgenshtein, L. Sudakov-Boreysha, U. Dinnar, C.G. Jakobson, Y. Nemirovsky, CMOS readout circuitry for ISFET microsystems, Sens. Actuators B: Chem. 97 (2004) 122–131.
[19] S. Casans, A.E. Navarro, D. Ramirez, E. Castro, A. Baldi, N. Abramova, Novel voltage-controlled conditioning circuit applied to the ISFETs temporary drift and thermal dependency, Sens. Actuators B: Chem. 91 (2003) 11–16.
[20] S. Casans, D. Ramirez, A.E. Navarro, A. Salazar, ISFET drawbacks minimization using a novel electronic compensation, Sens. Actuators B: Chem. 99 (2004) 42–49.
[21] S. Martinoia, G. Massobrio, A behavioral macromodel of the ISFET in SPICE, Sens. Actuators B: Chem. 62 (2000) 182–189.
[22] K. Wada, Y. Tadokoro, Design of a body-effect reduced-source follower and its application to linearization technique, Proc. IEEE Int. Symp. Circuits Syst. 3 (2002) 723–726.

Biographies

Wen-Yaw Chung was born in Hsin-Chu, Taiwan, ROC, on 15 March 1957. He received the BSEE and MS degrees from Chung Yuan Christian University, Chung Li, Taiwan, in 1979 and 1981, respectively, and the PhD degree in electrical and computer engineering from Mississippi State University, USA, in 1989. Subsequently, he joined the Advanced Microelectronics Division, Institute for Technology Development in Mississippi, where he was involved in the design of a bipolar optical data receiver. In 1990 he worked as a design manager for the Communication Product Division, United Microelectronics Corporation, Hsin-Chu, where he was involved in the design of analog CMOS data communication integrated circuits. Since 1991 he has been an associate professor in the Department of Electronic Engineering at Chung Yuan Christian University. His research interests include mixed-signal VLSI design, biomedical IC applications, and test-chip design methodology for deep submicron VLSI electronics.

Chung-Huang Yang was born in Kinmen, Fujian, ROC, on 19 January 1966. He received the BSEE and MS degrees from Chung Yuan Christian University, Chung Li, Taiwan, in 1992 and 1994, respectively. Since 1994, he has been an Instructor of Electronic Engineering at the Vanung University of Science and Technology. He is currently working toward the PhD degree in the Department of Electronic Engineering at Chung Yuan Christian University. His research interests include mixed-signal IC design.

Dorota G. Pijanowska received the MSc degree in biomedical engineering from the Faculty of Precision Mechanic in the Warsaw University of Technology. She completed her PhD thesis on analysis of factors determining parameters of ion sensitive field effect transistors as the sensors of biochemical quantities in 1996. Her research interests include fabrication and characterization of chemical sensors and biosensors, mainly of the ISFET type, and their applications in biomedical diagnosis and environmental monitoring. She is a member of the Polish Society of the Sensor Technology.

Piotr B. Grabiec graduated Warsaw University of Technology in 1973 and received there PhD degree in chemistry in 1985. In 1974 he joined Institute of Electron Technology, Warsaw, Poland, where he was involved in research on CVD and diffusion technology. From 1988 he was a deputy and next, head of Silicon Technology Laboratory and R&D silicon technology line. In 1992–1993, he carried out research on advanced doping techniques in University of Houston, USA. In 1998–2000, he was involved in building and organization of Institute's Silicon Technology Lab on new premises. From 1999, he is head of Silicon Microsystem and Nanostructure Department. Currently he is responsible for R&D in the area of technology of ASIC's, silicon-based sensors and photodetectors. His present research activity involves a technology of silicon optoelectronic devices and MEMS, sensors and actuators with special emphasis on integration of mixed technologies. He was and is involved in 10 EU projects. Dr Grabiec has been awarded numerous professional awards for development and commercialization of advanced micro-devices. He is IEEE member and member of Electrochemical Society. He is an author of over 200 scientific papers and over 100 conference presentations and holds 10 patents.

Wladyslaw Torbicz obtained the MSc degree (1958) in electrical engineering from the Warsaw University of Technology and a PhD (1965) in electronic engineering and DSc (1989) in biomedical engineering from the Polish Academy of Sciences. Since 1991 he has been professor in the Institute of Biocybernetics and Biomedical Engineering of the Polish Academy of Science. His research work was devoted to electronic components of control systems, memory devices and biomedical devices. Since the early 1980s his fields of research work are chemically sensitive semiconductor devices, mainly of the ISFET type and their applications in biomedical diagnosis and environmental monitoring. He is the deputy president of the Polish Society of Sensor Technology.