Study on Performance of Capacitor-less LDO with Different Types of Resistor

Wan Maziyah Ab. Halim
Dept. of Electronic Engineering
UNiKL BMI
Malaysia
maziyah.halim@s.unikl.edu.my

Julie Roslita Rusli
Dept. of Electronic Engineering
UNiKL BMI
Malaysia
julie@unikl.edu.my

Suhaidi Shafie
Dept. of Electrical & Electronic Engineering
UPM
Malaysia
suhaidi@upm.edu.my

Yuzman Yusoff
Research and Development (IC),
MIMOS Bhd.
Malaysia
yuzman@mimos.my

Chia Chieu Yin
Research and Development (IC),
MIMOS Bhd.
Malaysia
cy.chia@mimos.my

***Abstract*—This paper studies the impact of utilizing different resistor types in capacitor-less low drop-out (LDO) voltage regulator on its key performance characteristics. In order to achieve this, a 1.8 V LDO voltage regulator is designed and characterized using 180 nm CMOS technology with a supply voltage of 3.3 V. Simulations are done in schematic level using Cadence on five different types of resistor for the same LDO, and the performance in terms of output voltage accuracy, stability and power supply rejection ratio (PSRR) are compared. From the simulation results, significant differences are observed in the LDO's performance with different types of resistor. The LDO with *hpoly* resistor gives the best results in terms of stability while *pdiffb* resistor LDO produces the highest PSRR.**

Keywords—capacitor-less LDO, capacitor-less LDO performance comparison, LDO resistor type comparison

I. INTRODUCTION

The expansion of mobile electronics area makes a low dropout (LDO) voltage regulator an important building block in power management system as it can be designed to supply a specific desired output voltage needed by the circuits from limited supply voltage. It enables the user to regulate an output voltage from a higher input voltage in a simple and inexpensive way [1] as it is used to approximate an ideal voltage source in real life [2]. A basic LDO circuit consists of four main parts; the error amplifier, the pass transistor, the feedback network and the load as shown in Fig. 1 [2]. One of the recent improvement areas in LDOs is to make it capacitor-less. In LDOs, a bulky external capacitor, denoted as C_L in Fig. 1, is often needed to provide stability and good transient response. Stability is critical in LDO design since the unity gain bandwidth (UGBW) and the poles locations are directly affected by the load current I_L [3]. The PSRR can also be improved by using the large off-chip load capacitor. However, the drawback of using it is mainly the need to use external component, hence preventing the LDO to be used in system-on-chip (SOC) solutions, besides higher cost and increased total printed circuit board (PCB) area [3]. Therefore, a LDO that has good stability and high PSRR but does not require a large external capacitor will provide a great advantage to a system which aims for minimum external component and minimal area, which is what portable device is all about these days.

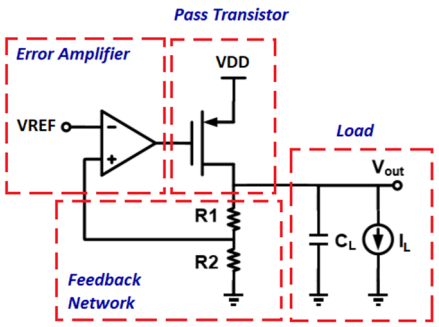

Fig. 1 Basic LDO topology

An LDO's performance is measured and evaluated based on a few key criteria. One of the key criteria is the stability, and the parameter which is used to determine it is the phase margin. In order for the system to be considered stable, the phase margin needs to be at least 60°. Another key criterion of the LDO is the PSRR. PSRR refers to the amount of voltage ripple at the output of the LDO coming from the input voltage [3]. The PSRR is measured in decibel (dB), with greater magnitudes implying better ripple rejection at the output. Variation across temperature and process also have to be considered, especially in systems involving resistors and capacitors. These variations can affect the output voltage accuracy of the LDO, since they can cause a change in a particular parameter in the elements, such as resistance, current and etc. This is because capacitors and resistors are circuit elements in which their values change with temperature [4].

Multiple studies and research were done in different areas of a LDO to improve its performance. For error amplifiers, different circuit approach and topologies were studied in order to find the best solution. Studies were also done on the pass transistor, on whether it is best to use NMOS or PMOS to get the best results under different conditions. There are also complementary circuits suggested in other studies to improve the PSRR of the LDO. Since numerous studies were done in the mentioned areas and other complementary circuits of the LDO, this paper will focus on the impact of different resistor types on the LDO performance. Different resistor types have different parameters, such as sheet resistivity which will affect its total area, parasitic capacitance, and variation in temperature and process. These parameters might affect the performance of the LDO in the key criteria discussed

previously. Due to its capacitor-less feature, parasitic capacitance has become an important parameter to be considered, as the LDO will not have the large external capacitor for stability compensation. Since there will be two resistors in the voltage divider, matching is also an important feature to achieve optimum results [5].

II. LDO Design

A. LDO Sub-circuits Design

The LDO in this paper employed a single stage differential op-amp topology for its error amplifier as shown in Fig. 2. The topology was chosen for design simplicity and stability purpose [6].

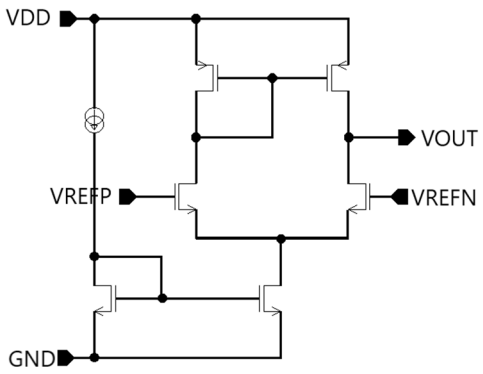

Fig. 2. Single-stage Op-amp Circuit

The pass transistor used for the LDO is a PMOS. PMOS is widely used in most LDOs as the pass transistor due to its characteristic of operation which turns on when the gate voltage is lower than the source voltage by a threshold voltage. This makes it suitable for systems with low supply voltage [7], which is currently the case for most integrated circuit designs as CMOS technology becomes smaller in scale with time. If a NMOS is to be used as the pass transistor, a higher voltage which is sufficient enough to turn on the pass transistor is required. If the supply voltage is not high enough, complementary circuits to boost up the voltage at the gate is needed.

Two resistors were used for the feedback network in the LDO as shown in Fig. 1. In this design, the value of VREF is 1.2 V, and it will set the feedback node of the LDO to this voltage. A 120 kΩ resistor for R2 was needed to maintain the pre-set current of 10 µA going through the two resistors. R1 was set to 60 kΩ in order to generate the 1.8 V output voltage of the LDO.

The load current set for the simulation was 10 mA, with a load capacitor of 100 pF. The load capacitance was decided based on available capacitor-less LDOs [8] [9].

B. Tested Resistor Types

Various resistor types are available in the 180 nm CMOS process library. There are resistors with smaller resistance value (in the range of tens to kΩ) while there are also resistors which can provide larger resistance values (up to the range of MΩ). Each resistor type comes with its own parasitic element modelled by the foundry, which means the parasitics were considered and included when the resistor was simulated. The resistors tested in this paper are all in the larger resistance value category, as the resistance of R1 and R2 are in the range of tens and hundreds of kΩ. The resistors tested were finalized to be five types as listed below:

i. *hpoly* (High P+ poly resistor)
ii. *pplyb* (P poly unsalicide resistor)
iii. *pdiffb* (P+ diffusion unsalicide resistor)
iv. *ndiffb* (N+ diffusion unsalicide resistor)
v. *sbninw* (N+ diffusion unsalicide resistor on nwell)

III. Design and Test Methodology

In designing the LDO used for this study, the initial step was to design and characterize an error amplifier to satisfy certain basic requirements such as gain, stability and PSRR. The error amplifier was then integrated with a PMOS pass transistor and a feedback network using ideal resistors to develop a complete LDO. The size of the pass transistor was properly tuned until it can drive the current set at the output node.

The simulated results of ideal resistors were obtained, and the resistors for the feedback network were changed from ideal to real resistors listed in section II (B). Simulations were repeated for every type of resistor. The parameters of each resistor material were set so that R1 and R2 would have the same width. The purpose of fixing the width was to match both resistors R1 and R2. R1 and R2 were divided into segments with each segment having the same width and length. This provides great advantage in matching and parasitic distribution in layout design. The usage of unit resistor is important for precision over large temperature range [10]. Table I specifies the details of the parameters set for all resistors used in the tests.

TABLE I. Resistor Material Type and Respective Parameters Set

Material	R1 = 60 kΩ		R2 = 120 kΩ		Estimated Total Area / µm²
	W/L ratio	No. of Segments	W/L ratio	No. of Segments	
Ideal	n/a	n/a	n/a	n/a	n/a
hpoly	1/9	6	1/9	12	840
pplyb	1/31	6	1/31	12	2600
pdiffb	1/23	20	1/23	40	6600
ndiffb	1/29	30	1/29	60	12000
sbninw	1/33	30	1/33	60	18500

IV. Results and Discussion

The LDOs with different resistors were compared in the following criteria:

A. Output voltage accuracy

B. Phase margin

C. UGBW

D. PSRR

A. *Output Voltage Accuracy*

The output voltage of the LDO with all resistors showed fairly accurate reading from 99.99% to 100% of accuracy as shown in Table II, taking the expected value of 1.8 V as 100% benchmark. This shows that there is almost no degradation in resistance value and no changes in current at the output node. LDOs with *hpoly*, *pplyb* and *pdiffb* produced the output voltage of 1.7999 V, while the LDOs with *ndiffb* and *sbninw* produced 1.8 V, the same with the expected output voltage of the LDO. All output voltages are shown in Fig. 3.

The output voltage was also simulated from a temperature of -40 °C to 125 °C, and the results showed very small variation for the five types of resistor, within the range of 30 µV to 50 µV. Based on Fig. 4, *hpoly* and *pplyb* have almost identical variation curve across temperature, overlapping with the ideal resistor's curve. As for *pdiffb*, the pattern is the same with *hpoly* and *pplyb* but at 20 µV lower potential. Resistors *ndiffb* and *sbninw* have slightly different curve patterns from the rest at higher temperatures.

In terms of process variation as can be seen in Fig. 5, three defined process in the library for the resistors were simulated; minimum, typical and maximum. The LDO with *hpoly* and *pplyb* resistors have the smallest voltage difference between minimum and maximum with 0.8 µV of voltage change, while the LDO with *sbninw* resistor, with 6.8 µV has the largest voltage change. From the voltage change shown in Table II, it can be observed that the value becomes larger for resistors which have larger total area which was shown in Table I.

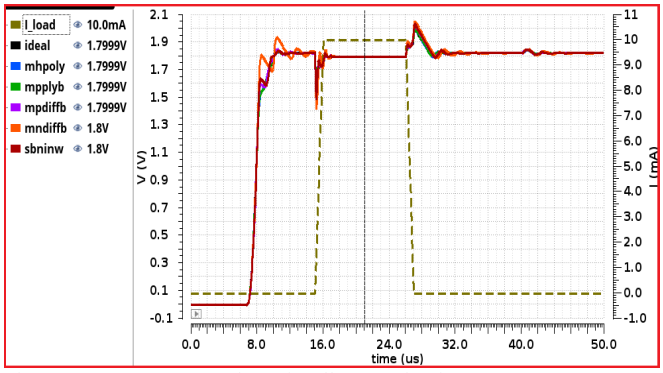

Fig. 3 LDO Output voltage for all types of resistor.

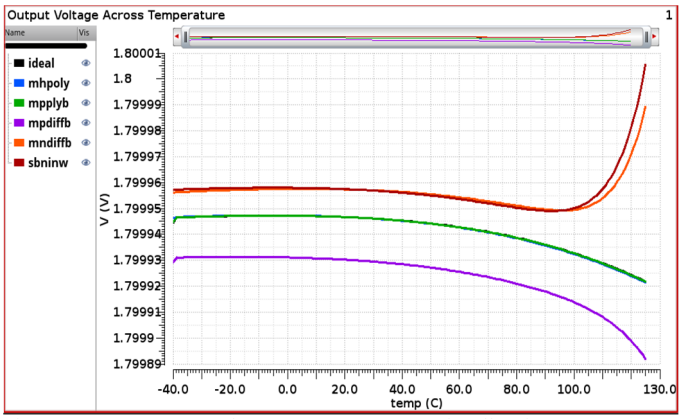

Fig. 4 LDO output voltage across temperature for all resistor types

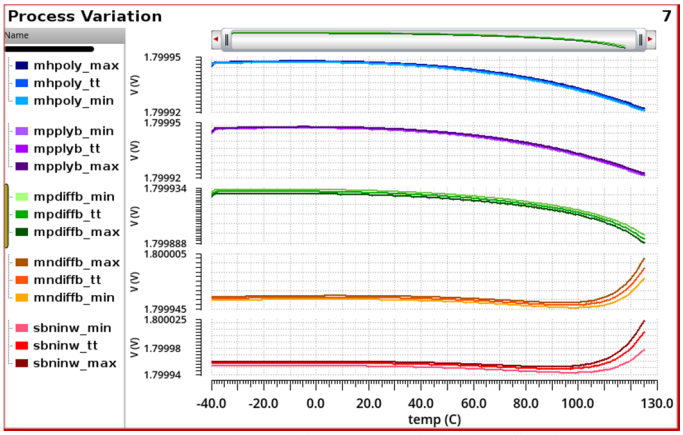

Fig. 5 LDO output voltage with process variation for all resistor types

B. *Phase Margin*

The phase margin produced by using ideal resistors was 84.8°, which is considered very stable for most systems, and followed closely by the LDO with *hpoly*, with a phase margin of 83.6°, showing a slight degradation from the ideal resistor. The LDO using *pplyb* came in third with 80.7°. Out of the five tested resistors, *hpoly* and *pplyb* were the only types which maintained the phase margin to be above 60°. The phase margin for the LDO using *pdiffb* was 53.0°, followed by *sbninw* with 50.4° and the lowest phase margin was 38.9°, produced by *ndiffb* with a difference of 45.9° compared to the ideal resistors LDO. All phase margin curves are included in Fig. 6.

Obvious degradation in phase margins could be observed for LDOs using *ndiffb* and *sbninw* resistors probably due to the parasitic capacitance produced by them. As the sheet resistivity for the two materials are much lower (below 100 Ω) compared to *hpoly*, *pplyb* and *pdiffb* (between 300Ω to 1 kΩ), the estimated total areas for *ndiffb* and *sbninw* were therefore larger, producing higher parasitic capacitance. If the parasitic capacitance is large enough, the position of the secondary pole could possibly be shifted, causing the system to become less stable.

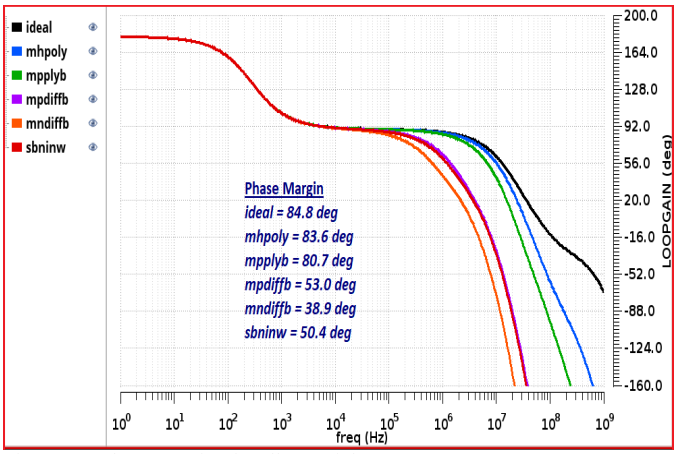

Fig. 6 Phase margins for all materials

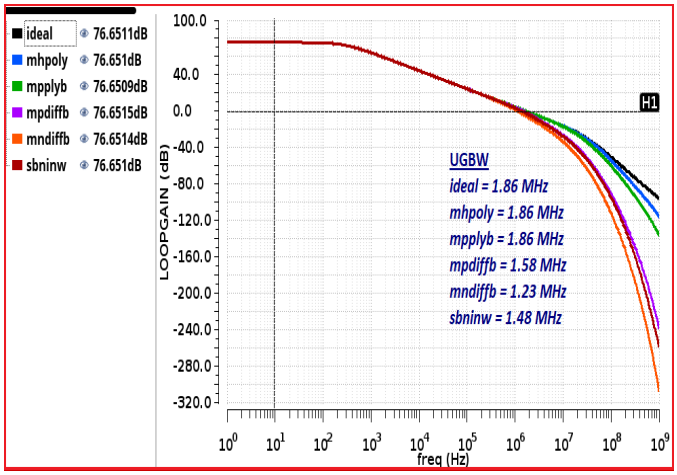

Fig. 7 DC gain for all materials

C. *UGBW*

All materials produced the same DC gain of approximately 76 dB as can be seen in Fig. 7. In terms of UGBW, LDOs with *hpoly* and *pplyb* had the same value with the ideal resistor UGBW of 1.86 MHz. The LDO with *pdiffb* resistor showed a slight decline to 1.58 MHz, followed by *sbninw* with 1.49 MHz. The lowest UGBW came from the LDO with *ndiffb* resistor with 1.23 MHz of UGBW, showing degradation of 630 kHz from the LDO with the ideal resistors.

D. *PSRR*

As shown in Fig. 8, the PSRR for ideal resistor LDO were approximately 76 dB, 65 dB, 25 dB and 6 dB at 10 Hz, 1 kHz, 100 kHz and 1 MHz respectively. The PSRR for all resistor types were around the same values as the ideal resistor LDO at 10 Hz. At 1 kHz, except for LDO using *pdiffb* resistor which obtained higher PSRR at about 72 dB, all other resistors had 65 dB of PSRR. At 100 kHz, the LDO with *pdiffb* resistor again showed the highest PSRR with 34 dB, while the rest of the resistors obtained the same PSRR as the ideal resistor LDO with 25 dB. The variation of PSRR at 1 MHz was more distinct for LDOs with *pdiffb*, *ndiffb* and *sbninw* with 10 dB, 1 dB and 3 dB respectively, while *hpoly* and *pplyb* showed the same PSRR as the ideal resistor LDO with 6 dB. While the LDOs using *hpoly* and *pplyb* resistors had the closest results to ideal resistor, the LDO using *pdiffb* resistor showed the highest PSRR at all three frequencies compared to the other materials, while ndiffb has the lowest PSRR at 1MHz frequency, as can be seen in Table II. The only difference between *pdiffb* and the other resistors is its body connection. While the body connections for *hpoly*, *pplyb* and *ndiffb* were to ground, the body of *pdiffb* was connected to the supply voltage. This implies that the parasitic capacitance models of the *pdiffb* resistor was also connected to the supply voltage. Table II summarizes the simulated performances of the LDO with different types of resistor.

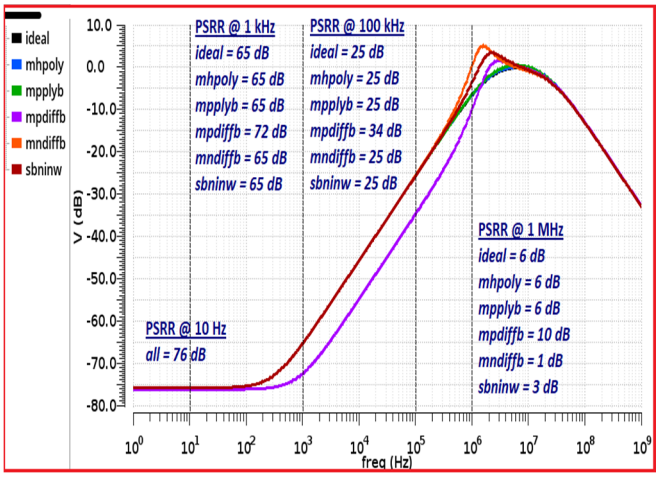

Fig. 8 PSRR for all materials

TABLE II. STABILITY AND PSRR COMPARISON FOR DIFFERENT RESISTOR TYPE LDOS

Resistor Type	Output Voltage Accuracy			UGBW (Hz)	Phase Margin (°)	PSRR (dB)			
	Vout (V)	Accuracy (%)	ΔV-Process (μV)			@10 Hz	@1 kHz	@100 kHz	@1 MHz
Ideal	1.7999	99.99	n/a	1.86 M	84.8	76	65	25	6
hpoly	1.7999	99.99	0.8	1.86 M	83.6	76	65	25	6
pplyb	1.7999	99.99	0.8	1.86 M	80.7	76	65	25	6
pdiffb	1.7999	99.99	3.5	1.58 M	53.0	76	72	34	10
ndiffb	1.8000	100.00	4.1	1.23 M	38.9	76	65	25	1
sbninw	1.8000	100.00	6.9	1.49 M	50.4	76	65	25	3

V. CONCLUSION

From the results, it is concluded that there are significant impacts in LDO performance when using different types of resistor. All five different types of resistor produce high level of accuracy for the output voltage with very small variation across temperature and under different process. In overall, *hpoly* has the best results comparable to the ideal resistor in terms of stability, with 1% difference in phase margin and identical UGBW with the ideal resistor, followed closely by *pplyb*. In terms of PSRR on the other hand, *pdiffb* shows the highest result, with a significant increase of approximately 11% at 1 kHz, 36% at 100 kHz and 67% at 1 MHz as compared to the ideal resistor. The drawback of *pdiffb* resistor

is its relatively much lower sheet resistivity compared to *hpoly* and *pplyb*, which results in very large area consumption for large resistance values, thus making it less suitable for LDOs which aim for low quiescent current. Nonetheless, if PSRR is the highest priority, *pdiffb* would make the best option given that bigger current is acceptable to compensate lower resistance value in order to reduce the total area of the resistor.

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