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Dual-transformer-based hybrid resonant three-level ZCS converter

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ABSTRACT

A hybrid resonant three-level converter comprised of dual transformers is proposed in this paper, which is suitable for the application of distributed photovoltaic power accessing the medium voltage dc distribution network. The proposed converter can be obtained by adding a control circuit into the traditional neutral point clamped (NPC) three-level (TL) circuit, achieving the basic TL circuit operating with a fixed duty cycle. Pulse width modulation (PWM) is adopted for the control circuit to realize zero current switchings for the basic TL circuit, which delivers most of the power, under full load range. As a result, the switching loss of the converter can be significantly reduced. The influences of the turn ratio of the second transformer and resonant capacitance on the switch current, the peak value of resonant voltage, and the value of the resonant inductance value are discussed in detail, and the parameters design principles are put forward. Finally, a prototype is built to verify the performance of the proposed converter.

1. Introduction

With the advancement of science and technology, the level of solar cell technology has been greatly improved in the past few years. The cost of photovoltaic power generation has been dropped rapidly, and the capacity for power generation has been greatly increased. In the next few years, the focus of the development of photovoltaic power generation in China will shift from a centralized power station to a distributed power generation system. In 2017 China's distributed photovoltaic power generation will add 19GW (Hu and Liu, 2017; Cheema and Mehmood, 2019; Cheema, 2020). The distributed photovoltaic power generates a DC output which is basically directly connected to the AC distribution network. Therefore, distributed PV access to DC power distribution networks can save many commutation links. It has a low operating cost, high reliability and low transmission losses (Jiang and Zheng, 2012; Song et al., 2013).

A certain amount of research experience has been accumulated in the field of DC power supply and distribution. The research work on low voltage DC power supply is mainly reflected in the low voltage DC microgrids, such as the green building research plan (Boroyevich et al., 2010) and a set of bipolar DC distribution network system (Kakigano et al., 2010) designed relatively few researches on medium voltage DC power distribution, such as the 10kV DC campus DC distribution project (Mura and W. De Doncker, 2011), and ± 10 kV DC power distribution demonstration project (Liu et al., 2016). To further study and promote medium-voltage DC distribution network technology, DC Power Distribution Feasibility Study is established in 2015 (Sheng et al., 2016).

The core device of distributed PV access to DC power distribution network is a medium voltage DC boost converter with a high step-up ratio, such as the resonant switched capacitor converter proposed by Chen et al. (2013) and the composite full-bridge converter in Ning et al. (2017a). With the increase of voltage and power of the photovoltaic module (Gkoutioudi et al.), the system puts forward higher requirements on the voltage stress of the new energy side switching of the medium voltage DC converter, so the classic full-bridge structure may not meet the new requirements. The multilevel circuit (Zhang and Ruan, 2004) can significantly reduce the voltage stress of the switching device. For example, in the commonly used three-level circuit (Liu et al., 2014), the voltage stress of the switching device is only half of the input voltage. In addition, to improve the transmission efficiency of the converter and reduce the cost and complexity of the system's heat dissipation structure of the system, soft switching technology can be incorporated into the three levels of DC converters. The most basic soft switching technologies are Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). Because the MOSFET's structure leads to a large parasitic capacitance, ZVS is suitable for MOSFETs (Ruan et al., 2005).

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Although MOSFETs may reach a high switching frequency, they are relatively common in low and medium power applications due to their low voltage through-current capability. The distributed photovoltaic access to the medium-voltage DC distribution network is relatively large. Therefore, it is more reasonable to use IGBTs as switching devices. For the IGBTs current tailing characteristics, the ZCS switching off can greatly reduce the switching losses (Yin et al., 2016). Yu (2017) proposed a new three-level DC–DC converter with an auxiliary source circuit based on Neutral Point Clamped (NPC) three-level circuit, which can realize all the switches, including auxiliary IGBTs. The maximum blocking voltage that the auxiliary IGBT must withstand is the output voltage, so it is only suitable for low voltage and high current output applications. Ning et al. (2017b) proposed a novel full-bridge DC–DC converter with double transformers, which can realize the ZCS of the switching and rectifier diodes. However, all switching voltage stress is the input voltage, and the current peak is larger.

To fully meet the voltage requirements of the access medium voltage direct current distribution network, a hybrid resonant three-level ZCS DC converter is proposed based on the dual transformer structure idea, and the resonance technology is introduced to reduce the peak current value. The converter mainly includes the basic NPC three-level circuits and the auxiliary circuit two parts. The power and voltage regulation of the whole converter can be realized only by using PWM pulse width modulation in the auxiliary circuit part, so that the 4 switches of the base three level are operated in the fixed duty ratio mode, Only need to use the PWM to the auxiliary circuit part to realize the power and voltage regulation of the whole converter, make the basic three-level 4 switches work in the fixed duty cycle mode, which has the advantages of the simple control. By reasonable design, the boost ratio of the main transformer so that the basic three-level circuit can transmit most of the power. It can achieve its ZCS turn-on and turn-off within the full load range, thereby significantly reducing the switching losses of the converter. Besides, the boost ratio of the auxiliary transformer can be optimized to reduce the loss of the converter further and improve the conversion efficiency.

2. Circuit configuration and operation principles

The main circuit topology of the converter proposed in this paper is shown in Fig. 1. The input side is divided into two parts:The first part is composed of input voltage divider capacitors C_{in1} and C_{in2}, switches Q_1 to Q_4(IGBT), clamp diodes D_{c1} and D_{c2}, the primary side of the first transformer T_{r1}, and inductance L_r(including the primary side leakage inductance of T_{r1}). The second part is an auxiliary circuit composed of voltage dividing capacitors C_{d1} and C_{d2}, switches Q_5 and Q_6 (MOSFET), freewheeling diodes D_{f1} and D_{f2}, auxiliary transformer T_{r2} primary and resonant capacitor C_r. The output side is the voltage doubler rectifier circuit, and the secondary windings of T_{r1} and T_{r2} are directly connected in series and used as the input of the rectifier circuit. The primary and secondary turns ratios of T_{r1} and T_{r2} are 1: N_1 and 1: N_2, respectively. In order for the converter to work properly, N_1 should be greater than N_2. Through proper design of N_1 and N_2, T_{r1} will process the majority of power (about 90%), and the T_{r2} will process the remaining small portion (about 10) of power.

Fig. 2 shows the main waveform of the converter. Switches Q_1 and Q_2 (Q_3 and Q_4) are simultaneously turned on and off at the same time with a 50% fixed duty cycle with enough dead time. Q_5 and Q_6 use chopper controlled on the leading edges of Q_1 and Q_3, respectively. The converter output voltage is controlled by adjusting the duty cycle of Q_5 and Q_6. Before making a detailed analysis, make the following assumptions:

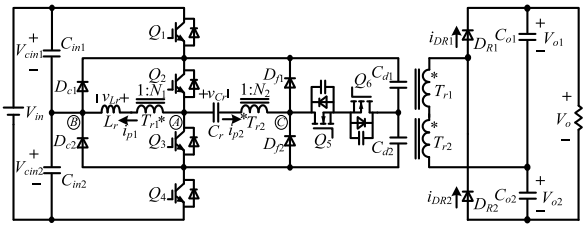

Fig. 1. Proposed converter.

(1) All switches, diodes, inductors, and capacitors are ideal devices;
(2) The input voltage divider capacitors C_{in1} and C_{in2} are equal and large enough, so $V_{cin1} = V_{cin2} = V_{in}/2$; the capacitors C_{d1} and C_{d2} are equal and large enough; the output filter capacitors C_{o1} and C_{o2} are equal and large enough, so the output voltage V_o is considered to be constant and $V_{o1} = V_{o2} = V_o/2$.
(3) The leakage inductance of the transformer T_{r2} is so small that it is negligible.

As can be seen in Fig. 2, the converter has four modes in the first half switching period [t_0, t_3], and the corresponding current paths for each mode are shown in Fig. 3.

(1) T_0: t_0 is the starting point of a new switching cycle. At that time, Q_3 and Q_4 are turned off, and Q_1, Q_2 and Q_5 are opened. From the current waveform given in Fig. 2, it can be seen that no current is flowing through all the switches before t_0. Therefore, Q_3 and Q_4 are ZCS turn off, while Q_1, Q_2, and Q_5 are turned ON with ZCS.
(2) Mode 1 [t_0, t_1] (see Fig. 3(a): The equivalent circuit of this model is shown in Fig. 3(a): In this mode, the primary current i_{p1} of T_{r1} flows through the primary windings Q_1, Q_2, L_r, T_{r1}, and C_{in1}. Therefore, the voltage between points A and B is half of the input voltage, $v_{AB} = 0.5V_{in}$. In the same way, the primary current i_{p2} of T_{r2} flows through the primary windings of Q_1, Q_2, C_r, T_{r2}, the parasitic capacitances of Q_5, Q_6, C_{d2}, D_{c2}, and C_{in1}. Because the voltage across Q_6 is $0.25V_{in}$ at t_0 discharges to zero in this mode, the voltage v_{AC} between A and C drops from $0.5V_{in}$ to $0.25V_{in}$. In this mode, L_r is resonant with three parasitic capacitances of C_r and Q_6, and the C_r terminal voltage v_{Cr} begins to rise from the minimum V_{Crmin}. Also, the current flowing through Q_1 and Q_2 is the sum of i_{p1} and i_{p2}, as shown in Fig. 3(a).
(3) Mode 2 [t_1, t_2] (see Fig. 3(b): At t_1, the voltage across Q_6 has been to zero, i_{p2} flows from the body diode of Q_6, and the current path of i_{p1} is constant, so L_r only resonates with C_r, and the current begins to resonate. At the same time, $v_{AB} = 0.5V_{in}$ and $v_{AC} = 0.25V_{in}$.
(4) Mode 3 [t_2, t_3] (see Fig. 3(c): Turning off Q_5 at time t_2, and i_{p2} begins to charge the parasitic capacitance of Q_5 through the body diode of Q_6, so Q_5 can realize ZVS and this charging current is far greater than the discharge current in Mode 1. Therefore, the parasitic capacitance charge time of Q_5 is very short and can be negligible. When the voltage across Q_5 rapidly rises to $0.25V_{in}$, i_{p2} flows back to Q_2 through freewheeling diode D_{f1}; then there is $v_{AC} = 0$. Therefore, it can be seen that the secondary voltage of T_{r1} is $V_o/2 + N_2 v_{Cr}$, and at the same time v_{Cr} continues to rise, causing the L_r terminal voltage to jump to a negative value so that the current begins to decrease in resonance. V_{Cr} rises to the maximum value V_{Crmax} at t_3. Since the average value of V_{Cr} in one cycle is zero, so $v_{Cr} = V_{Crmax} = -V_{Crmin}$. Since no current flows through Q_5 and Q_6 in this

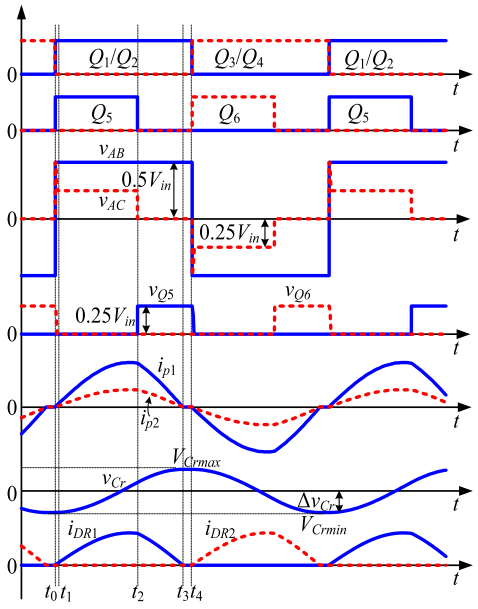

Fig. 2. Key waveforms of the proposed converter.

Table 1
Switching characteristic and voltage stress of semiconductors.

	$Q_1 \sim Q_4$	Q_5, Q_6	D_{f1}, D_{f2}	D_{R1}, D_{R2}
Turn-on	ZCS	ZVZCS	–	–
Turn-off	ZCS	ZVS	ZCS	ZCS
Voltage stress	$0.5V_{in}$	$0.25V_{in}$	$0.5V_{in}$	V_o

mode, the terminal voltages of both remain $0.25V_{in}$ and zero, respectively.

(5) Mode 4 [t_3, t_4] (see Fig. 3(d): By designing important parameters such as L_r, N_1, N_2, and C_r, all currents drop to zero at t_3 time. Hence, D_f and rectifier diode D_{R1} are turned off with ZCS. The reflected voltage to the secondary windings of T_{r1} and T_{r2} is lower than the rectified voltage, that is, $(N_1V_{in} - N_2V_{Crmax}) < V_o/2$ (when it comes to the rectifier diode D_{R2}, one can obtain $N_1V_{in} - N_2V_{Crmax} + V_o/2 > 0$), leading to D_{R1} and D_{R2} reversely blocked. In this mode, although the switches Q_1 and Q_2 are turned on, the currents i_{p1}, i_{p2}, and i_{DR1} are always zero, and the load is supplied by the output filter capacitor

(6) t_4: t_4 is the end of the first half switching cycle, and the starting point of the second half of switching cycle. Obviously, Q_1 and Q_2 are turned off with ZCS, Q_3, Q_4, and Q_6 are turned on with ZCS. In addition, since the terminal voltage of Q_6 in modes 3 and 4 is already zero, Q_6 achieves zero voltage zero current switching (ZVZCS) turn-on.

The second half of the switching cycle is similar to the analysis of the above half switching cycle. In addition, because T_{r1} transfers more energy than T_{r2}, the rated current of $Q_1 \sim Q_4$ is larger than that of Q_5 and Q_6. Therefore, the proposed converter has a smaller switching loss. In addition, the maximum blocking voltage that Q_5 and Q_6 need to withstand is only $0.25V_{in}$, and they can realize the ZVZCS on. Then, MOSFETs can be selected for Q_5 and Q_6. Based on the above analysis, the switching characteristics and voltage stress of semiconductor devices can be summarized in Table 1.

3. Parameters design

For the convenience of analysis, a DC–DC converter with the following specifications is taken as an example in this section.

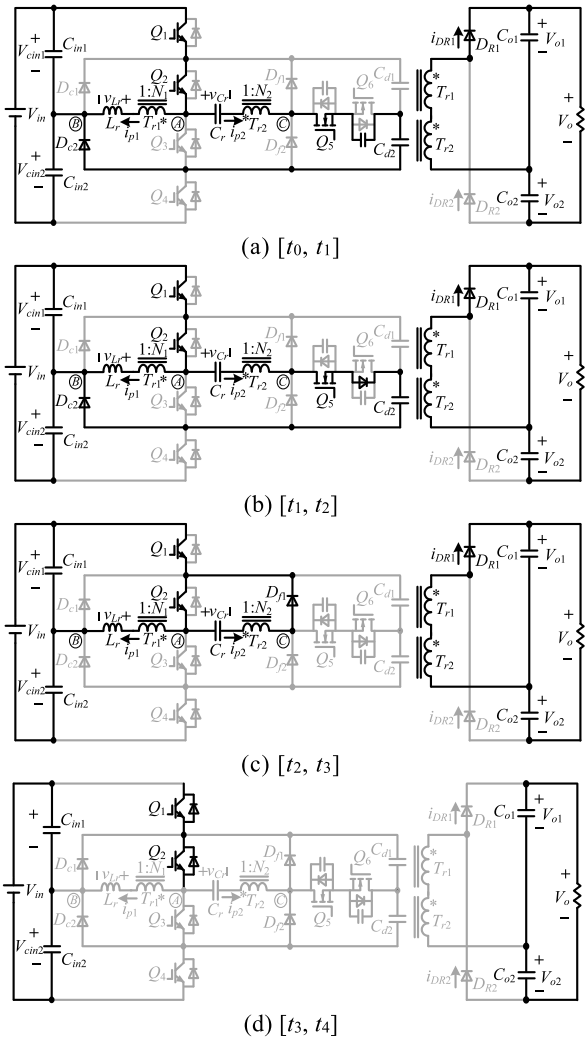

Fig. 3. Circuit paths of four modes.

- input voltage $V_{in} = 1.5$ kV
- output voltage $V_o = 15$ kV
- rated power $P_N = 500$ kW
- switching frequency $f_s = 1$ kHz

According to the above mode analysis, converting the main resonant elements L_r and C_r to the output side can obtain the equivalent circuit as shown in Fig. 4, where $L_{r\_s} = N_1^2L_r$ and $C_{r\_s} = C_r/N2^2$. The resonant angular frequency and resonant impedance of the equivalent circuit can be expressed as:

$$\begin{cases} \omega_r = 1/\sqrt{L_{r\_s}C_{r\_s}} = 1/\sqrt{N_1^2L_rC_r/N_2^2} \\ Z_r = \sqrt{L_{r\_s}/C_{r\_s}} = N_1N_2\sqrt{L_r/C_r} \end{cases} \tag{1}$$

Because the time length of Mode 1 is very short, and the resonant current and the resonant voltage change little during this period, it can be ignored in this section. According to Kirchhoff's voltage law (KVL), Modes 2 and 3 can be represented by second-order differential equations.

$$\begin{cases} \dfrac{(N_1 + N_2/2)\,V_{in}}{2} - \dfrac{V_o}{2} = N_1^2L_r\dfrac{C_r}{N_2^2}\dfrac{d^2v_{Cr\_s}(t)}{dt^2} + v_{Cr\_s}(t) \\ \dfrac{N_1V_{in}}{2} - \dfrac{V_o}{2} = N_1^2L_r\dfrac{C_r}{N_2^2}\dfrac{d^2v_{Cr\_s}(t)}{dt^2} + v_{Cr\_s}(t) \end{cases} \tag{2}$$

where $i_s(t) = C_{r\_s}dv_{Cr\_s}(t)/dt$ is the secondary current and v_{Cr_s} is the voltage across C_{r_s} (see Eq. (3) in Box I).

$$\begin{cases} [v_{Cr\_s}(t) - ((N_1/2 + N_2/4)V_{in} - V_o/2)]^2 + (Z_r i_s(t))^2 = [(N_1/2 + N_2/4)V_{in} - V_o/2 - V_{Cr\_smin}]^2 & (Mode2) \\ [v_{Cr\_s}(t) - (N_1 V_{in}/2 - V_o/2)]^2 + (Z_r i_s(t))^2 = (N_1 V_{in}/2 - V_o/2 - V_{Cr\_smax})^2 & (Mode3) \end{cases} \quad (3)$$

Box I.

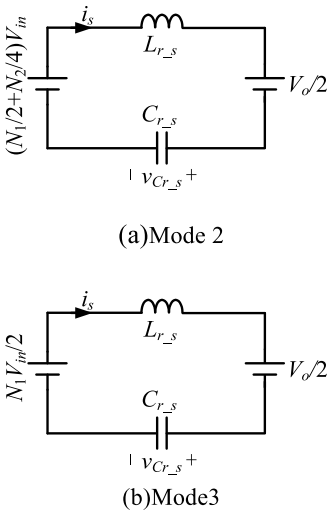

Fig. 4. Equivalent circuits of Modes 2 and 3.

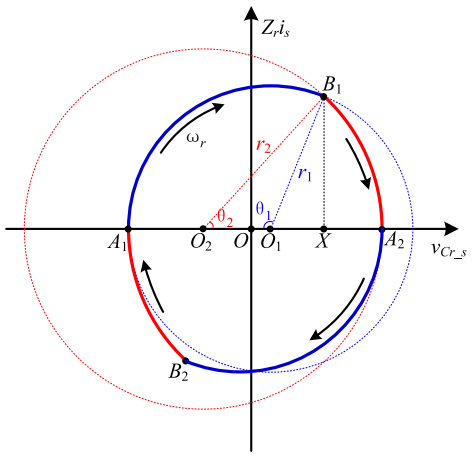

Fig. 5. Steady-state trajectory path.

With the reduced-order calculation of (2), one can obtain (3), where v_{Cr_smax} and v_{Cr_smin} are the maximum and the minimum values of v_{Cr_s}, respectively, and $\Delta v_{Cr\_s} = V_{Cr\_smax}$ = -V_{Cr_smin}.

Fig. 5 shows the steady-state trajectory path and is drawn according to (8). The axis of abscissa represents the voltage v_{Cr_s}, and the axis of ordinate represents multiplied by Z_r. Thus, both axes share the same unit-volts. $A_1 \rightarrow B_1$ represents the process of Mode 2 (Generally, the intrinsic capacitor of MOSFET is much smaller than the resonant capacitor so that Mode 1 is not taken into consideration in this section), while $B_1 \rightarrow A_2$ represents Mode 3. The node A_2 represents Mode 4 as the current is zero, and the voltage v_{Cr_s} remains unchanged during this mode. Likewise, the next half switching cycle is $A_2 \rightarrow B_2 \rightarrow A_1$. Due to the symmetry of two half switching cycles, only Modes 2 to 4 will be analyzed in the following.

The node A_1 (V_{Cr_smin}, 0) represents the starting time point of a switching cycle, while the node A_2 (V_{Cr_smax}, 0) is the end of the first half switching cycle. Therefore, the radius of arcs A_1B_1 and B_1A_2 can be expressed as

$$\begin{cases} r_1 = |A_1O_1| = (N_1/2 + N_2/4)V_{in} - V_o/2 - V_{Cr\_smin} \\ r_2 = |O_2A_2| = V_{Cr\_smax} - (N_1 V_{in}/2 - V_o/2) \end{cases} \quad (4)$$

Hence, the abscissa values of θ_1 and θ_2 are $(N_1 + N_2/2)V_{in}V_o/2$ and $N_1V_{in}V_o/2$, respectively.

The abscissa value of the node B_1 can be calculated by solving (3), and we can get

$$x(B_1) = [4V_o - (4N_1 + N_2)V_{in}]\frac{\Delta v_{Cr\_s}}{N_2 V_{in}} \quad (5)$$

θ_1 and θ_2 represent the angles of Modes 2 and 3, respectively, and can be express as

$$\begin{cases} \theta_1 = \omega_r(t_2 - t_1) \\ \quad = \arccos\left(\dfrac{(N_1/2 + N_2/4)V_{in} - V_o/2 - x(B_1)}{r_1}\right) \\ \theta_2 = \omega_r(t_3 - t_2) = \arccos\left(\dfrac{x(B_1) - N_1 V_{in}/2 + V_o/2}{r_2}\right) \end{cases} \quad (6)$$

According to Fig. 5, the current can be expressed as

$$i_s(t) = \begin{cases} r_1 \sin(\omega_r(t - t_1))/Z_r & t_1 < t < t_2 \\ r_2 \sin(\omega_r(t_3 - t))/Z_r & t_2 < t < t_3 \end{cases} \quad (7)$$

3.1. Turns ratio N_1 and N_2

As mentioned before, by properly designing N_1 and N_2, the transformer T_{r1} can transmit a majority of the power while the transformer T_{r2} transmits the remaining power. Therefore, this section will elaborate on the design of the transformer turns ratio. Similarly, only the power transmission within the first half of the switching period $[t_0, t_4]$ will be analyzed below.

Assuming that the transmission efficiency of the converter is 100%, the total power P_{tot} of $[t_0$ and $t_4]$ can be expressed as

$$P_{tot} = \frac{2}{T_s}\frac{V_o}{2}\int_{t_0}^{t_4} i_{DR1}dt = \frac{V_o}{T_s}\int_{t_0}^{t_3} i_{DR1}dt \quad (8)$$

where T_s = $1/f_s$ is the switching period.

Similarly, the transmission power of T_{r1} is

$$P_1 = \frac{2}{T_s}\frac{V_{in}}{2}\int_{t_0}^{t_4} i_{p1}dt = \frac{V_{in}}{T_s}\int_{t_0}^{t_3} i_{p1}dt \quad (9)$$

According to $i_{p1} = N_1 i_{DR1}$, P_1 can also be expressed as

$$P_1 = \frac{N_1 V_{in}}{T_s}\int_{t_0}^{t_3} i_{DR1}dt \quad (10)$$

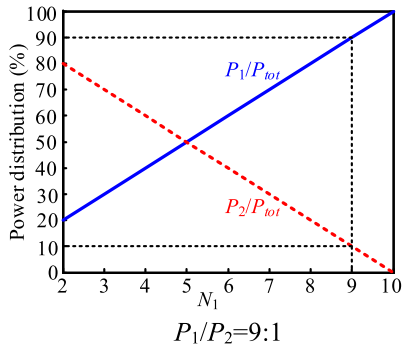

Fig. 6. Power distribution versus N_1.

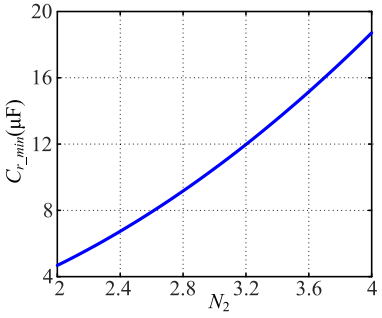

Fig. 7. Relationship of C_r and N_2 when N_1 = 9.

By (8) and (10)

$$\frac{P_1}{P_{tot}} = \frac{N_1 V_{in}}{V_o} \tag{11}$$

According to the conservation theory of energy, the transmission power of T_{r2} is

$$P_2 = P_{tot} - P_1 \tag{12}$$

By (10) and (12)

$$\frac{P_1}{P_2} = \frac{P_1}{P_{tot} - P_1} = \frac{N_1 V_{in}}{V_o - N_1 V_{in}} \tag{13}$$

From (13) that when the input and output voltages are determined, the ratio of the transmission power of the two transformers is only related to $P_1/P_2 N_1$. According to the parameters given at the beginning of this section, P_1 and P_2 are plotted in relation to P_{tot}, respectively, as shown in Fig. 6. It can be seen that as N_1 increases, P_1/P_{tot} increases, and P_2/P_{tot} decreases, which means that N_1 should be designed to be large enough to ensure that T_{r1} transmits much more power than T_{r2}. Without loss of generality, when N_1 takes 9, there are P_1/P_{tot} = 90%, P_2/P_{tot} = 10%, and P_1/P_2=9:1

Moreover, the losses in the transformer tr1 and tr2 depend on the power-sharing. The high power-sharing transformer suffers higher power losses, and low power-sharing transformer possesses lower power loss. Mostly the power loss in the transformer is due to higher frequency switching of switches. In this case, the t_{r1} share most of the power; therefore, the power-sharing is higher in t_{r1} in comparison to t_{r2}.

As you can see from Fig. 5, the origin of the axis θ is between θ_1 and θ_2, so

$$(N_1 V_{in} - V_o)/2 < 0 < (N_1/2 + N_2/4) V_{in} - V_o/2 \tag{14}$$

That is, N_1 and N_2 should be satisfied

$$\begin{cases} N_1 < V_o/V_{in} \\ N_2 > 2\,(V_o/V_{in} - N_1) \end{cases} \tag{15}$$

Therefore, when $N_1 = 9$, the N_2 should be greater than 2.

3.2. Resonant capacitor C_r

During $[t_0, t_4]$, the output power P_0 can be expressed as

$$\begin{aligned} P_o &= 2f_s\,(V_o/2) \int_{t_0}^{t_4} i_s\,(t)\,dt \\ &= 2f_s\,(V_o/2) \left(\int_{t_1}^{t_2} i_s\,(t)\,dt + \int_{t_2}^{t_3} i_s\,(t)\,dt \right) \end{aligned} \tag{16}$$

Substituting (6) and (7) into the above formula is available

$$\begin{aligned} P_o &= 2f_s\,(V_o/2)\left(C_r/N_2^2\right)(r_1 + r_2 - N_2 V_{in}/4) \\ &= 2f_s V_o C_r \Delta v_{Cr\_s}/N_2^2 \end{aligned} \tag{17}$$

According to the state analysis in mode 4, we should know that v_{Cr} should be satisfied.

$$\Delta v_{Cr} = V_{Crmax} < (N_1 V_{in} + V_o)/(2N_2) \tag{18}$$

Due to $\Delta v_{Cr\_s} = N_2 \Delta v_{Cr}$, C_r and substitution (17)

$$C_r > \frac{N_2^2 P_o}{f_s V_o (N_1 V_{in} + V_o)} = C_{r\_min} \tag{19}$$

Where C_{r_min} is the lower limit value to be considered when designing C_r.

Based on the given converter parameters, $N_1 = 9$ should be drawn in Fig. 7. It is obvious that for the proper operation of the converter, C_{r_min} increases with the increase of N_2.

3.3. Resonant inductor L_r

When the converter operates on the critical current continuous mode, the $t = t_3$-t_0 is just equal to the half of the switching period and neglects the time of mode 1.

$$t_3 - t_1 = (\theta_1 + \theta_2)/\omega_r \le \frac{T_s}{2} \tag{20}$$

With (1) and (20) L_r needs to satisfy

$$L_r \le \frac{N_2^2}{4 f_s^2 N_1^2 C_r (\theta_1 + \theta_2)^2} = L_{r\_max} \tag{21}$$

Among them, L_{r_max} is the upper limit to be considered when designing L_r.

3.4. Optimal design of N_2 and C_r

For high-power applications, the switching loss of power devices generally accounts for a substantial part of whole losses, and then the conduction loss. According to Table 1, although ZVS can be achieved by MOSFETs Q_5 and Q_6, the switching loss of the proposed converter is mainly generated when they are turned off. Hence, the switching loss is strongly determined by the turn-off current I_{off} of Q_5 and Q_6. Furthermore, I_{peak1} and I_{peak2}, as the peak currents of i_{p1} and i_{p2}, respectively, will affect the power devices' conduction loss and transformer loss, and high peak currents will penalize the selection of power devices. Hence, in this subsection, the optimal design of N_2 and C_r will be discussed to get a reasonable peak and turn-off currents to improve the converter performance (see Eq. (22) in Box II).

I_{off} can be achieved through the ordinate y(B_1) of node B_1 in Fig. 5, so that mode 3 (3) and (5) can be obtained (22). Considering the lower bound C_{r_min} of C_r value, according to (22), Fig. 8 (where L_r takes its upper limit value L_{r_max}), it can be seen that Q_5 and $Q_6 I_{off}$ decreases rapidly with the decrease of N_2, while I_{off} decreases very slightly with the decrease in C_r. Hence, I_{off} is mainly affected by N_2, implying that N_2 should be designed to be as small as possible to obtain lower switching loss.

$$I_{off} = N_2 \frac{y(B_1)}{Z_r} = \frac{\sqrt{C_r/L_r}}{N_1} \sqrt{\left(\frac{N_1 V_{in}}{2} - \Delta v_{Cr} N_2 - \frac{V_o}{2}\right)^2 - \left[\frac{\Delta v_{Cr}\,(4V_o - (4N_1 + N_2)\,V_{in})}{V_{in}} - \left(\frac{N_1 V_{in}}{2} - \frac{V_o}{2}\right)\right]^2} \tag{22}$$

Box II.

As can be seen from Fig. 5, the maximum value of Z_{ris} is related to the position of node B_1 and the size of θ_1 and θ_2. For example, when the node B_1 is in the first quadrant since the center θ_2 is on the negative half axis, θ_2 is less than $\pi/2$. While the center θ_1 is on the positive half axis, it may be on the left or right of the mapping point X (the mapping of the node B_1 on the horizontal axis). Obviously, when the center θ_1 is on the left of the mapping point X, θ_1 is greater than $\pi/2$, the maximum value of Z_{ris} is the radius r_1; when the center θ_1 is on the right of the mapping point X, θ_1 is smaller than $\pi/2$, and the maximum value of Z_{ris} is the ordinate $y(B_1)$ of the node B_1. Similarly, when the node B_1 is in the second quadrant, the maximum value of Z_{ris} can be obtained according to the size of θ_2 and $\pi/2$. Under the same parameters, when the maximum value of Z_{ris} is determined, the peak of i_s also determined, and I_{peak1} and I_{peak2} are also determined, i.e. (23).

$$I_{peakj} = \begin{cases} N_j r_1 / Z_r & x > 0 \,\&\, \theta_1 \geq \pi/2 \\ N_j r_1 \sin\theta_1 / Z_r & x > 0 \,\&\, \theta_1 < \pi/2 \\ N_j r_2 / Z_r & x < 0 \,\&\, \theta_2 \geq \pi/2 \\ N_j r_2 \sin\theta_2 / Z_r & x < 0 \,\&\, \theta_2 < \pi/2 \end{cases} j = 1,\ 2 \tag{23}$$

According to the detailed modal analysis in the previous section, the four IGBTs ($Q_1 \sim Q_4$) have the same current peak I_{peak_IGBT} and are the sum of I_{peak1} and I_{peak2}. The two MOSFETs (Q_5 and Q_6) also have the same current peak I_{peak_MOS} and I_{peak2}. Therefore, according to (4), (6) and (23), Fig. 9(a) and (b) it can be seen that both I_{peak_IGBT} and I_{peak_MOS} decrease rapidly with the decrease in N_2, but only show a slight decrease with the decrease in C_r. Therefore, similar to I_{off}, the size of I_{peak_IGBT} and I_{peak_MOS} is mainly affected by the influence of N_2. From the perspective of reducing the peak current to facilitate switching selection, the smaller N_2 should also be chosen. Although the decrease of C_r is beneficial to reduce the peak current and turn off current of the converter, the peak value of the resonant voltage Δ_{vCr} is also changed with the change of C_r and N_2, and the magnitude of the Δ_{vCr} is also related to the selection of the voltage resistance of the resonant capacitor. For this reason, the change in Δ_{vCr} should also be considered, as shown in Fig. 10. It can be seen from the figure that Δ_{vCr} decreases with the decrease of N_2 but increases rapidly with the decrease of C_r. The higher the voltage of the capacitor, the larger the volume, and the higher is the cost. Therefore, from the perspective of resonant capacitor selection, we should still choose a smaller N_2, and C_r should be designed slightly larger.

In addition, the change curve of L_{r_max} is shown in Fig. 11. Similar to Δ_{vCr}, L_{r_max} decreases as N_2 decreases but increases rapidly as C_r decreases. In general, the small inductor has a relatively small volume and loss. Therefore, from the perspective of designing the resonant inductor, the smaller N_2 should still be selected, and C_r should be designed to be slightly larger.

In summary, the smaller N_2 is, the smaller the peak current and the turn-off current of the switch, the peak resonant voltage, and the resonant inductance, and the reduction of C_r is beneficial to reduce the peak current and the turn-off current of the converter, but it will make the peak value of the resonant voltage and the value of the resonant inductor increase rapidly. Therefore, N_2 should be designed as small as possible under the premise of satisfying (15), and the value of Cr should be taken into consideration.

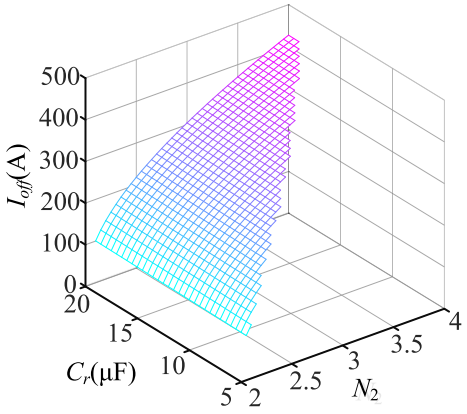

Fig. 8. Graph of I_{off} with different N_2 and C_r.

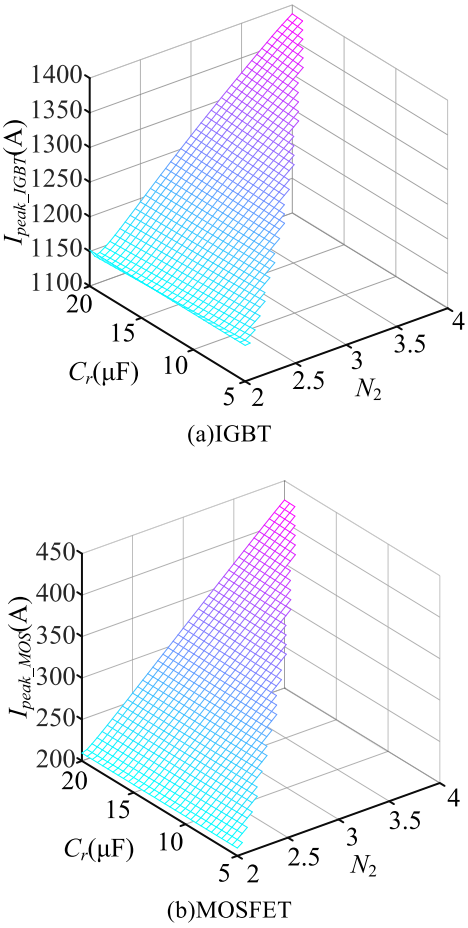

Fig. 9. Graphs of current peak of switches with different N_2 and C_r.

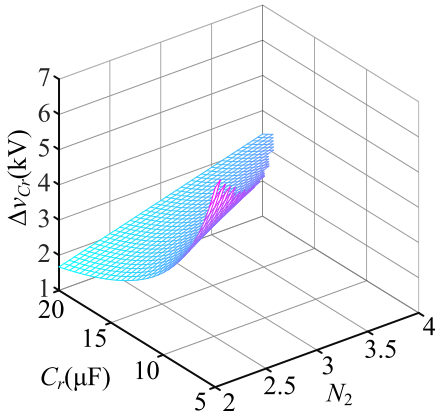

Fig. 10. Graph of Δv_{Cr} with different N_2 and C_r.

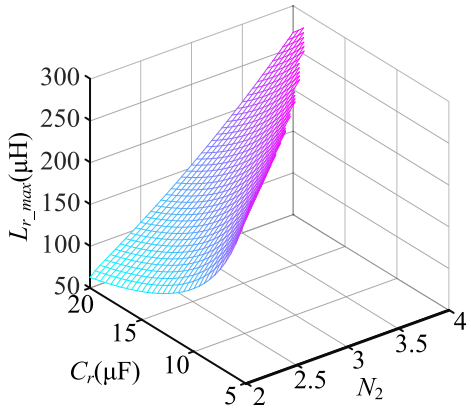

Fig. 11. Graph of L_{r_max} with different N_2 and C_r.

Table 2
Main platform parameters.

Rated power P_N	2000 W
Output power P_o	1900 W
Input voltage V_{in}	300 V
Output voltage V_o	1500 V
Switching frequency f_s	10 kHz
Main transformer turn ratio N_1	4.5
Auxiliary transformer turn ratio N_2	1.2
Resonant InductorL_r	15 μH
Resonant capacitor C_r	2 μF

4. Experimental results

Based on the above theoretical analysis, and to further verify the working principle and performance of the proposed converter, a set of the small-power experimental platform was built. The main parameters are shown in Table 2. In order to ensure that the converter operates in the discontinuous current mode, the actual transmitted power P_o of the converter is slightly less than the rated power P_N.

From Fig. 12, v_{AB}, v_{AC}, the primary side current waveform of two transformers, and the resonant capacitor voltage v_{Cr}. It can be seen that the amplitude of v_{AB} is 150 V, which is 1/2 of the input voltage. The v_{AC} has a small spike at the beginning of each half-switching period, and the amplitude at the moment before the MOSFET transistors Q_5 and Q_6 turn off is 75 V, and only 1/4 of the input voltage, which is consistent with the theoretical analysis. Additionally, v_{Cr} is at a minimum at the beginning of each switching cycle and reaches a maximum after half a resonant switching cycle. It should be noted that the two transformer

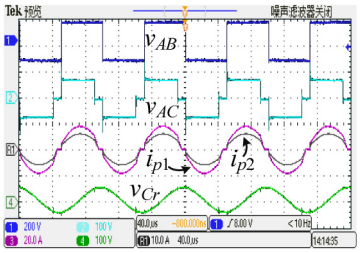

Fig. 12. Waveforms of v_{AB}, v_{AC}, i_{p1}, i_{p2} and v_{Cr}.

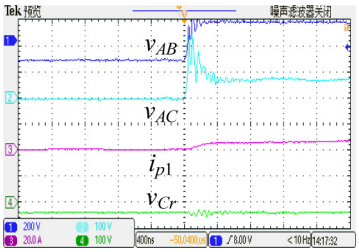

Fig. 13. Zoomed in switching cycle starting.

primary currents i_{p1} and i_{p2} have a relatively fast rising process at the beginning of each half of the switching cycle. This process corresponds to mode 1, that is, L_r is resonant with the parasitic capacitance of C_r and Q_6 in which the parasitic capacitance of Q_6 is much smaller than C_r, resulting in a smaller resonant cycle of mode 1, and therefore there is a phenomenon that a small current quickly rises, as shown in Fig. 13.

As shown in Figs. 14 and 15, the maximum blocking voltage required for the switches Q_1 and Q_2 are only 1/2 of the input voltage, and both Q_1 and $Q2$ can achieve good ZCS turn-off. Also, due to the presence of mode 1, the current starting point of Q_1 and Q_2 has a more rapid rise. According to converter mode 2 current path, as shown in Fig. 3(b), it is known that the current flowing through Q_1 and Q_2 is the sum of both I_{P1} and I_{P2} in the phase of the resonance current rising, so its peak is slightly larger than the peak of I_{P1} in Fig. 12.

Fig. 16 shows the driving, voltage, and current waveforms of Q_5. It is obvious that the peak voltage of Q_5 is 75 V, with only 1/4 of the input voltage. In addition, before opening Q_5, the voltage has always been zero, and its current has also decreased to zero. Therefore, Q_5 achieves the opening of ZVZCS. Because Q_5 has a turn-off the current, it has enough energy to complete the charge and discharge of the parasitic capacitances of Q_5 and Q_6 to achieve its ZVS turn-off, as shown in Fig. 17.

The steady state trajectories of the experimental platform are shown in Fig. 18. The nodes of each mode can also be clearly distinguished from the diagram, as shown in Fig. 5. According to the steady state trajectories, the switching current and the capacitive voltage of the converter can be determined in different parameters, and the two nodes are corresponding to the nodes B_1 and A_2, respectively. Finally, the efficiency curve of the experimental platform is given, as shown in Fig. 19. It can be seen that the transmission efficiency of the converter decreases as the load becomes lighter, and the conversion efficiency of the converter is more than 96% in a wide range of loads.

5. Conclusion

In this paper, a hybrid resonant three-level converter based on double transformers working in the discontinuous current mode is proposed. It mainly includes a basic three-level circuit and auxiliary circuit. By rationally designing the boost ratio of the main

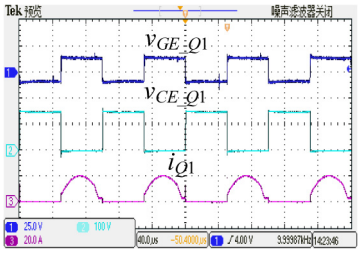

Fig. 14. Waveforms of v_{GE} of Q_1, v_{CE} of Q_1, and current of Q_1.

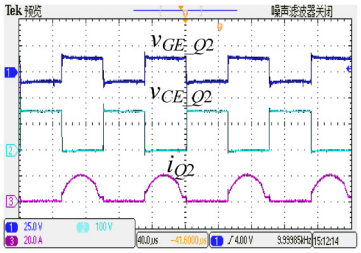

Fig. 15. Waveforms of v_{GE} of Q_2, v_{CE} of Q_2, and current of Q_2.

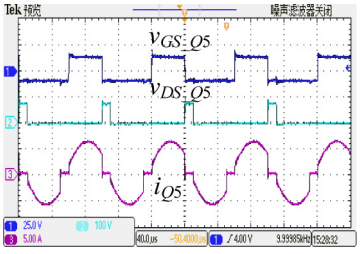

Fig. 16. Waveforms of v_{GS} of Q_5, v_{DS} of Q_5, and current of Q_5.

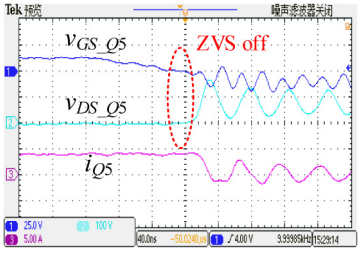

Fig. 17. Zoomed in turn-off waveforms of Q_5.

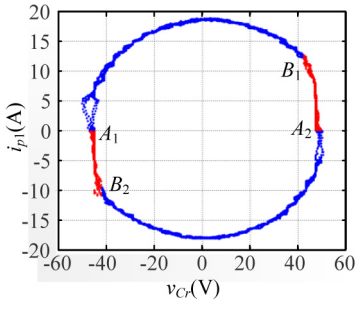

Fig. 18. Experimental steady-state trajectory path.

transformer, the basic three-level circuit transmits most of the power. The power and voltage regulation of the entire converter can be achieved by only chopper control of the auxiliary circuit,

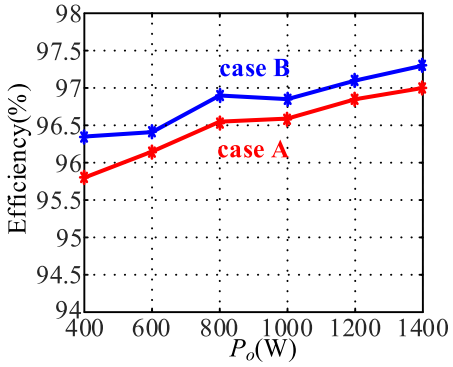

Fig. 19. Efficiency curve.

and the 4 switches based on three-levels are completely liberated, so that they work in the fixed duty ratio mode and the control is simple. At the same time, zero-current switching on and off of the switches is realized, and the switching loss is significantly reduced. The design of the auxiliary transformer's boost ratio is as small as possible. It helps to reduce the peak current of all switch tubes, the closing current of the two control switches, the peak resonant voltage, and the resonant inductance value, which can further reduce the loss and facilitate the resonant capacitor and the design of the resonant inductor. Finally, the experimental results verify the superior performance of the proposed converter and prove the correctness of the above conclusions.

CRediT authorship contribution statement

Syed Waqar Azeem: Conception and design of study, Drafting and revision of manuscripts. **Kashif Mehmood:** Problem formulation, Acquisition of data, Results simulation, Drafting and revision of manuscripts. **Khalid Mehmood Cheema:** Conception and design of study, Drafting and revision of manuscripts. **Ahmed M. El-Sherbeeny:** Problem formulation, Acquisition of data, Results simulation, Drafting and revision of manuscripts.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

Boroyevich, D., Cvetkovic, I., Dong, D., et al., 2010. Future electronic power distribution systems:a contemplative view. In: 2010 12th International Conference on Optimization of Electrical and Electronic Equipment. IEEE, Basov, Russia, pp. 1369–1380.

Cheema, Khalid Mehmood, 2020. A comprehensive review of virtual synchronous generator. Int. J. Electr. Power Energy Syst. 120, 106006.

Cheema, Khalid Mehmood, Mehmood, Kashif, 2019. Improved virtual synchronous generator control to analyse and enhance the transient stability of microgrid. IET Renew. Power Gener. 14 (4), 495–505.

Chen, W., Huang, A., Li, C., et al., 2013. Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems. IEEE Trans. Power Electron. 28 (4), 2014–2023.

Gkoutioudi, E., Bakas, P., Marinopoulos, A., 2013. Comparison of PV systems with maximum DC voltage 1000V and 1500V. In: IEEE Photovoltaic Specialists Conference (PVSC), pp. 2873–2878.

Hu, Runqing, Liu, Jiandong, 2017. Review and prospect of photovoltaic power market in 2017. Sol. Energy 2018 (01), 14–18.

Jiang, Daozhuo, Zheng, Huan, 2012. Research status and developing prospect of DC distribution network. Autom. Electr. Power Syst. 36 (8), 98–104.

Kakigano, H., Miura, Y., Ise, T., 2010. Low-voltage bipolar-type DC microgrid for super high quality distribution. IEEE Trans. Power Electron. 25 (12), 3066–3075.

Liu, Jilong, Xiao, Fei, Chen, Wei, et al., 2014. Research on a novel control scheme for three-level full-bridge converter. Proc. CSEE 34 (33), 5854–5860.

Liu, Guowei, Zhao, Yuming, Yuan, Zhichang, et al., 2016. Application framework of VSC medium-voltage DC distribution technology in shenzhen power grid. Southern Power Syst. Technol. 10 (4), 1–7.

Mura, F., W. De Doncker, Rik, 2011. Design aspects of a medium-voltage direct current (MVDC) grid for a university campus. In: Proceedings of the 8th International Conference on Power Electronics and ECCE Asia. IEEE, Jeju, pp. 2359–2366.

Ning, G., Chen, W., Shu, L., et al., 2017a. Hybrid resonant ZVZCS PWM full-bridge converter for large photovoltaic parks connecting to MVDC grids. IEEE J. Emerg. Sel. Top. Power Electron. 5 (3), 1078–1090.

Ning, G., Chen, W., Shu, L., et al., 2017b. A hybrid ZVZCS dual-transformer-based full-bridge converter operating in DCM for MVDC grids. IEEE Trans. Power Electron. 32 (7), 5162–5170.

Ruan, X., Chen, Z., Chen, W., 2005. Zero-voltage-switching PWM hybrid full-bridge three-level converter. IEEE Trans. Power Electron. 20 (2), 395–404.

Sheng, Wanxing, Li, Rui, Li, Yue, et al., 2016. A preliminary study on voltage level sequence and typical network architecture of direct current distribution network. Proc. CSEE 36 (13), 3391–3403+3358.

Song, Qiang, Zhao, Biao, Liu, Wenhua, et al., 2013. An overview of research on smart DC distribution power network. Proc. CSEE 33 (25), 9–19.

Yin, Z., Hu, J., Chung, H., et al., 2016. A ZCS-PWM voltage-driven three-level converter with a secondary-side simple soft-switching snubber. IEEE Trans. Ind. Electron. 63 (12), 7542–7552.

Yu, Shiyao, 2017. Research on the Control Strategy of Neutral Point Voltage Fluctuation in Three-Level Neutral-Point-Clamped Converter. Beijing Jiaotong University.

Zhang, Yuanyuan, Ruan, X.I.nbo, 2004. A novel control strategy for the flying capacitor voltage of the multilevel converter. Proc. CSEE (08), 37–41.