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Decreasing the frequency of HVDC commutation failures caused by harmonics

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Abstract: Commutation failure, primarily caused by voltage drops and distortion, may lead to high-voltage direct current (HVDC) power interruption and AC system oscillation. To date, there have been few studies on the mechanism and prevention of commutation failure based on voltage distortion caused by harmonics. This study analyses the influence of harmonic voltage on commutation failure based on voltage time area and proposes a method for quantitative analysis of harmonic effects. The analysis shows that limiting the DC current is an effective method to mitigate commutation failure caused by harmonics. A voltage distortion-dependent commutation failure prevention strategy is proposed, and the controller is applied on the inverter side. The selection of parameters is based on the influence of various harmonic orders. The validity and effectiveness of the proposed methods are verified by simulations, which show that voltage distortion-dependent commutation failure prevention strategy can improve the DC system recovery characteristics and suppress subsequent commutation failure caused by harmonics.

1 Introduction

With the advantage of economical operation and high controllability, high-voltage direct current (HVDC) has been widely used in the field of long-distance transmission [1, 2]. Currently, hundreds of HVDC have been put to use in the world, and China is expected to have 38 HVDC by 2020. Consequently, many heavy load areas will form a pattern of multi-infeed HVDC, such as eastern and southern China.

As the most common faults in HVDC systems, commutation failures (CFs) can lead to temporary interruption of transmitted power and stressing the converter equipment [3]. Short-time CFs can produce large power and voltage fluctuations, while long-time and continuous CF may cause HVDC blocking [4]. There have been many studies related to the factors influencing CF and preventive measures.

Thio *et al.* [5] analysed the mechanism of CF and proposed a voltage-time area method. The analysis shows that the fundamental reason for CF is that the commutation voltage-time area cannot meet the demand of the DC current. Further simulation analysis was carried out in [6], based on [5]. Short-circuit capacity can be used to identify the HVDC immunity ability of CF [7]. Actually, the DC current could rise to over 1.5 times the rated value under AC system faults, hence using only the voltage drop for analysis may cause large errors. A method was proposed to determine whether CF occurs based on the voltage drop and DC current in [8].

Although CF can never be completely avoided, many methods, including firing angle and DC current setting controllers, have been proposed to prevent it as much as possible and obtain good results in some situations. Zhang and Dofnas [9] proposed commutation failure prevention (CFPREV), which could immediately advance the firing angle when AC side faults are detected. An improved strategy of control system based on CFPREV has been proposed and shows better results [10]. These methods can effectively prevent CF, but sometimes result in negative impacts of reducing the recovery speed and enlarging the reactive power demand because the firing angle is advanced [11]. The supply voltage is continuously monitored and the dangerous voltage is calculated to ensure if it is necessary to advance the firing pulses in [12]. An improved VDCOL control strategy is presented to cooperate with the advancing firing angle control to mitigate CF in [8], which could decrease the frequency of CF under AC system single-phase and three-phase faults.

The methods above are mostly based on the reduction of fundamental voltage. The application of power electronic devices and the saturation of the converter transformers [13] could produce a large number of harmonics, which may cause CF and harmonic instability in severe situations [14, 15]. When an HVDC system is in unipolar-earth operating condition, it is more likely to result in voltage distortion with converter transformer excitation current injection and an increased risk of CF [16]. The harmonics, especially low-order ones, are important reasons that remote CFs can be caused by local faults [17]. The simulation analysis in [17] shows that the dominant cause of CF for a remote converter at low local fault levels is the distortion of the voltage waveform. However, for more severe faults, although there is less distortion, a sudden reduction in the magnitude of the fundamental voltage is the primary cause of CF. The authors in [18, 19] reported two CFs caused by voltage distortion in a practical power system based on transient fault recorder data.

This paper analyses the mechanism of the influence of harmonic voltage on CF based on voltage time area and proposes a practical method for quantitative analysis of harmonic effects. A voltage distortion-dependent CF prevention (VDDCFP) controller is proposed and applied on the inverter side to decrease the frequency of CF caused by harmonics. The calculation of parameters is based on the influence of various harmonic orders. PSCAD simulations are used to prove the validity of the proposed analytical method and VDDCFP strategy.

2 Harmonic effect on the commutation process

2.1 Harmonic effect on the commutation process

As shown in Fig. 1, the basic module of the HVDC converter is a three-phase full-wave bridge circuit. The bridge consists of thyristors V_{T1}–V_{T6}, the necessary turn-off condition of which is that the current must be lower than the maintenance current. The

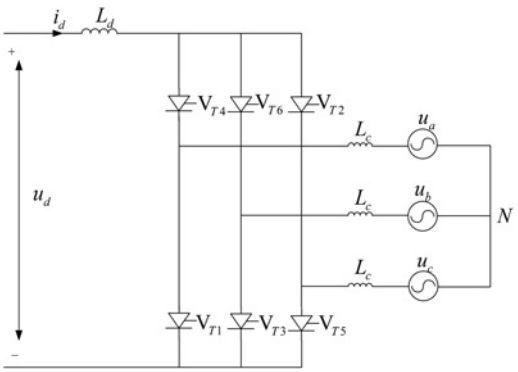

Fig. 1 *Equivalent circuit of three-phase full-wave bridge converter*

commutation process starts from the trigger delay angle ($\omega t = \alpha$) and ends with the advanced angle of extinction ($\omega t = \alpha + \mu$, where μ is the overlap angle). The commutation margin is the extinction angle (γ).

Fig. 2 is the equivalent circuit of commutation from V_{T4} to V_{T6}. The circuit can be described as

$$L_c \frac{\mathrm{d}i_1}{\mathrm{d}t} + U_a = L_c \frac{\mathrm{d}i_2}{\mathrm{d}t} + U_b \tag{1}$$

where i_1 and i_2 are the currents flowing through valves 4 and 6, respectively. I_d denotes the DC current. Because $i_1 + i_2 = I_d$, (1) can be rewritten as

$$U_{ab} = L_c \frac{\mathrm{d}(I_d - i_1)}{\mathrm{d}t} - L_c \frac{\mathrm{d}i_2}{\mathrm{d}t} = -2L_c \frac{\mathrm{d}i_1}{\mathrm{d}t} \tag{2}$$

During the process from valves 4 to 6, i_1 approaches 0 from I_d. (2) can be written as (3) after the definite integral. The upper limit of the integral is the end moment t_1 ($t_1 = (\alpha + \mu)/\omega$ of the commutation process, while the lower limit of the integral is the initial moment t_0($t_0 = \alpha/\omega$).

$$I_d = \int_{t_0}^{t_1} -\frac{U_{ab}}{2L_c}\mathrm{d}t \tag{3}$$

2.2 Commutation process considering harmonics

When the system has a harmonic injection or the converter transformer is saturated, the inverter bus voltage will be distorted. Considering the n-order harmonic voltage, the line–line voltage

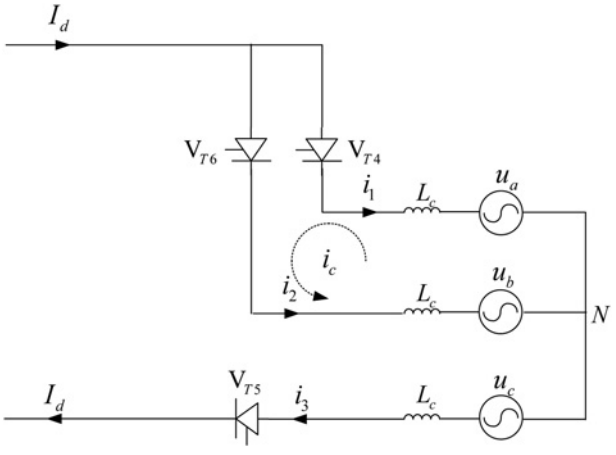

Fig. 2 *Equivalent circuit of commutation process*

can be written as.

$$U_{ab} = E_1 \sin(\omega t) + \sum_{n=2}^{N} E_n \sin(n\omega t + \varphi_n) \tag{4}$$

where E_n is the n-order harmonic voltage amplitude and φ_n is the phase. Substituting (4) into (3), (3) can be written as

$$\begin{aligned} I_d &= \int_{t_0}^{t_1} -\frac{E_1 \sin(\omega t) + \sum_{n=2}^{N} E_n \sin(n\omega t + \varphi_n)}{2L_c}\mathrm{d}t \\ &= \int_{t_0}^{t_1} -\frac{E_1 \sin(\omega t)}{2L_c}\mathrm{d}t + \sum_{n=2}^{N}\int_{t_0}^{t_1} -\frac{E_n \sin(n\omega t + \varphi_n)}{2L_c}\mathrm{d}t \end{aligned} \tag{5}$$

where $\sum_{n=2}^{N}\int_{t_0}^{t_1} -((\mathrm{E}_n \sin(n\omega t + \varphi_n))/2L)\mathrm{d}t$ is the superposition of all harmonic orders. To avoid CF, (6) must be satisfied.

$$\omega t_1 = \alpha + \mu \le 180^\circ - \gamma_{\min} \tag{6}$$

The critical extinction angle $\gamma_{\min}$ depends on the physical characteristics of the thyristor. In this study, 7° is ordinarily appropriate as a minimum extinction angle for a 50-Hz system. If (5) is not satisfied, that is, the voltage-time area is lower than I_d at the critical moment of t_1, valve 4 will continuously conduct and CF will occur, as (7) shows.

$$I_d > \int_{t_0}^{t_1} -\frac{E_1 \sin(\omega t)}{2L_c}\mathrm{d}t + \sum_{n=2}^{N}\int_{t_0}^{t_1} -\frac{E_n \sin(n\omega t + \varphi)}{2L_c}\mathrm{d}t \tag{7}$$

where $t_0 = \alpha/\omega$, $t_1 = (\pi - \gamma_{\min})/\omega$. Therefore, to commutate successfully, the impact of $\sum_{n=2}^{N}\int_{t_0}^{t_1} -((E_n \sin(n\omega t + \varphi_n))/2L_c)\mathrm{d}t$ should be as small as possible.

Fig. 3 shows the inverter commutation process and the effect of a sudden commutating voltage distortion. The required voltage time area depends on $I_d = A = A'$. The harmonic voltage would decrease

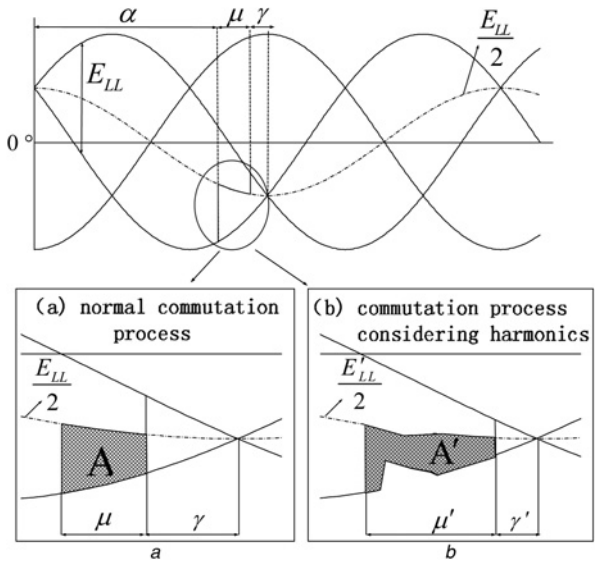

Fig. 3 *Harmonic effect on the commutation process*

a Normal commutation process
b Commutation process considering harmonics
E_{LL} = Line-to-line commutation voltage
E'_{LL} = Line-to-line commutation voltage with harmonics
α = firing angle of the valves
γ = normal extinction angle
γ' = extinction angle considering harmonics
μ = commutation overlap angle
μ' = commutation overlap angle considering harmonics
A=A' = volt-time area required for the commutation process

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the fundamental voltage time area and force the commutation time to increase. In some severe occasions with large harmonics, γ would be lower than 7°, leading to CF.

The harmonic volt-time area of time n can be written as

$$F_n = \int_{t_0}^{t_1} -\frac{E_n \sin(n\omega t + \varphi_n)}{2L_c} \mathrm{d}t = \frac{E_n \cos(n\pi - n\gamma + \varphi_n) - E_n \cos(n\alpha + \varphi_n)}{2n\omega L_c} \quad (8)$$

It can be seen that the influence of the harmonics is related to the amplitude and phase of the harmonic voltage, harmonic order, and the trigger delay angle α. Considering the worst-case scenario, γ= 7°, (8) can be simplified and written as.

$$F_n = A_n E_n \sin(\theta_n + \varphi_n) \quad (9)$$

where A_n is defined as the harmonic commutation coefficient, $A_\mathrm{n} = \left|\sin(((n\alpha + n\gamma - n\pi)/2))/X_n\right|$, θ_n is an additional angle for the simplification process, and X_n is the n-order harmonic impedance. The significance of A_n is the worst influence of the n times harmonic on the commutation process, which depends on the normal operating parameter of α and the harmonic order.

The equivalent circuit is shown in Fig. 1. X_n can be written as $X_n = nX_1$. Supposing $X_1 = 1$ p.u., Fig. 4, which shows the relationship between the harmonic commutation coefficient and harmonic order under various operating values of α, can be obtained. With an increase in the number of harmonics, the harmonic change coefficient decreased because of the increase in harmonic impedance. During the fault time, the low-order harmonic voltage is larger than that of the higher orders because of the saturation of transformers [17]. Therefore, low-order harmonics play an important role in CF caused by voltage distortion.

The harmonic phase is difficult to measure accurately. Neglecting the harmonic phase and supposing $\sin(\theta_n + \varphi_n) = 1$, a more practical formula, which is defined as the harmonic influence coefficient, can be obtained from (9).

$$G_{n1} = \frac{F_n}{F_1} = P_{n1}\frac{E_n}{E_1} \quad (10)$$

where $P_{n1} = A_\mathrm{n}/A_1$. The harmonic influence coefficient G_{n1}, including A_n and the harmonic voltage, reflects the largest influence of the harmonic voltage on the commutation process under the worst phase circumstances.

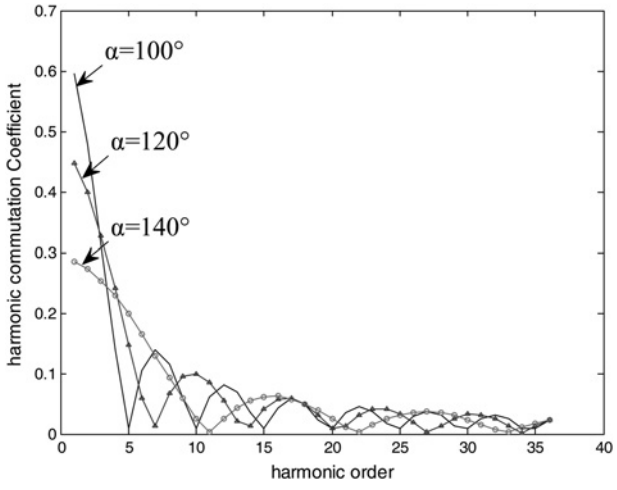

Fig. 4 *Relationship between harmonic commutation coefficient and harmonic order*

2.3 Calculation of volt-time area margin of commutation process

In normal operation, γ at the inverter side is ordinarily working at 15°–20°, with consideration of a sufficient commutation margin and avoiding the consumption of too much reactive power. To commutate successfully, the required voltage-time area is calculated as (11), where I_{dN} is the rated DC current.

$$S_1 = I_{dN} = \int_{\alpha}^{\pi-\gamma} \frac{E_1 \sin(\omega t)}{2L_c} \mathrm{d}\omega t \quad (11)$$

Considering the extreme case where $\gamma_{\min} = 7^\circ$, the voltage time area that the fundamental voltage could offer is shown as.

$$S_2 = \int_{\alpha}^{\pi-\gamma_{\min}} \frac{E_1 \sin(\omega t)}{2L_c} \mathrm{d}\omega t \quad (12)$$

According to (11) and (12), the voltage-time area margin can be calculated as.

$$S_{\mathrm{mN}} = \frac{S_2 - S_1}{S_1} \quad (13)$$

S_{mN} is the voltage time area margin in normal operation. If the negative effect of the harmonic voltage time is larger than S_{mN}, CF is likely to happen. The harmonic voltage time area should be lower than S_{mN} to avoid CF. To be more specific, (14) can be used as a discriminant for CF caused by harmonics.

$$S_{\mathrm{mN}} \le \sum G_{n1} \quad (14)$$

3 Commutation failure prevention method based on harmonic detection

Traditional VDCOL mitigates CF by limiting the DC current when the DC voltage is reduced, without considering the effects of inverter bus harmonics. According to the previous analysis, the influence of the harmonic voltage on the commutation process is embodied in the decrease in the fundamental voltage time area. The required voltage time area depends on the operating DC current I_d. Therefore, CF can be avoided by reducing I_d when the harmonic is detected. This paper designs a VDDCFP method to prevent CF caused by harmonics. According to (15), the output ΔI_d of VDDCFP can increase the commutation margin by reducing the DC current.

$$\begin{cases} I_d = I_{dN} - \Delta I_d \\ S_\mathrm{m} = \dfrac{S_2 + \Delta I_d - S_1}{S_1} > S_{\mathrm{mN}} \end{cases} \quad (15)$$

As Fig. 5 shows, VDDCFP includes four control parts. The detailed procedures of VDDCFP control are as follows.

(i) Monitor three-phase instantaneous voltage and calculate the harmonic voltage.

(ii) Calculate the harmonic distortion rate of different orders according to (16) and take the maximum one of three phases as the feedback signal. The n-time harmonic distortion rate is calculated as follows.

$$D_n = \frac{E_n}{E_1} \times 100\% \quad (16)$$

(iii) Starting module is added after harmonic distortion rate calculation. Only if D_n is larger than the threshold value ABZ_n

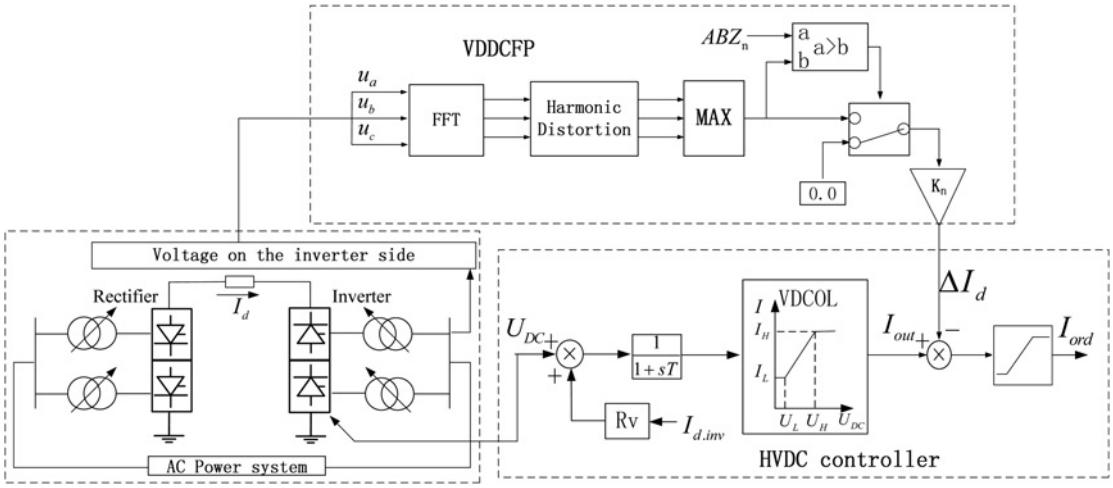

Fig. 5 *Detailed block diagram for VDDCFP*

would VDDCFP start to work. Otherwise, the controller has no output. ABZ_n is calculated from (17) considering different harmonic order effects, and $\sum ABZ_n$ should be lower than the voltage area margin S_{mN} calculated from (13). With the starting module, VDDCFP will not influence normal operation of the HVDC system, even if there is a small voltage distortion. In other words, there is no need to limit DC power if the harmonics are not large enough to lead to a CF.

$$ABZ_n \le \frac{A_n S_{mN}}{\sum A_n} \tag{17}$$

(iv) Thereafter, K_n is the gain of the n-order harmonic. K_n reflects the importance of the n-order harmonic distortion rate on the DC current reference value. If K_n is large, the HVDC would be sensitive to the harmonics and may reduce the transmission power in some unnecessary circumstances. If K_n is small, it cannot achieve the desired decrease in value of the DC current to prevent CF. According to Fig. 4, different harmonic orders have different effects on CF, which can be quantitatively analysed by the harmonic commutation coefficient; low-order harmonics are more likely to lead to CF.

$$\Delta I_d = K_n D_n \ge G_{n1} - S_{mN} \Rightarrow K_n > P_{n1} \tag{18}$$

K_n is determined by P_{n1} and must be larger than P_{n1}, with a certain margin for the signal time delay. The margin is suggested to be 10–30%, depending on the time delay and the CF frequency of various HVDC systems.

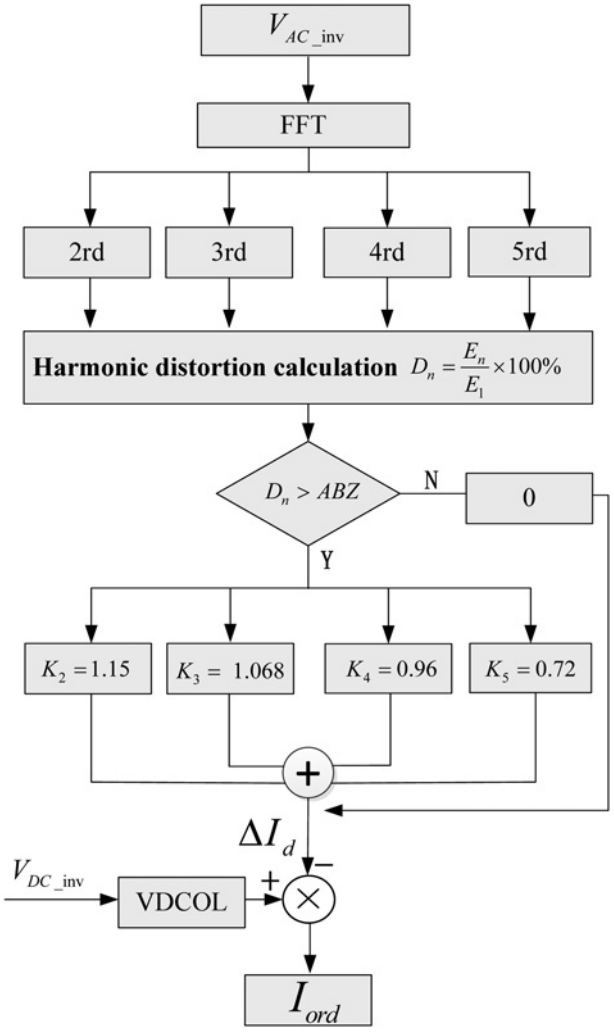

Fig. 6 *Flow chart of VDDCFP controller in simulation model*

4 Case study

4.1 VDDCFP controller design in CIGRE HVDC benchmark model

PSCAD/EMTDC is a specialised software designed mainly for the analysis of high-capacity and high-voltage AC/DC systems. The CIGRE HVDC Benchmark Model [20] is used as the simulation model in this paper. According to the calculation of the harmonic commutation coefficient, low-order harmonics play an important role in CF. The design of VDDCFP in this case takes 2–5-order harmonics into consideration, with 2–5-order harmonic voltages after FFT as the feedback signal. The flow chart of VDDCFP in this case is shown in Fig. 6. The threshold value ABZ_n at rated

Table 1 Calculation of parameters in VDDCFP

Harmonic order	ABZ_n	P_n	K_n
2	0.04	0.9588	1.15
3	0.037	0.89	1.07
4	0.033	0.8	0.96
5	0.029	0.7	0.84

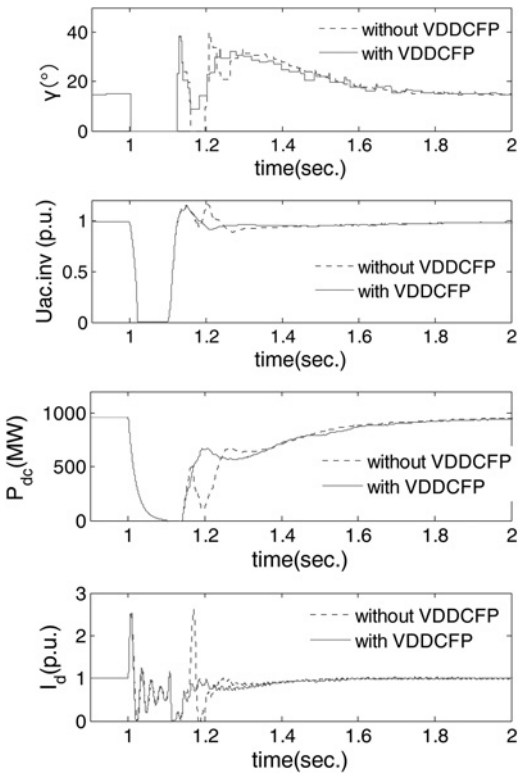

Fig. 7 *System response under three-phase fault (γ is the extinction angle on the inverter side. $U_{ac.inv}$ is RMS voltage of AC system on the inverter side. P_{dc} is the HVDC power transmitted to the AC system. I_d is the Direct current)*

power is calculated by (16), and K_n is determined by P_n with a 20% margin, as shown in Table 1.

4.2 Simulation in CIGRE HVDC benchmark model

(i) *Three-phase fault simulation:* Fig. 7 is the system response under a three-phase metallic short circuit. The fault occurs at 1.0 s and lasts 100 ms. As can be seen, the first CF occurs immediately after fault and lasts almost 0.1 s due to the reduction of AC voltage. A second CF occurs at 1.16 s, and state variables such as the AC voltage and DC current have large fluctuations during the

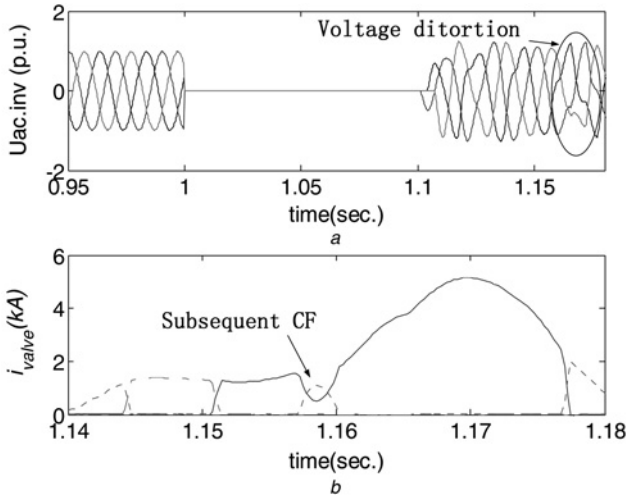

Fig. 8 *Instantaneous three-phase voltage and valve current under three-phase fault without VDDCFP ($U_{ac.inv}$ is instantaneous three-phase voltage of AC system on the inverter side. i_{valve} is the valve current)*

Table 2 Calculation of harmonic influence coefficient in CIGRE HVDC test system

Harmonic order	A_n	E_n	G_{n1}
1	0.284	137	1
2	0.272	23.7	0.166
3	0.253	11.5	0.075
4	0.228	3.08	0.018
5	0.198	1.51	0.008
6	0.164	2.95	0.012
7	0.129	2.34	0.008
sum of (2–7)	–	–	0.287

recovery period after the fault is removed. It is obvious that the three-phase voltage has recovered almost to its rated value, but large distortion is detected as shown in Fig. 8*a* when the second CF occurs as shown in Fig. 8*b*. Therefore, the first CF at 1.0 s is due to the voltage reduction, and the voltage distortion during the recovered period leads to the second CF. The DC current and transmission power could recover to the rated value steadily and effectively with VDDCFP, and the subsequent CF does not occur, as can be seen in Fig. 7.

Table 2 shows the calculation of the harmonic influence coefficient when the subsequent CF occurs. The fundamental voltage has recovered to the rated value, and the DC current is lower than the rated value, but the voltage has a large distortion, as can be seen in Fig. 8 and Table 2. The second harmonic voltage has the largest influence on the commutation process. With an increase in harmonic order, the harmonic influence shows a decreasing trend. However, the sum of the 2–7 harmonic voltage-time areas reach 28.7%, which is far more than the tolerable decreasing area of

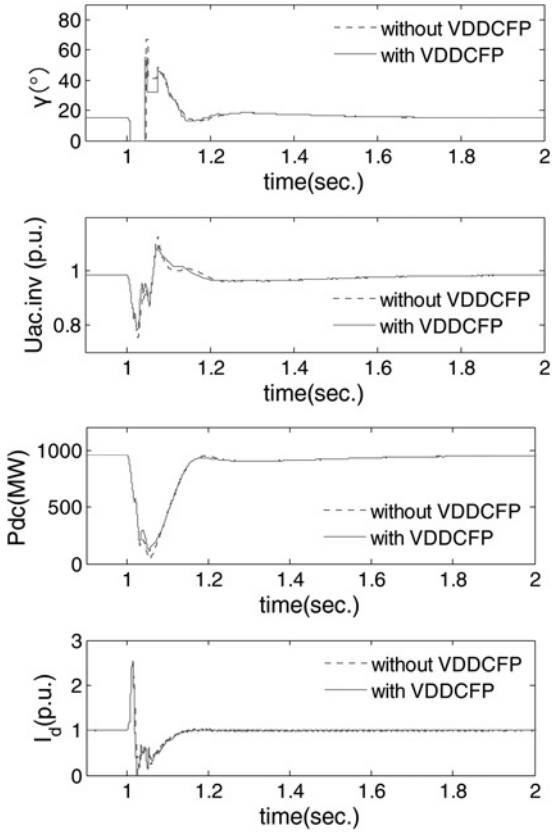

Fig. 9 *System response under single-phase fault (γ is the extinction angle on the inverter side. $U_{ac.inv}$ is RMS voltage of AC system on the inverter side. P_{dc} is the HVDC power transmitted to the AC system. I_d is the direct current)*

Table 3 VDDCFP parameters in 50% DC power conditions

Harmonic order	ABZ_n	P_n	K_n
2	0.3714	0.9799	1.1759
3	0.3714	0.9470	1.1364
4	0.3419	0.9020	1.0824
5	0.3207	0.846	1.0152

13.5% calculated from (13) considering the worst harmonic phase. Therefore, it is not the voltage drop but the voltage distortion causes the subsequent CF during the recovery period.

ii. *Single-phase fault simulation:* Common AC system faults include symmetric and asymmetric faults. To verify the robustness of VDDCFP and its effect on the system response performance after faults, a single-phase fault where $L_f = 0.5$ H, lasting 50 ms, is used. As Fig. 9 shows, although subsequent CF does not occur, the system with VDDCFP improves response performance during the fault. Uac.inv fell more drastically without VDDCFP and reached over 1.1 p.u. after the fault was removed. The response was better with VDDCFP, showing fewer fluctuations and faster recover speed.

iii. *Three-phase fault simulation in reduced power condition:* If the system is in reduced power operating conditions, the immune capacity of CF is increased because the necessary voltage-time area is decreased, according to (7). It is therefore necessary to modify parameters such as I_d and α accordingly for a change of state variables at the inverter. To study the validity of VDDCFP in reduced power operating conditions, 50% P_{dn} is selected as an example. The parameters of the controller are modified according to (17) and (18), as Table 3 shows. Fig. 10 is the system response under a three-phase metallic short circuit in 50% DC power condition. As can be seen, better results are obtained with VDDCFP with respect to the inhibition of subsequent CF caused by harmonics.

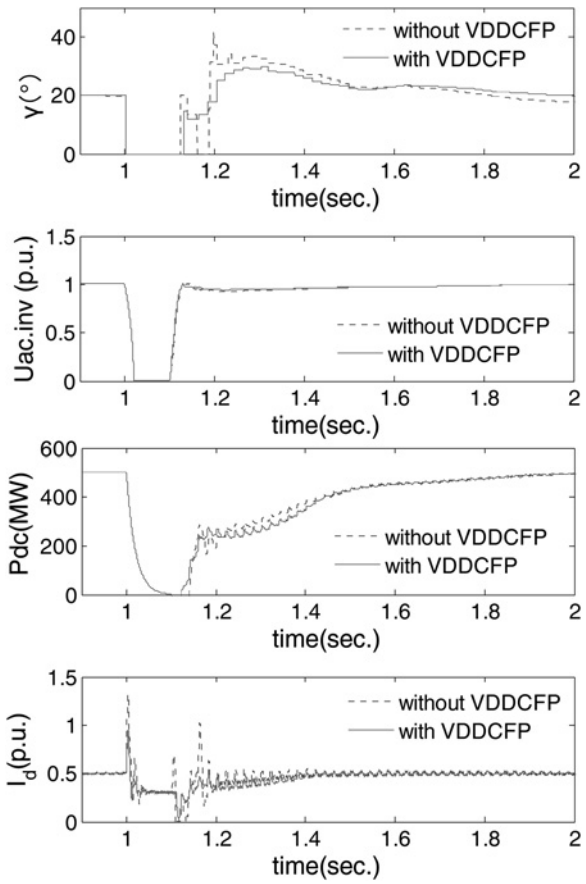

Fig. 10 *System response under three-phase fault in 50% power conditions (γ is the extinction angle on the inverter side. $U_{ac.inv}$ is RMS voltage of AC system on the inverter side. P_{dc} is the HVDC power transmitted to the AC system. I_d is the direct current)*

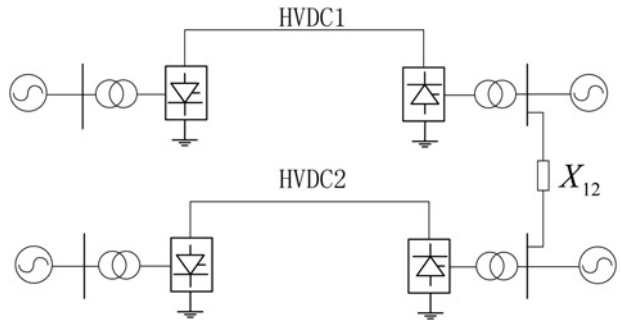

Fig. 11 *Schematic diagram of the typical dual-infeed HVDC test system*

4.3 Simulation in dual-infeed HVDC system based on CIGRE HVDC benchmark model

To verify the effect of VDDCFP on CF caused by harmonics during the recovery period, a typical dual-infeed HVDC system including two equivalent AC sources with their associated impedance based on the CIGRE First HVDC Benchmark model is established, as shown in Fig. 11. The associated impedance is $X_{12} = 0.33\text{H} + 7.5\,\Omega$. VDDCFP is applied on both HVDCs.

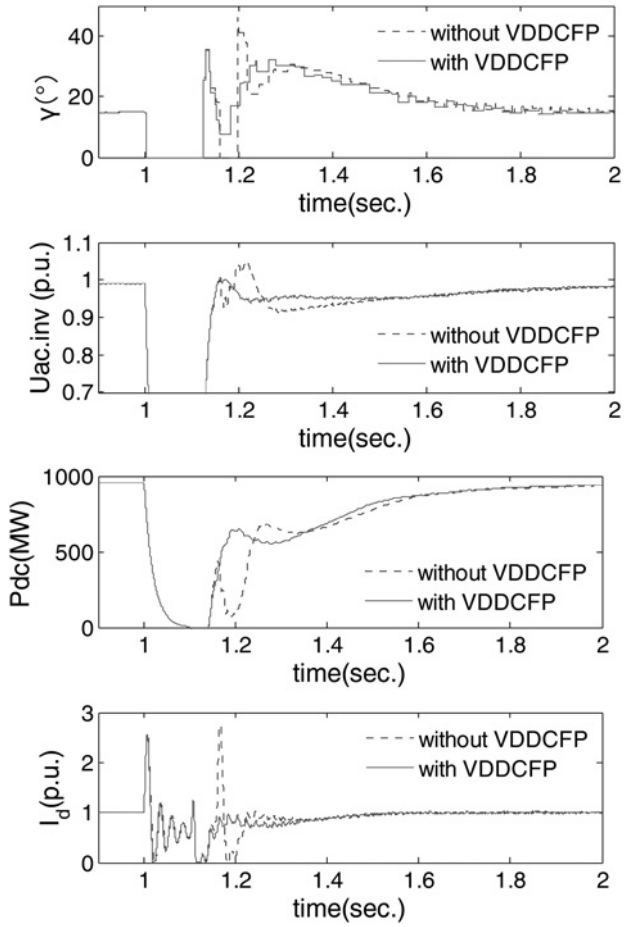

Fig. 12 *Inverter station I responses under single-phase fault in an AC system on the inverter I side (γ is the extinction angle on the inverter side. $U_{ac.inv}$ is RMS voltage of AC system on the inverter side. P_{dc} is the HVDC power transmitted to the AC system. I_d is the direct current)*

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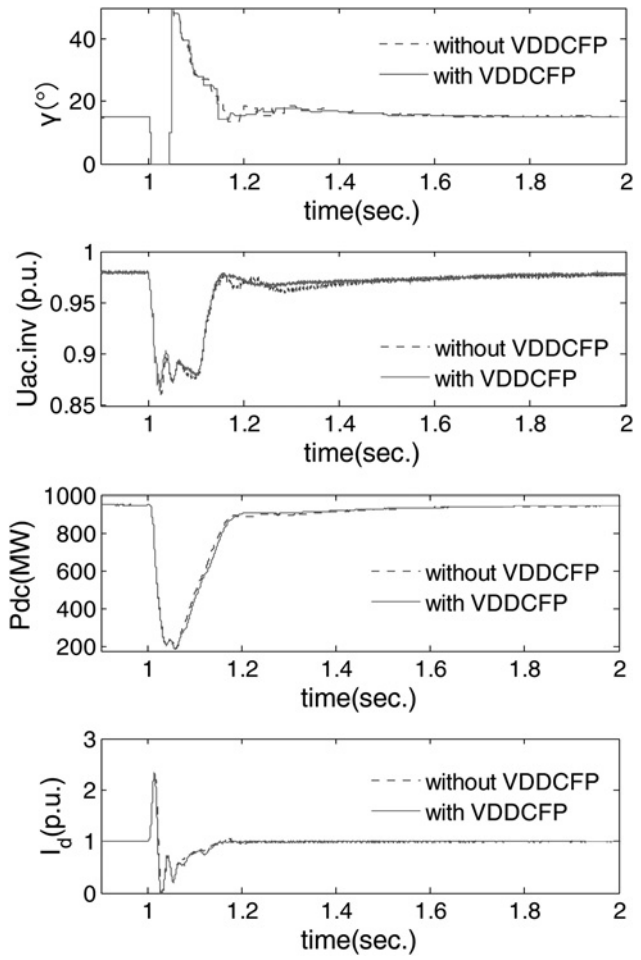

Fig. 13 *Inverter station II responses under single-phase fault in an AC system on the inverter I side (γ is the extinction angle on the inverter side. $U_{ac.inv}$ is RMS voltage of AC system on the inverter side. P_{dc} is the HVDC power transmitted to the AC system. I_d is the direct current)*

Figs. 12 and 13 are the system responses of HVDC1 and HVDC2, respectively, under a three-phase metallic short circuit. The fault occurs on HVDC1 at 1.0 s and lasts 100 ms. The VDDCFP controller can effectively inhibit subsequent CF of HVDC1 and improve the recovery characteristics of HVDC2. The figure of voltage with VDDCFP in Fig. 13 shows less fluctuation and fast speed to the rated value, which is of benefit to the stability of AC system.

Table 4 is a calculation of the harmonic influence coefficient when the subsequent CF occurs. The sum of the 2–7 harmonic voltage-time areas reaches 25.4%, which is larger than the voltage area margin calculated from (13)

Table 4 Calculation of harmonic influence coefficient in dual-infeed HVDC test system

Harmonic order	A_n	E_n	G_{n1}
1	0.284	135	1
2	0.272	17.2	0.122
3	0.253	9.6	0.06
4	0.228	3.2	0.02
5	0.198	3.9	0.02
6	0.164	3.7	0.015
7	0.129	5	0.017
Sum of (2–7)	–	–	0.254

5 Conclusion

In this paper, the mechanism of commutation failure caused by harmonics is analysed. A quantitative method for determining the influence of various harmonic orders on commutation failure is proposed, and the analysis shows that the harmonic amplitude, phase, and harmonic commutation coefficient are important factors leading to commutation failure. During the recovery period of an HVDC after commutation failure, the harmonics of the inverter bus may lead to subsequent commutation failure, and low-order harmonics play a major role. A VDDCFP strategy is proposed in this paper to prevent CFs caused by harmonics. Simulation results show that the proposed method and controller are useful for analysing and preventing CFs caused by harmonics. Moreover, the recovery characteristics are improved with the proposed VDDCFP controller.

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