Hetero-gate-dielectric double gate junctionless transistor (HGJLT) with reduced band-to-band tunnelling effects in subthreshold regime

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Abstract: We propose a hetero-gate-dielectric double gate junctionless transistor (HGJLT), taking high-k gate insulator at source side and low-k gate insulator at drain side, which reduces the effects of band-to-band tunnelling (BTBT) in the sub-threshold region. A junctionless transistor (JLT) is turned off by the depletion of carriers in the highly doped thin channel (device layer) which results in a significant band overlap between the valence band of the channel region and the conduction band of the drain region, due to off-state drain bias, that triggers electrons to tunnel from the valence band of the channel region to the conduction band of the drain region leaving behind holes in the channel.These effects of band-to-band tunnelling increase the sub-threshold leakage current, and the accumulation of holes in the channel forms a parasitic bipolar junction transistor (n–p–n BJT for channel JLT) in the lateral direction by the source (emitter), channel (base) and drain (collector) regions in JLT structure in off-state. The proposed HGJLT reduces the subthreshold leakage current and suppresses the parasitic BJT action in off-state by reducing the band-to-band tunnelling probability.

Key words: hetero-gate-dielectric double gate junctionless transistor; band-to-band tunnelling; off-state
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1. Introduction

Recently, junctionless transistors (JLT)[1], based on Lilienfeld's device[2], are being studied to overcome the scaling limitation of MOSFETs due to the simple fabrication steps of JLTs compared with those in conventional MOSFETs. Junctionless transistors do not have any metallurgical p–n junction unlike MOSFETs. They have $N^+N^+N^+$ or $P^+P^+P^+$ structures with thin body and highly doped channel and the source, channel and drain have uniform doping. A JLT is turned off by the depletion of carriers in the channel by a suitable work function difference of gate material and channel and turned on by bulk conduction of current through the thin highly doped channel. Different types of structures for junctionless transistor have also been proposed and fabricated, such as, junctionless nanowire gate-all-around (GAA) architectures[3], multi-gated nanowire architectures with silicon-on-insulator (SOI)[4] and with bulk substrate[5], planar junctionless transistor on bulk substrate[6], planar junctionless transistor with non-uniform doping[7] etc.

Many research works explore the physics of the junctionless transistor[4, 5, 8, 9] and the effect of band-to-band tunnelling (BTBT) on their characteristics has been studied in Refs. [10–15]. The effect of band-to-band tunnelling, in off-state of JLT, has been studied in detail in Ref. [10]. In off-state, the suitable off current is maintained by the depletion of carriers in the channel on applying the work function difference in between the gate metal and the channel (ϕ_{MS}) and on application of drain bias, the conduction band of drain overlaps the valence band of the channel that triggers the electron to tunnel from the valence band of the channel to the conduction band of the drain (n-channel JLT). When an electron tunnels from the valence band of the channel to the conduction band of the drain, it creates holes in the channel and due to accumulation of holes in the channel, a parasitic bipolar junction transistor (n–p–n BJT for channel JLT)[10] is formed in the lateral direction by the source (emitter), channel (base) and drain (collector) regions in JLT structure in off-state.The accumulation of holes increases the potential of a floating-body channel (base of parasitic BJT) and turns on the parasitic BJT by forward biasing the base-emitter junction, resulting in a large drain current (collector current of the BJT) in off-state of JLT. In this context, large static power dissipation due to large leakage current in off-state, which increases with the decrease of gate length from one technological node to the next one, has become a big problem for low standby power (LSTP) applications. Here, band-to-band tunnelling (BTBT) in off-state significantly affects the sub-threshold leakage current, and has to be handled carefully to reduce the static power dissipation.

Recently, the hetero-gate-dielectric tunnel field effect transistors (HGTFETs) have been theoretically proposed[16, 17] and also experimentally investigated[18] to improve electrical characteristics. It has been shown that the hetero-gate-dielectric tunnel field effect transistors (HGTFETs) have higher on current, lower ambipolar leakage current and smaller subthreshold slope without sacrificing chip density. The physics of ambipolar leakage current in TFETs is the same as the effect of band-to-band tunnelling in JLTs. Hence, combining the advantages of the hetero-gate-dielectric structure and junctionless transistor, we propose a hetero-gate-dielectric double gate junction-

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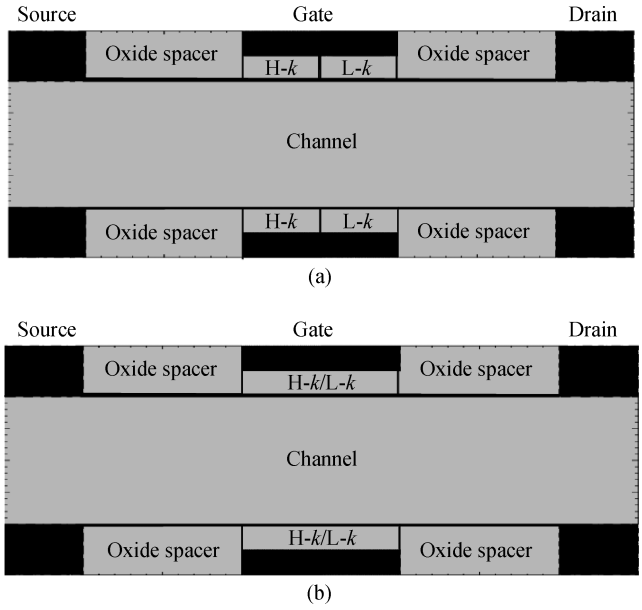

Fig. 1. A 2-D schematic structure of (a) a HGJLT-dual-k JLT, (b) a double gate junctionless transistor with high-k gate dielectric only (high-k JLT)/low-k gate dielectric only (low-k JLT).

less transistor (HGJLT) to optimize electrical characteristics by reducing the band-to-band tunnelling (BTBT) current in sub threshold regimes. It has been shown that HGJLT has lower sub threshold leakage current and it suppresses the parasitic BJT action[10].

2. Device structure and simulation

A 2-D schematic view of the HGJLT is shown in Fig. 1(a). In HGJLT the gate dielectric materials at source and at drain sides are different, that can be fabricated by isotropic etching of silicon oxide (here, silicon oxide is low-k gate dielectric material in HGJLT structure) followed by high-k material deposition as described in Ref. [16]. Here HfO_2 is used as high-k gate dielectric material at source side and SiO_2 as low-k gate dielectric material at drain side. We assume that the interface between the HfO_2 and SiO_2 is abrupt as reported in Refs. [16, 17] and that the diffusion length of HfO_2 in SiO_2 is only $\sim$0.035 nm when the device is annealed at 1000 ℃ for 5 s[19]. Here, HGJLT corresponds to dual-k JLT in which one half of the total gate insulator length (L_G) of dual-k JLT is HfO_2 and the other half is SiO_2. In addition, for comparison of electrical characteristics, a double gate junctionless transistor with high-k gate dielectric only (corresponds to high-k JLT) and low-k gate dielectric only (corresponds to low-k JLT) is shown in Fig. 1(b).

To evaluate the performance of the proposed HGJLT, a double gate junctionless transistor (JLT) for n-channel operation is simulated in Taurus-MEDICI 2D Device Simulator[20] and compared with high-k JLT and low-k JLT. For simulation, Fermi-Dirac statistics, Lombardi's mobility model with electric field dependent mobility and concentration dependent Shockley-Read-Hall model, Auger recombination model, and bandgap narrowing model to account for the effects of high channel doping are used. A nonlocal band-to-band tunnelling model (BTBT BT.LOCAL = 0 BT.MODEL = 2) available in

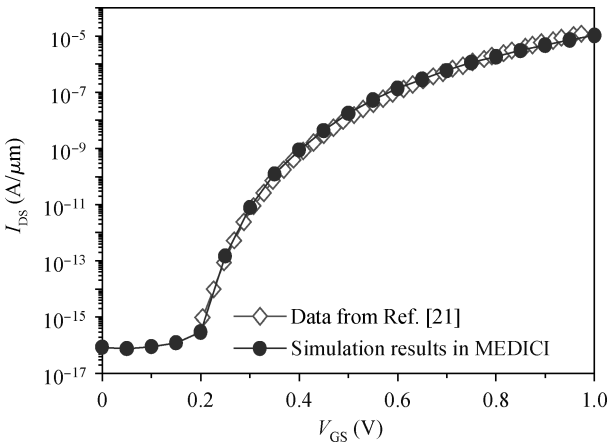

Fig. 2. Results of band-to-band tunnelling simulation and BTBT model calibration with the data of a double-gate tunnel FET with HfO_2 gate dielectric in Ref. [21].

Table 1. Parameters used for the device simulation.

Parameter	Value
Gate length (L_G)	20 nm
Length of oxide spacer	20 nm
High-k gate dielectric	HfO_2
Low-k gate dielectric	SiO_2
Gate dielectric thickness	2 nm
Length of high-k dielectric (L_{HfO_2}) in dual-k JLT	10 nm
Length of low-k dielectric (L_{SiO_2}) in dual-k JLT	10 nm
Device layer/channel thickness (T_{si})	10 nm
Source/channel/drain doping (N_d)	10^{19} cm^{-3}
Supply voltage (V_{DD})	1 V

MEDICI is used to study band-to-band tunnelling effects and a band-to-band tunnelling model is calibrated with the data of a double-gate Tunnel FET with HfO_2 gate dielectric in Ref. [21], as shown in Fig. 2. Parameters used for n-channel JLT simulation are shown in Table 1.

3. Result and discussion

The electrical characteristics of the hetero-gate-dielectric double gate junctionless transistor with dual gate dielectric materials of high-k at source side and low-k at drain side (dual-k JLT) are investigated and compared with corresponding compatible junctionless transistors with high-k gate dielectric only (high-k JLT) and low-k gate dielectric only (low-k JLT). For better comparison, work functions of gate material for all three cases, are adjusted to satisfy off-state current $I_{off} = 10$ pA/μm for low standby power (LSTP) application[22]. The gate work function for dual-k JLT, high-k JLT, and low-k JLT are taken 5.11, 5.0 and 5.24 eV, respectively.

Figure 3 shows the I_{DS}–V_{GS} characteristics for dual-k JLT, high-k JLT and low-k JLT of physical gate length $L_G = 20$ nm. We observe that subthreshold leakage current with band-to-band tunnel model is several orders higher compared with the subthreshold leakage current without band-to-band tunnel model. But subthreshold characteristic of high-k JLT is much

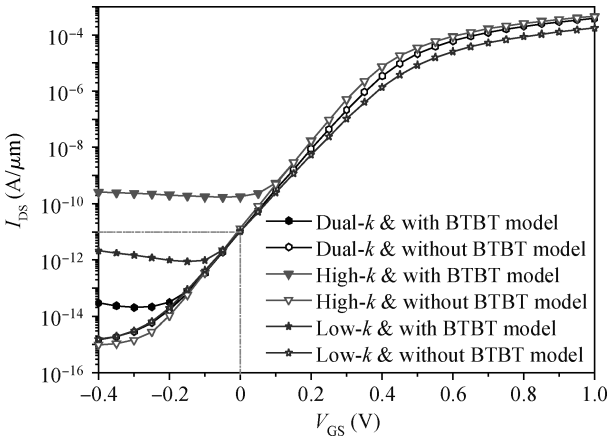

Fig. 3. I_{DS}–V_{GS} characteristics of dual-k JLT (for gate work function of 5.11 eV), high-k JLT (for gate work function of 5.0 eV), and low-k JLT (for gate work function of 5.24 eV) structure of gate length L_G = 20 nm with and without BTBT model, V_{DD} = 1 V.

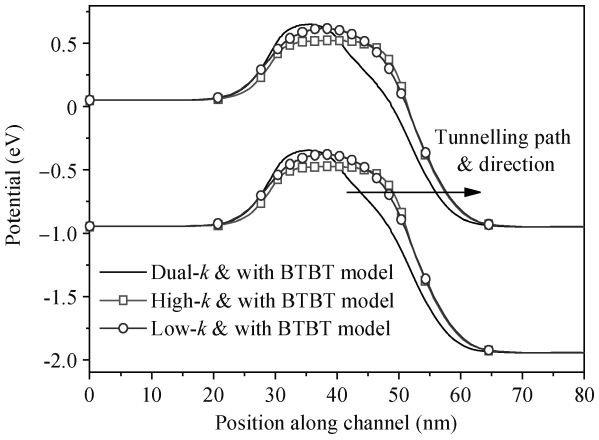

Fig. 5. Energy band diagram in the lateral direction with cut-line at 1nm below gate dielectric for dual-k JLT, high-k JLT and low-k JLT structure of gate length L_G = 20 nm in off-state (V_{GS} = 0 V and V_{DD} = 1 V).

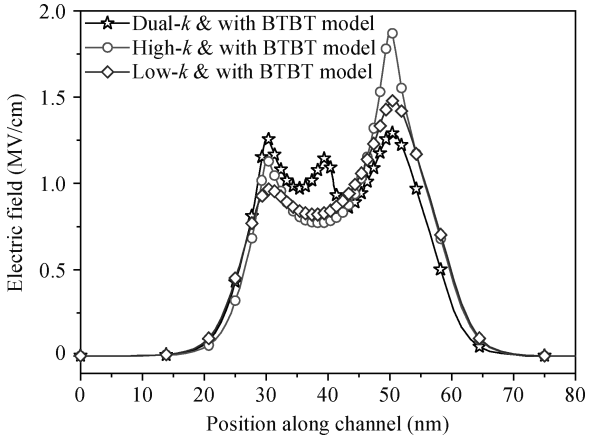

Fig. 4. Electric field in the lateral direction with cut-line at 1nm below gate dielectric for dual-k JLT, high-k JLT and low-k JLT structure of gate length L_G = 20 nm in off-state (V_{GS} = 0 V and V_{DD} = 1 V).

more affected by band-to-band tunnelling at drain side with less effect on dual-k JLT. The junctionless transistors with high-k gate dielectric only (high-k JLT) or low-k gate dielectric only (low-k JLT) (i.e. conventional junctionless transistor) have uniform gate to channel coupling strength from source to drain. Due to drain bias, in off-state, gate–drain electronic potential ($\phi_{MS} + V_{Drain}$) is higher than source–gate electronic potential (ϕ_{MS}) and this results in band overlap between the valence band of the channel and the conduction band of the drain, and very high electric field at the drain side is observed compared with the source side as shown in Fig. 4. At the drain side, the electronic energy band overlap with high electric field easily triggers the electron to tunnel from the valence band of the channel to the conduction band of the drain. As high-k JLT has strong gate-to-channel coupling strength compared with low-k JLT, very high electric field is created at the drain side resulting in very high band-to-band tunnelling current for high-k JLT. In the proposed hetero-gate-dielectric double gate junctionless transistor (dual-k JLT), the strong gate-to-channel coupling strength is observed at the source side because of the use of high-k dielectric and the weak gate-to-channel coupling strength is observed at the drain side because of the use of low-k gate dielectric. The strong gate to channel coupling at the source side maintains the off-state current due to the depletion of carriers in the channel and it results in a large potential barrier between the source and the channel for electrons while the weak gate to channel coupling at the drain side reduces the electric field and results in a decrease of tunnelling probability of electron from the valence band of the channel to the conduction band of the drain. Hence dual-k JLT improves the electrical characteristics in the subthreshold regime. The use of hetero-gate-dielectric improves the off-current by four orders of magnitude for a comparable on-current and SS compared to the high-k JLT structure with BTBT model, as can be seen in Fig. 3.

We also investigate the energy band diagram and tunnelling barrier width in the lateral direction with cut-line at 1 nm below gate dielectric for dual-k JLT, high-k JLT and low-k JLT structure of gate length L_G = 20 nm in off-state (V_{GS} = 0 V and V_{DD} = 1 V) as shown in Figs. 5 and 6. From Fig. 5, we observe that the conduction band and valence band of high-k JLT and low-k JLT fall abruptly compared with the conduction band and valence band of dual-k JLT at drain side. As the conduction band and valence of dual-k JLT falls gradually, it results in an increase in tunnelling barrier width of dual-k JLT compared with high-k JLT and low-k JLT as shown in Fig. 6. Tunneling barrier width or tunnelling distance is defined as the minimum distance between the maximum of the valence band at a given point in the channel to the minimum of the conduction band in the drain[10]. As the tunneling distance or tunneling barrier width is a critical aspect of band-to-band tunnelling[23], the increase of tunneling distance for dual-k JLT suppresses the subthreshold leakage current due to band-to-band tunneling by decreasing tunneling probability (BTBT generation rate) of the electron from the valence band of the channel to the conduction band of the drain.

Now we study the parasitic BJT behaviour of JLT. Electrons and holes are generated at the end of the tunneling path by electron tunnelling from the valence band to the conduction band and creating a hole in the valence band. Accumulation of holes makes the channel p-type (n-channel JLT), it forms

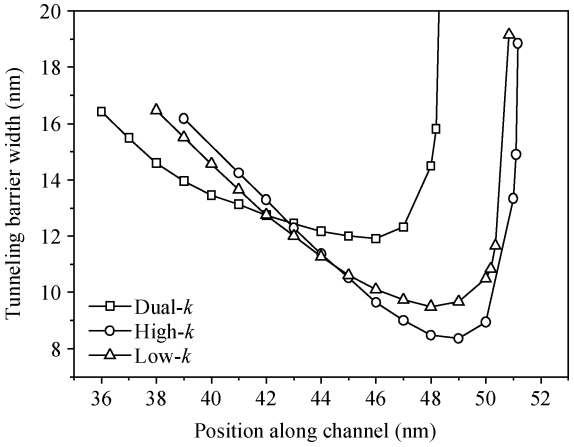

Fig. 6. Tunneling barrier width along tunneling path in the lateral direction with cut-line at 1nm below gate dielectric for dual-k JLT, high-k JLT and low-k JLT structure of gate length $L_G = 20$ nm in off-state ($V_{GS} = 0$ V and $V_{DD} = 1$ V). Tunnelling barrier width or tunnelling distance is defined as the minimum distance between the maximum of the valence band at a given point in the channel to the minimum of the conduction band in the drain[10].

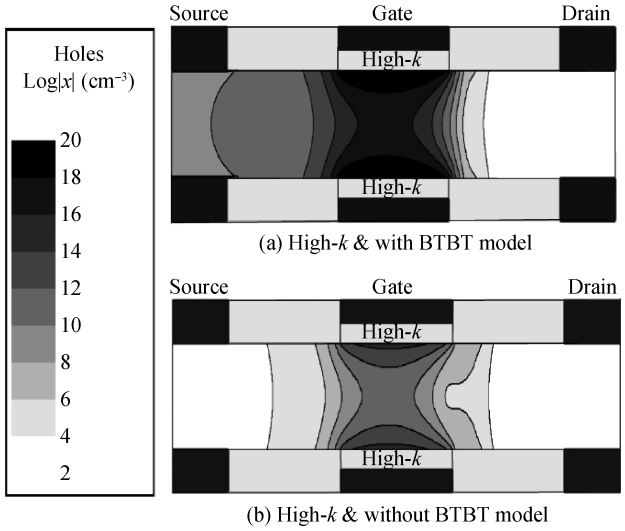

Fig. 7. 2D hole concentration contour plot for high-k JLT with BTBT model and without BTBT model in off-state ($V_{GS} = 0$ V, $V_{DD} = 1$ V).

a parasitic BJT (n–p–n) with source (n-type region)-channel (p-type region)-drain (n-type region) in the lateral direction of the device. In JLT, parasitic bipolar junction transistor (BJT) action due to band-to-band tunneling has been studied in detail in Ref. [10]. Here we show that the proposed hetero-gate-dielectric double gate junctionless transistor (dual-k JLT) reduces the chances of parasitic BJT formation by suppressing band-to-band tunnelling.

As discussed earlier, high-k JLT has higher electron tunnelling probability and results in a large amount of hole accumulation in the channel in off-state because electrons tunnel from the valence band of the channel to the conduction band of the drain. The holes are left behind in the channel and the barrier between the source and the channel prevents holes from flowing from channel to source. Figures 7(a) and 7(b) show hole concentration of high-k JLT with and without

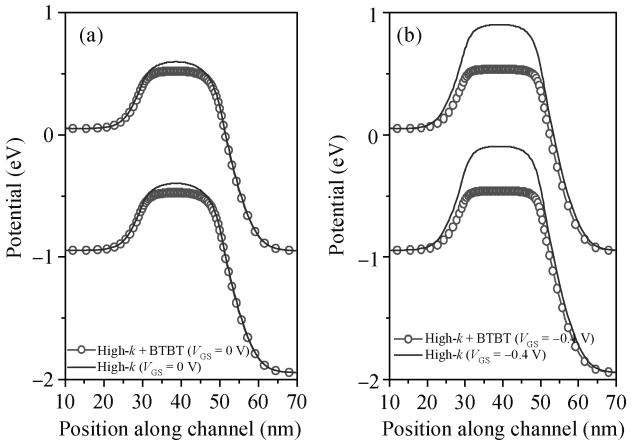

Fig. 8. Energy band diagram in the lateral direction with cut-line at 1 nm below gate dielectric for high-k JLT structure of gate length $L_G = 20$ nm when (a) $V_{GS} = 0$ V and $V_{DD} = 1$ V with and without BTBT model, (b) $V_{GS} = -0.4$ V and $V_{DD} = 1$ V with and without BTBT model.

BTBT model, respectively. From Figs. 7(a) and 7(b), it is clear that with BTBT model, large numbers of holes accumulate in the channel compared with the concentration of holes in the channel without BTBT model and this creates a parasitic BJT in off-state. The energy band diagram in Fig. 8 shows that the potential of a floating-body-channel (base of parasitic BJT) is increased, when the BTBT model is included in the simulation because of accumulation of holes in the channel. The increase of potential in floating-body (channel) leads to a forward bias at the base–emitter junction of parasitic BJT and turns on the parasitic BJT, resulting in large drain current. In high-k JLT, because of high tunnelling rate, the parasitic BJT is turned on at $V_{GS} > 0$ V and results in large leakage current in off-state ($V_{GS} = 0$ V and $V_{DD} = 1$ V). Once parasitic BJT is turned on, it remains on and the potential of the channel remains constant and does not decrease with the decrease of gate voltage, unlike when BTBT model is not included in the simulation. The accumulation of holes in the channel due to band-to-band tunneling, increases the potential of the channel, which results in forward bias of the base-emitter junction of parasitic BJT and turns on the parasitic BJT. Here, the channel region acts as Base of parasitic BJT, the source acts as emitter and the drain acts as collector[10]. Once parasitic BJT is turned on, the voltage drop between base and emitter remain almost constant (0.6–0.8 V)[24] similar to normal BJT operation. As the source region of junctionless transistor (emitter of parasitic BJT) bias to ground for n-channel JLTs operation, the channel potential (base potential of parasitic BJT) remains almost constant.

Figures 9(a) and 9(b) show the hole concentration of low-k JLT with and without BTBT model, respectively. We observe a small difference in the hole concentration in off-state for low-k JLT and lower concentration of holes compared with high-k JLT. Figure 10 shows that in off-state ($V_{GS} = 0$ V) a small accumulation of holes in the channel has no effect on the increase of the potential in the floating-body (channel) when BTBT model is included in the simulation, but at $V_{GS} = -0.4$ V, the increase of potential in the channel (with BTBT model) shows the effects of significant band-to-band tunnelling and accumulation

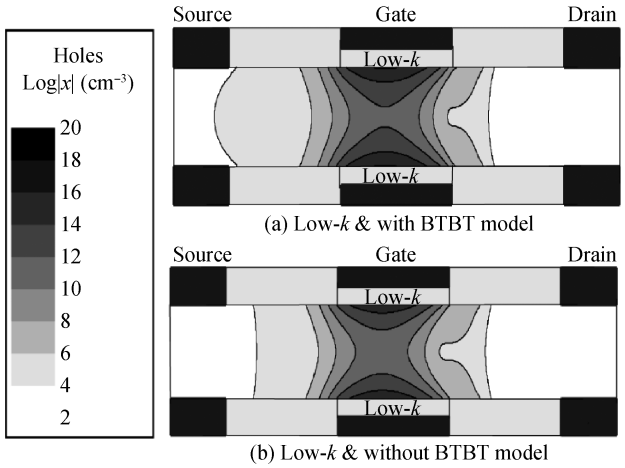

Fig. 9. 2D hole concentration contour plot for low-k JLT with BTBT model and without BTBT model in off-state ($V_{GS} = 0$ V, $V_{DD} = 1$ V).

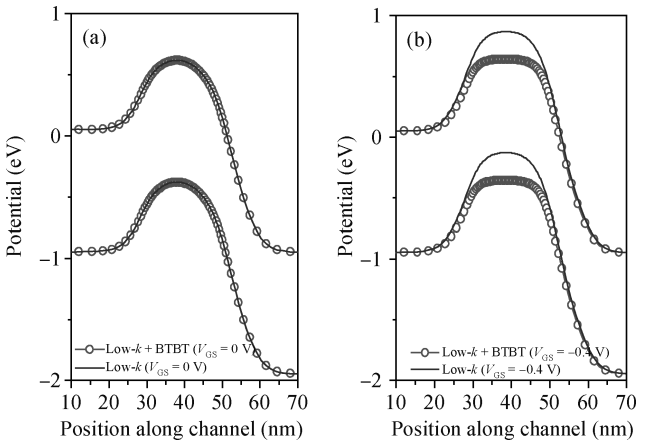

Fig. 10. Energy band diagram in the lateral direction with cut-line at 1 nm below gate dielectric for low-k JLT structure of gate length $L_G = 20$ nm when (a) $V_{GS} = 0$ V and $V_{DD} = 1$ V with and without BTBT model, (b) $V_{GS} = -0.4$ V and $V_{DD} = 1$ V with and without BTBT model.

of holes in the channel.

On the other hand, from Figs. 11(a) and 11(b), the hole concentration in the channel of the dual-k JLT in off-state with and without BTBT model are almost identical due to negligible BTBT generation rate in off-state and very much lower hole concentration is observed compared with high-k JLT. In Fig. 12, the energy band diagram at $V_{GS} = -0.4$ V shows a small change in the potential in the channel (base of parasitic BJT) and a small accumulation of holes in the channel due to reduced band-to-band tunnelling effects in dual-k JLT compared with high-k JLT and low-k JLT. Hence, the proposed hetero-gate-dielectric double gate junctionless transistor (dual-k JLT) suppresses the effects of parasitic BJT formation in JLT.

The impact of variation of oxide spacer length on the I_{DS}–V_{GS} curve is shown in Fig. 13. We have taken 20 nm oxide spacer length, so that minimum leakage power is achieved. The 20 nm of oxide spacer length is also taken for a 20 nm channel length in Ref. [25]. From the figure we observe that for the comparable ON current, the oxide spacer length of 20 nm gives the two orders of leakage current improvement as compared to the 5 nm oxide spacer length. For a larger length of oxide spacer, the improvement in OFF current and little degradation in ON current is observed, i.e., because of the presence of higher resistivity path along the direction of charge transport.

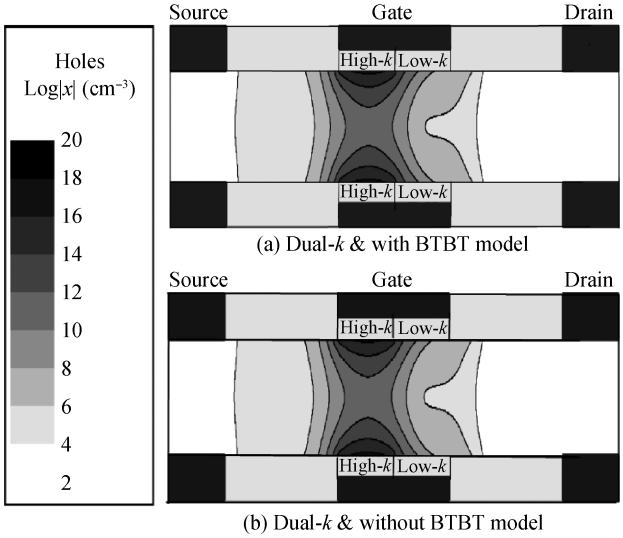

Fig. 11. 2D hole concentration contour plot for dual-k JLT with BTBT model and without BTBT model in off-state ($V_{GS} = 0$ V, $V_{DD} = 1$ V).

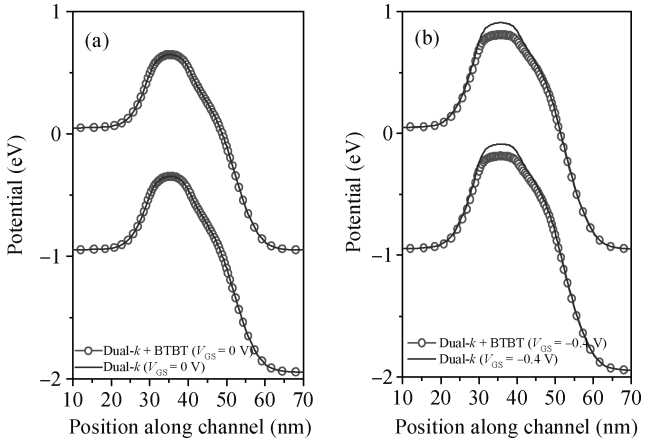

Fig. 12. Energy band diagram in the lateral direction with cut-line at 1nm below gate dielectric for dual-k JLT structure of gate length $L_G = 20$ nm when (a) $V_{GS} = 0$ V and $V_{DD} = 1$ V with and without BTBT model, (b) $V_{GS} = -0.4$ V and $V_{DD} = 1$ V with and without BTBT model.

Figure 14 shows the simulated I_{DS}–V_{GS} characteristics for air ($K_{sp} = 1$), Al_2O_3 ($K_{sp} = 9.6$) and HfO_2 ($K_{sp} = 21$) spacers using BTBT model. From the simulation results we observe that the OFF current (with BTBT model) is a strong function of spacer-k. It is observed that with the increase of the dielectric constant of the spacer, the off-state leakage current due to band-to-band tunnelling is reduced. In off-state, the channel is depleted and a gate-channel vertical electric field is observed. The use of high-k spacers on either side of the gate enhances the gate-channel fringing electric field through the spacer and it spreads depletion layers beyond the gate edges and reduces the peak of electric fields in the channel. As the depletion layers and electric fields spread towards the drain region, the conduc-

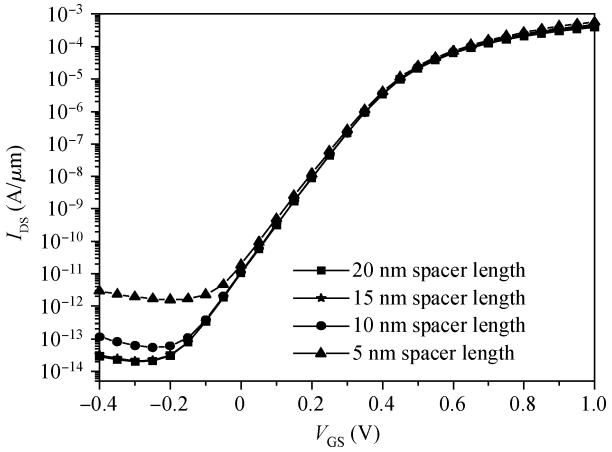

Fig. 13. I_{DS}–V_{GS} characteristics of double gate JLTs of gate length L_G = 20 nm with BTBT model for different oxide spacer length, V_{DD} = 1 V.

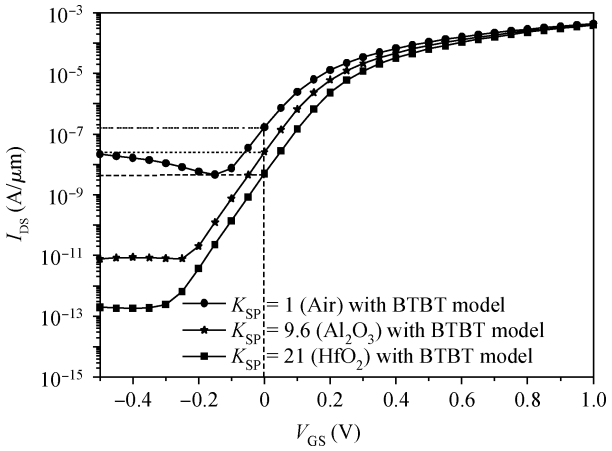

Fig. 14. I_{DS}–V_{GS} characteristics of double gate JLTs of gate length L_G = 20 nm with BTBT model, V_{DD} = 1 V for air (K_{sp} = 1), Al_2O_3 (K_{sp} = 9.6) and HfO_2 (K_{sp} = 21) spacers. Gate material work-function (ϕ_{MS}) = 5.11 eV, Length of spacer (L_{sp}) = 20 nm.

tion band and the valence band at the drain side fall gradually and this increases the tunneling width along the tunneling path of the electron. Since the tunneling width along the tunneling path of the electron is a critical aspect of band-to-band tunneling, the increase of tunneling width for the use of high-k spacer reduces the tunneling probability of the electron from the valence band of the channel to the conduction band of the drain, resulting in reduction of the off-state leakage current due to band-to-band tunneling. The improvement in off-current using high-k spacer for JLTs has also been discussed in Ref. [26].

I_{DS}–V_{GS} characteristics of double gate JLTs of gate length L_G = 20 nm with BTBT model for different length of high-k dielectric (L_{HfO2}) in dual-k JLT is shown in Fig. 15. From the simulation results, we observe that the equal length of high-k dielectric (L_{HfO2}) and low-k dielectric (L_{SiO2}) gives the optimized result. From the figure we observe that as the length of high-k dielectric (L_{HfO2}) increases from source to drain, off-current decreases for L_{HfO2} from 5 to 15 nm, and this is because of a continuous increase in threshold voltage of the device. However because the L_{HfO2} equals 20 nm, unexpected

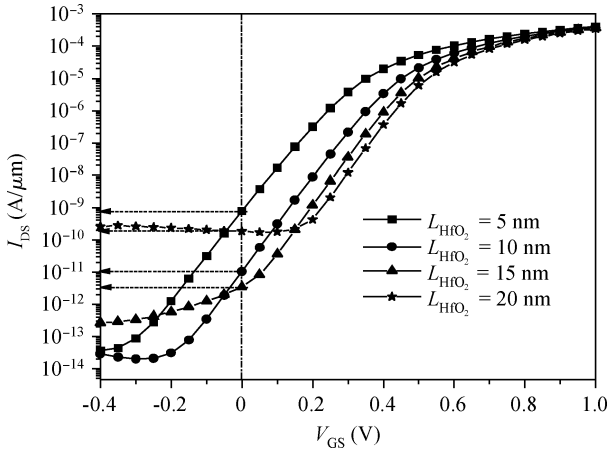

Fig. 15. I_{DS}–V_{GS} characteristics of double gate JLTs of gate length L_G = 20 nm with BTBT model for different length of high-k dielectric (L_{HfO_2}) in dual-k JLT (for gate work function of 5.11 eV), V_{DD} = 1 V.

off-current trends are observed, i.e. off-current of L_{HfO2} equal to 20 nm is higher than the L_{HfO2} equal to 10 nm and 15 nm, even though threshold voltage of L_{HfO2} equal to 20 nm is higher than the 10 nm and 15 nm length of high-k dielectric. This is because the length of high-k dielectric of 20 nm offers a better coupling effect near the drain-to-channel p–n junction. The better coupling effect offered by the higher dielectric constant material near the drain-to-channel p–n junction significantly reduces the tunneling barrier width in off-state (V_{GS} = 0 V, V_{DD} = 1 V). The reduction in tunneling barrier width increases the off-state current significantly compared to the 10 nm and 15 nm length of high-k dielectric, even though the threshold voltage of L_{HfO2} equal to 20 nm is higher than the 10 nm and 15 nm length of high-k dielectric. For the lower value of L_{HfO2} (i.e., $L_{HfO2} \leqslant$ 15 nm) the coupling effect near the drain-to-channel p-n junction in off-state does not become very prominent, hence clear trends of continuous decrease in off-current is observed; this is because of a continuous increase of threshold voltage for L_{HfO2} from 5 to 15 nm.

4. Conclusions

We have evaluated the performance of a hetero-gate-dielectric double gate junctionless transistor (HGJLT) in a subthreshold regime and its subthreshold characteristic is compared with a junctionless transistor with high-k gate dielectric only (high-k JLT) and also with a junctionless transistor with low-k gate dielectric only (low-k JLT). 2D numerical simulations show that HGDJLT has less band-to-band tunnel current in off-state and hence it suppresses both the subthreshold leakage current and the effects of parasitic BJT action.

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