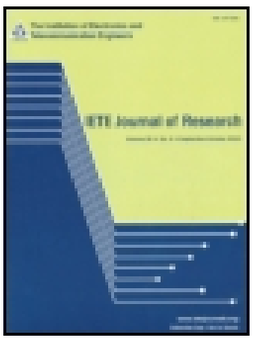

# An Area Efficient Sub-threshold Voltage Level Shifter using a Modified Wilson Current Mirror for Low Power Applications

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# An Area Efficient Sub-threshold Voltage Level Shifter using a Modified Wilson Current Mirror for Low Power Applications

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**ABSTRACT**

In the present communication, a new technique has been introduced for implementing low-power area efficient sub-threshold voltage level shifter (LS) circuit. The proposed LS circuit consists of only nine transistors and can operate up to 100 MHz of input frequency successfully. The proposed LS is made of single threshold voltage transistors which show least complexity in fabrication and better performance in terms of delay analysis and power consumption compared to other available designs. CAD tool-based simulation at TSMC 180 nm technology and comparison between the proposed design and other available designs show that the proposed design performs better than other state-of-the-art designs for a similar range of voltage conversion with the most area efficiency.

**KEYWORDS**

Current mirror; CAD simulation; Level shifter (LS); Low power; Sub-threshold operation; Typical transistor (TT)

## 1. INTRODUCTION

With the increasing demand of portable devices in electronics, low power consumption has become the main design criterion for Very Large Scale Integrated (VLSI) circuits and systems. High complexity designs need to trade off between performance and power. In general, small area and high performance are two conflicting constraints [1]. Dynamic power consumption and static power consumption are noted in VLSI circuit. Dynamic power has two components *i.e.* switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [2]. The static power of Complementary Metal Oxide Semiconductor (CMOS) VLSI circuits is determined by the leakage current through each transistor. For a high complexity VLSI circuit the switching power dominates other types of power consumptions. The switching power can be expressed as follows.

$$P_{\text{switching}} = \alpha C V_{DD}^2 f \tag{1}$$

So by reducing the circuit activity ($\alpha$), capacitance ($C$), supply voltage ($V_{DD}$) and frequency ($f$) we can reduce the power consumption [3]. But in modern computation the frequency of operation is so high that it will increase the power consumption. There are many methods for reducing power in today's devices. These are: (1) Dynamic logic, (2) clock gating, (3) gate sizing and (4) multiple voltage design [4,5]. The first three methods are used to reduce the circuit activity or the capacitance value in order to reduce the switching power consumption. The fourth method deals with reducing the supply voltage which is a useful tool in reducing total power. Such a method uses multiple supply voltages ($V_{DD}$). The main idea is to assign a high $V_{DD}$ (VDDH) to the gates that belong to the critical path, while a separate low $V_{DD}$ (VDDL) is supplied to off-critical path for the remaining gates [6]. Such multiple supply voltage improves the dynamic power consumption performance, but it also increases the static current. To remove the static current, one possible solution is the use of level converters placed between the VDDL- and VDDH-supplied gates, which again may increase area and power. To improve power consumption performance and area overhead of level converters, several approaches have been introduced. The high- to low-level shifter (LS) is a simple design [7]. It consists of a pair of inverters connected to a low supply voltage. The conventional low- to high-voltage level shifters are of two types and they work near threshold voltage [8]. The low- to high-LS has a complex circuitry especially when the input operating voltage becomes less than the threshold voltage of the MOS transistors [9]. To overcome this problem several designs have been introduced.

## 2. PRIOR WORK

The two types of conventional LS using differential cascade voltage switch (DCVS) and current mirror load are

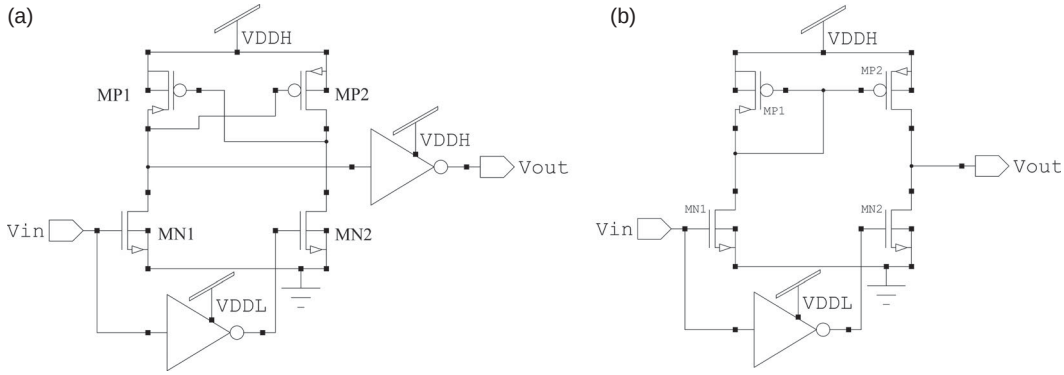


**Figure 1:** Conventional low- to high-voltage LS (a) type-I and (b) type-II

shown in Figure 1. The limitation for these kinds of level shifters is that these cannot work in sub-threshold voltage region. But some real-time systems require sub-threshold operation [10,11]. Several solutions have been proposed to address the problem of the conventional level shifters. T.H. Chen, J. Chen, and L. T. Clark proposed a circuit where they added PMOS current limiter to drive the circuit at sub-threshold on current [12]. The limitation of the circuit was that it required a few more fabrication steps. A 24 transistor swing inverter-based LS [13], PMOS half latch-based LS [14], and Wilson current mirror-based LS [15] were also in the line of problem solver. Recently, Lanuzza, Corsonello reported a modified DCVS-based LS in 2012 [16]. But it suffers with large power consumption at high-frequency range. Hosseini, Saberi proposed a modified logic error correction technique in the LS [17]. In [18,19] modified Wilson current mirror hybrid buffer-based designs were proposed. Some designs were also proposed using modified device (multi-threshold, Tunnel FET) structures [20,21]. But multiple threshold device or TFET-MOSFET-based designs require a few additional fabrication steps. Recently a few more designs have been reported with additional circuit blocks [22–24]. However, additional circuitry involves larger area and increases power consumption. Very recently two notable designs have been introduced in [25,26]. In [25], a capacitor has been introduced which increases the power consumption of the circuit. Similarly the design presented in [26] suffers with higher static power consumption due to a pass transistor placed within the circuit. In order to solve these issues related with complex fabrication, larger area and power overhead the authors are proposing a new design for sub-threshold VDDL to VDDH LS.

## 3. PROPOSED LS DESIGN

The proposed LS circuit is based on the modified Wilson current mirror. The circuit is shown in Figure 2. It consists of an inverter which is working over low-voltage level, a modified Wilson current mirror and a driver inverter.

The first inverter is working in the low-voltage domain. The transistors present in the inverter are working in the sub-threshold region. The drain current produced by MOS transistor operating in the sub-threshold region is a function of gate to source voltage ($v_{GS}$), drain to source voltage ($v_{DS}$) and source to substrate voltage ($v_{BS}$). As in the proposed design all the transistors have source and substrate shorted; therefore, the drain current can be written as

$$i_D = \left(\frac{W}{L}\right)\mu_e C_{ox}(n-1)\emptyset_t{}^2 e^{(v_{GS}-v_T)/n\emptyset_t} \tag{2}$$

In (2) the factor $W/L$ is the aspect ratio of the transistor, $\mu_e$ is the mobility and $C_{ox}$ is the oxide layer capacitance, $n$ is the sub-threshold slope factor and $\emptyset_t$ is the surface potential. At sub-threshold region the maximum $v_{GS}$ can be equal to threshold voltage ($v_t$). The sub-threshold drain current is mainly produced by diffusion and can reach a maximum value

$$i_{D,\,\text{max-sub}} = \left(\frac{W}{L}\right)\mu_e C_{ox}(n-1)\emptyset_t{}^2 \tag{3}$$

It produces log-linear response at the output with differential fast transition low-voltage input signals. This linear output is fed to the gate of MN1. The NMOS transistor MN1 is a narrow width transistor which offers larger on state impedance resulting lower value of drain current through N3. MP1 is a narrow width PMOS which controls the gate voltage for MP2. When the transistor MP2 is on, the impedance decreases across it, which results a larger drain current to drive through MP4 and MN2. The transistors MP4 and MN2 act like a current output inverter with strong pull-up at N2. Therefore, the low logic is inverted with pull up voltage connected to VDDH which is being forwarded to the final stage inverter. The

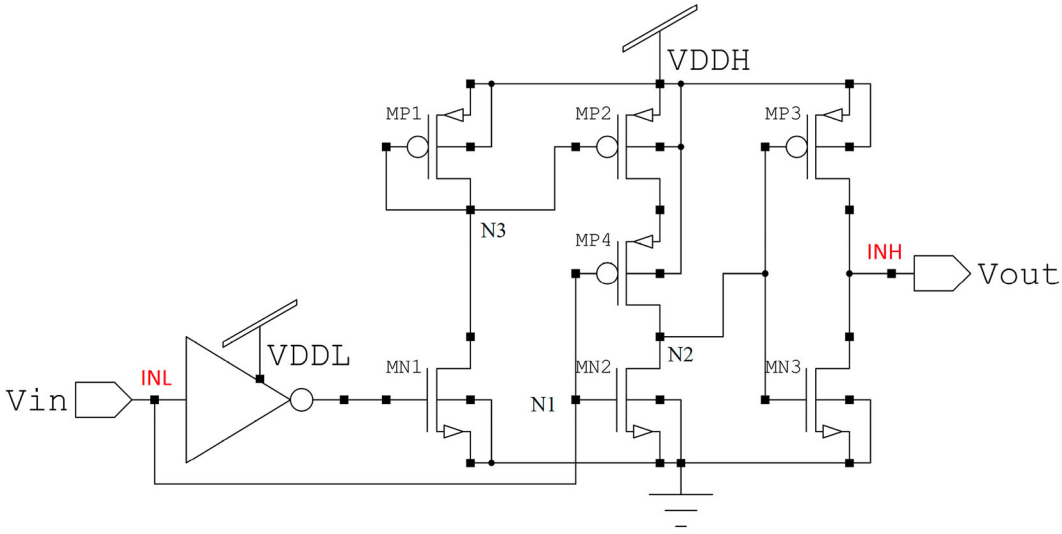


**Figure 2:** Proposed LS

final stage inverter is the output driver creating the same logic of the low-input logic Vin.

### 3.1 Logical Analysis

In order to analyze the circuit let us take logical low-voltage "0" as an input at Vin. As the first stage inverter is working on sub-threshold voltage the output will be logical with high "VDDL". Corresponding "VDDL" is fed to MN1which is making it on and creating the reference current level. So MP1 is on and makes MP2 to flow the same drain current. MN2 and MP4 are producing inverted logic *i.e.* "high" at their shorted drain node. The strong pull-up network is producing "high" logic as VDDH. The last inverter stage is therefore inverting the logic by shaping the waveform. Similarly when the input Vin is logic "high" as "VDDL" the corresponding first-stage output becomes "low" *i.e.* grounded. MN1 remains off which makes MP1 and MP2 off. As Vin is "high" it makes MN2 on and pulls down the drain output to ground. Therefore the final inverter stage output becomes "high" as VDDH.

### 3.2 Properties

In this section, the performance of the proposed LS has been evaluated using CAD simulation with TSMC 180 nm process technology. A normal VDDH was set to 1.8 V. Simulations have been done assuming the input signal frequency of 10 MHz, rise and fall times of 0.1 ns. The transistor sizes used in the proposed circuit are tabulated in Table 1. The robustness of the LS has a wide input range of process voltage and temperature (PVT).

**Table 1: Transistor dimensions**

| Transistor | W/L |
|---|---|
| MN1 | 0.36 µm/0.54 µm |
| MN2 | 0.18 µm/0.18 µm |
| MN3 | 0.18 µm/1.62 µm |
| MP1 | 0.18 µm/1.08 µm |
| MP2 | 0.36 µm/0.18 µm |
| MP3 | 1.08 µm/0.18 µm |
| MP4 | 0.18 µm/0.18 µm |

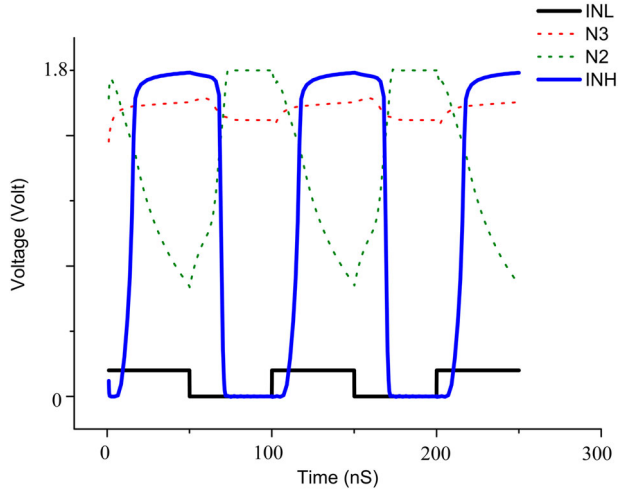


**Figure 3:** Transient response of the proposed LS

Figure 3 shows the transient response of the proposed LS. Typical temperature is set at 25°C. The amplitude of the input node INL is 0.2 V and the frequency is 10 MHz. The proposed LS is able to convert the input signal into a 1.8-V output signal at INH. Figure 3 also shows the voltage variations at nodes N2 and N3.

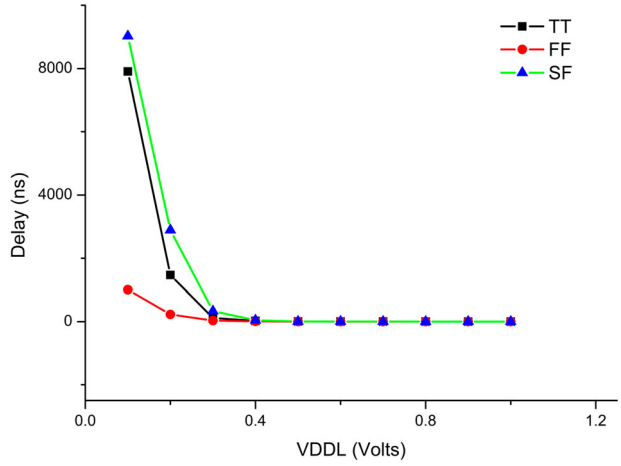


**Figure 4:** Propagation delay vs VDDL

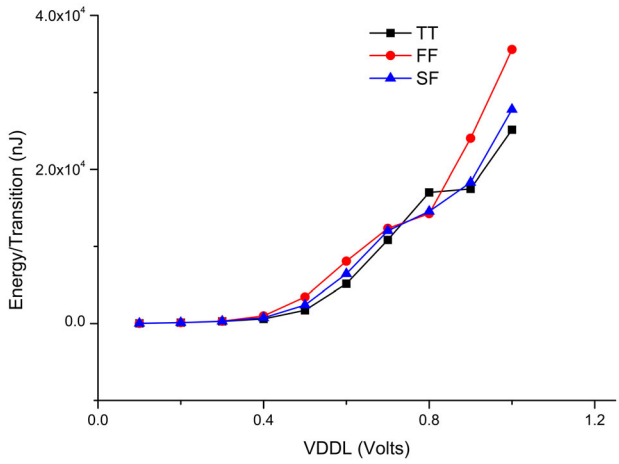


**Figure 5:** Energy dissipation per transition at discrete VDDL

## 4. SIMULATION RESULTS

The typical PVC case is simulated with the typical transistor (TT) model parameters with the VDDL being set as 0.2 V and VDDH being set as 1.8 V. The power supply voltages are then changed by 10% for both cases, while the temperature is increased by 50% to find the worst case of operation. Figure 4 exhibits the propagation delay as a function of VDDL for TT case, fast PMOS–fast NMOS case (FF) as well as for slow NMOS–fast PMOS model (SF) case. Detailed analysis of delay, energy per transition and power has been carried out in the following sections.

### 4.1 Delay Analysis

Figure 4 shows the propagation delay of the proposed LS with respect to change in VDDL. At three PVT corners the proposed LS shows a marginal delay across the VDDL range of 0.3–1.2 V. As the voltage scales down, the propagation delay increases. It becomes poor as the VDDL value decreases from 0.3 V. The delay is more for SF and TT. This is happening due to the increment in the leakage current of the transistors working in the weak inversion region. In fact, in the typical corner, the delay of the proposed design is 140.48 ns when VDDL is 0.2 V and the transition frequency is 10 MHz.

### 4.2 Energy Per Transition Analysis

Figure 5 shows the energy per transition in nano Joule as the function of the VDDL in three PVT corners of the proposed design. We know that the total energy includes both the dynamic energy and the static energy dissipation. The energy dissipation value is low for all PVT corners when VDDL is significantly low. The optimized value obtained at VDDL is equal to 0.31 V at a transition rate of 1 MHz and the value is 128fJ.

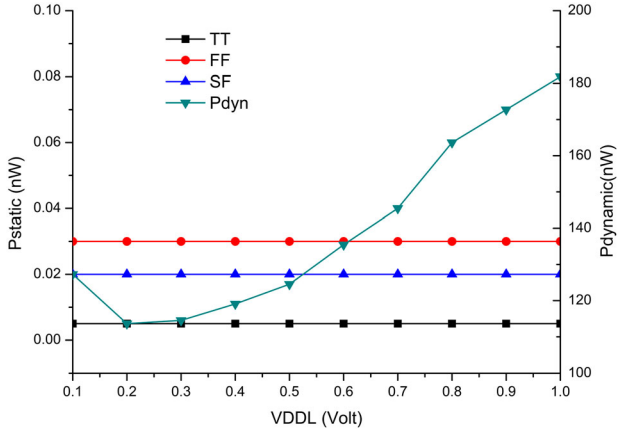


**Figure 6:** Dynamic and static power consumptions as a function of VDDL

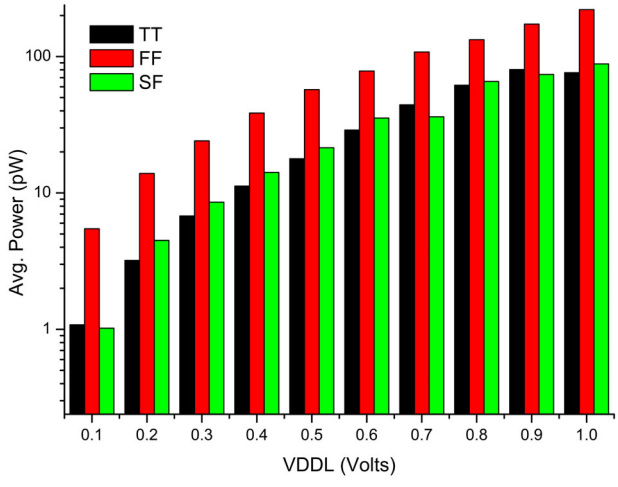


**Figure 7:** Average power consumption of the proposed LS at discrete VDDL

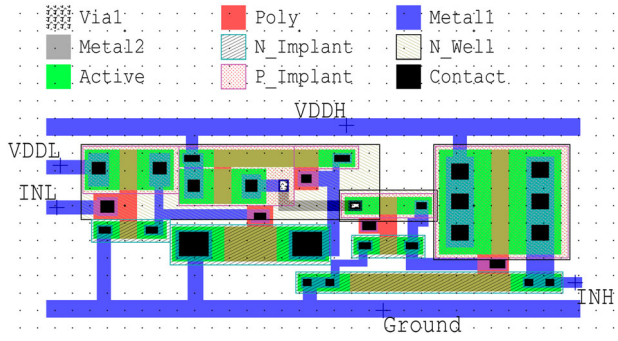


**Figure 8:** Layout of the proposed LS in TSMC 180 nm technology

**Table 2: Frequency response of LS**

| Frequency | VDDL,min(V) | Max Power | Delay |
|---|---|---|---|
| 1 Mhz | .30 | 286 nw | 140.21 ns |
| 5 Mhz | .33 | 348 nw | 64.69 ns |
| 10 MHz | .38 | 613.9 nw | 19.09 ns |
| 20 Mhz | .41 | 50.35 uw | 14.93 ns |
| 50 Mhz | .50 | 86.13 uw | 3.34 ns |
| 100 Mhz | .68 | 204.24 uw | 1.32 ns |
| 500 Mhz | 1.5 | 1.28 mw | 360.14 ps |

### 4.3 Power Analysis

Figures 6 and 7 shows the dynamic and static power consumptions as well as average power consumption across VDDL. For TT case the static power is less than 0.01 nW and for FF case the static power is maximum (0.03 nW). It has been found that the dynamic power consumption continues to lower down at near threshold level but as the VDDL continuous to scale down to deep sub-threshold, the power starts rising suddenly owing to the fact that static energy dominates the main energy consumption. In Figure 7, the average power consumption at discrete VDDL has been displayed. The average power consumption of the LS in discrete VDDL shows that the TT case consumes less than 10pW.

Figure 8 shows the CAD-based schematic-driven layout of the proposed LS in generic 180 nm technology. The top metal-1 line is high power source (VDDH) line while bottom metal-1 line is the ground rail. Minimum poly width is set to 180 nm. Metal 1 overlap to surrounding contact is set to 50 nm. In such a technology the proposed design layout consumes 92.3 $\mu m^2$ area. The post layout parasitic extraction is performed in order to find the resistance and capacitance traces over their surroundings. With decreasing interconnect feature size the value of parasitic increases. It becomes more relevant when the transistor size shrinks down. The hierarchical physical verification is done using LVS and DRC extraction. In order to reduce the crosstalk effect minimum overlap of wires is maintained in the layout.

Table 2 shows the frequency response of the proposed LS. Though the proposed LS can up lift from minimum VDDL as 0.2 Volts to VDDH, it has been found that the optimum response occurs near 1 MHz with VDDL as 0.32 Volts and the power delay product is 4.73aJ.

## 5. COMPARATIVE ANALYSIS

In order to reveal the benefits of the proposed design, the authors have performed a comparative result analysis of different LS by simulation. The simulations have been made using standard CAD tool simulator by considering generic 180 nm process technology and maintaining the same W/L ratios as indicated in the referenced briefs at a temperature parameter fixed at 25°C. Also all the referenced briefs are designed using regular threshold voltage devices in order to evaluate the advantages offered by the circuits. Comparisons are made with respect to the conversion range, delay, transition energy, average power consumption, power-delay-product and no. of transistors used. The detailed comparison is shown in Table 3. It is revealed that the proposed LS can work in the sub-threshold voltage region and can lift up the voltage from 0.2 to 1.8 Volt. The average delay of producing the output is 19.9 ns at a conversion frequency of 1 MHz which is 16% faster than that shown in [22]. The average power consumed by the proposed LS is 38 pw which shows 37% better result than [23]. The proposed design also

**Table 3: Comparisons between different LSs**

| Design | Strategy | Conversion range (V) | Delay | Etr | Pavg . | PDP (attoJ) | No. of transistors | Results |
|---|---|---|---|---|---|---|---|---|
| [16] | DCVS | 0.2–1.8 | 16.6 ns | 0.074 nj(90 nm) @ 0.2 V–1 Mhz | 73.46075 nw | 1219.436 | 15 | Simulation |
| [19] | CM | 0.2–1.2 | 162 ns | 136fj (65 nm) @ 0.3 V–20 khz | 405.6 nw | 65707.2 | 16 | Simulation |
| [17] | CM + AC | 0.4–1.8 | 30 ns | 150 fj (180 nm) @ 0.4 V–1 Mhz | 205 nw | 6150 | 16 | Simulation |
| [20] | CM | 0.2–1.2 | 25 ns | 30.7 fj(65 nm) @ 0.3 V–1 Mhz | 234.9007 nw | 5872.5 | 12 | Simulation |
| [22] | CM + CL | 0.1–1.2 | 13.7 ns | 90.9 fJ (65 nm) @ 0.2 V–1 Mhz | 243.5019 nw | 3335.95 | 11 | Simulation |
| [23] | DCVS | 0.1–1.8 | 31.7 ns | 173 fJ (180 nm) @ 0.4 V–1 MHz | 0.060 nw | 1.907 | 14 | Simulation |
| [24] | CM + AC | 0.4–1.8 | 30 ns | 123 fj (180 nm) @0.4 V–1 MHz | 159 nw | 4770 | 14 | Simulation |
| [18] | CM | 0.21–3.3 | 163 ns | 954 fj (180 nm) @ 0.3 V–1 MHz | 0.970 nw | 158.11 | 18 | Simulation |
| [25] | CM + AC | 0.3–1.8 | 17.3 ns | 56 fj(180 nm) @ 0.4 v–500 kHz | 0.270 nw | 4.671 | 13 | Simulation |
| [26] | CM + AC | 0.3–1.8 | 9.8 ns | 186.8 fj(180 nm)@0.3 V–1 MHz | 2.89 nw | 28.32 | 11 | Simulation |
| This work | CM | 0.2–1.8 | 19.9 ns | 128 fj (180 nm) @ 0.3 V–1 MHz | 0.238 nw | 4.73 | 9 | Simulation |

has the lowest static power dissipation of only 0.03 nw. Therefore the PDP has been improved by 60% than that shown by [23]. Most strikingly, it is the most simple and area efficient as it is consuming only 92.3 $\mu m^2$ as the core area. The best energy per transition result is shown by [20]. However our proposed design is also showing better energy/transition response than other state-of-the-art designs.

## 6. CONCLUSION

In this paper, the authors have presented a low-power nine transistor-based LS which can up-convert from the deep sub-threshold voltage to the VDDH supply voltage of 1.8 V at a frequency of 10 MHz. The proposed design shows the propagation delay of 19.9 ns over a wide range of operating voltages. The high voltage range is 1.8 Volt for CMOS 180 nm technology. The LS avoids multiple threshold transistors, thereby reducing the fabrication complexities. The modified Wilson current mirror-based proposed LS shows excellent logical and functional response over a wide range of frequencies. The layout area is 92.3 $\mu m^2$ at TSMC 180 nm technology. Therefore it can be concluded that authors' proposed LS shows better PDP and area efficiency compared to available other designs.

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