Scheduling based Energy Optimization Technique in multiprocessor Embedded Systems

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Abstract-- At the operating system level, multi-core and multiprocessor SoC(MPSoC) started a new computing era but brought various twofold scheduling challenges in current developed thermal aware algorithms for multi-core processors. An offline thermal aware scheduling algorithm is proposed for improvement in multi core embedded system in case of energy, reliability as well as performance of a multi core system has been introduced. Embedded systems are increasing at much rapid speed than ever before. The temperature of a multi-core processor is managed and measured by the hardware management system due to shrinking of chip size power densities are increasing due to this increase in the temperature of chip occurs that reduces the processor's speed in multi-core embedded system. High peak temperature on chip adversely affects the life span of chip. Task migration is a common technique to avoid peak temperature values in multi core system. Those tasks have been migrated in a multi core system which produces more heat to such individual core that has less temperature. The proposed technique also considers other thermal problems which affects the reliability and performance of multi-core system. In this research, a suitable scheduling mechanism assign tasks to the core that has less temperature by considering power and performance of the multi core system. This scheduling technique migrate load on the cores that is far away from the core reaches threshold temperature. For attaining stability in temperature among multiple cores results are evaluated by comparing different task migration techniques which are introduced previously. All types of hot and cold tasks are considered to predict accurate temperature by using thermal history. The scheduling policy attains maximum efficiency in terms of energy by considering only those cores that are executing some tasks in highest energy state such as running state while considering all other cores in lowest energy state such as sleep or a deep sleep mode. The simulation results shows that the proposed technique reduces almost 5℃ temperature at 10% utilization and works efficiently when least number of tasks is in running state. The proposed technique has the ability to schedule more tasks to make a slower and energy efficient processor to control and manage the thermal effects on chip and also mange the processor energy consumption.

Keywords— ***Dynamic Voltage and Frequency Scaling, Dynamic Power Management, Dynamic Thermal Management, , Dynamic Voltage Scaling, Energy Optimization***

I. INTRODUCTION

Now a day electrical machines are all around us and machines are upgrading and developing day by day. The development in embedded machine technologies made our work easier and efficient using embedded systems. World is occupied by embedded devices so we cannot imagine the advancement of a machine without the contribution of embedded systems. A processing unit is already built-in in all the embedded machines that are working as a brain of the machine that needs to be updated with the passage of time. If the processing unit have higher processing speed it can execute and manage intense tasks efficiently at short interval of time.

The development in the processing unit is capable to run heavy tasks but it can have some issues e.g. Dimension, cost, power utilization, performance, reliability and processing speed are the major issues with the advancement in processor. The lack of concentration can affect the overall system performance. The temperature on the chip increases for which various mechanisms are used to reduce the thermal effects due to high heat and increase the performance of the system because high heat causes the chip to be damage [1].

H. Sun, P. Stolf, and J. Pierson et al. (2017) proposed a thermal-aware online scheduling based technique is used for high-performance homogeneous systems using a thermal model that considers both spatial and temporal gradients and their correlation with temperature evolution. Increase the performance of the homogeneous system dynamic voltage and frequency scaling is used for the smooth execution of task [2].

A. Asad, O. Ozturk, M. Fathy et al. (2017) Introduces a technique that improve the performance and reliability of a multi-core processor by checking the impact of power consumption of multi-core processor and dynamically check the frequency and voltage. This approach is also used to predict the thermal variation on each core. The proposed method gives 54.3% improvement in results and 61% improvement in energy delay as compared to the conventional multi-processor [3].

X. Mei, Q. Wang et al. (2017) proposed a GPU dynamic voltage and frequency scaling that is very efficient for saving energy for various applications and also used evaluate the impact of GPU DVFS on application power consumption when an application is in running state and also consider the impact of application perform ace and energy conversation as compared to DVFS that is widely used in embedded devices like cell phones and various multipurpose electronic gadgets to improve performance because GPU-DVFS consider both the architecture and application of GPU [4].

P. Wu and M. Ryu et al. (2017) proposed a scheduling based best speed fit EDF technique that chooses the suitable processor when the task is allocated for execution and the proposed technique doesn't consider the fastest core. The performance and reliability of the chip is more improved then that of the global earliest deadline first algorithm that considers the priority of the task while executing. Migration of task can occur at any time with different speed processors, and

task were assign on the basis of deadlines those tasks that can have an early deadline can have higher priority [5].

S. Chakraborty and H. K. Kapoor et al. (2017) proposed a technique that turns off and on some on-chip last level cache (LLC) is used to reduce the heat that produces high leakage power. This technique is used to increase the performance and reliability of the system. The effect due to high temperature on chip causes various thermal issues due to high heat on chip the cooling cost also increases. When the temperature of the chip reduces to 4℃ a simultaneous 52% maximum savings in cache leakage occurs [6].

Inchoun Yeo describes a dynamic thermal management technique that is one of the most reliable technique to reduce and stabilize temperature of the multi-core system. DTM technique gives high performance as well as efficient reliability of the system. In a multi-core system exponentially decrease in the temperature also reduces the power utilization. DTM technique is a way to efficient to manage thermal responses of a processing systems. There are many techniques that are combined to manage temperature and thermal responses including “Dynamic Voltage and Frequency Scaling (DVFS)”, “Dynamic Power Management (DPM)” and “Dynamic Voltage Scaling (DVS)". These techniques are very useful but they cause some reliability and performance issues as well as they are mostly used to resolve on chip temperature and power problem. Dynamic voltage scaling is used to control the gradual increase in on chip power consumption by decreasing the power. Dynamic voltage scaling also reduces the temperature of the system which improves the performance and reliability of the system. Reducing errors by maintaining the systems voltage at run time can manage the gradual increase in on chip power consumption. Dynamic voltage scaling is commonly applied in the active state high power state while dynamic power management technique is functional to operate a multi core processor when the power is in lower state. When the chip is in idle mode by following the appropriate migration policies the overall performance and reliability of the system increases. If the policies are aggressive the temperature on chip is increasing and these policies causes high temperature cycle that reduces the overall system reliability [7].

Khalid Bati et al. (2013) proposed a dynamic thermal management technique for reducing the power of consumption of each core. This thermal aware mechanism for scheduling of various task by considering their ambient temperature for allocation of task to a scheduler and various frequency and voltage levels on the basis of utilization factor of a task. In this thermal aware scheduling technique the simulation was done on EDF scheduling algorithm [8].

Mehik proposed a thermal control technique that reduces thermal errors around 1.63℃ and consider hotspot by accurately measuring the temperature of the core using a sensor placement mechanism and select the most appropriate point for sensor placement [9]. As high temperature affects the reliability of the processor and causes various thermal issues. Dynamic thermal management is a techniques used to control and mange the thermal problem. For monitoring of temperature DTM technique is further classified as sensor placement technique on a processor and estimation of peak temperature on cores techniques this technique is measure the temperature efficiently because of offline phase. This is a thermal aware technique and reduces almost 4.5℃. Temperature in comparison to thermal unaware technique DTM is also used to avoid a thermal problem in cooling liquid technique and temperature aware task scheduling technique as well that is used in embedded devices [10].

II. Literature Review

B. Calhoun and A.Chandrakasan Introduces a static approach for interruption in information and workload which can be used to make algorithms for insertion of reconfiguration commands[11] T. Simunic, K. Mihic proposed that the power usage in the chip can be efficiently managed by using “Power management” technique that reduces the power consumption because all the cores that are not in working condition can be turned off due to which the performance of the system increases by decreasing the overall chip temperature the power consumption is also decreased. Due to replication of a single core configuration when the transition becomes among the two states when the power is high and from that state to a state when power is low these transitions can disturb the processor performance [12].

Inchoun Yeo describes (DTM) technique that is one of the most reliable way to reduce and stabilize system’s temperature and also helpful for the high performance as well as efficient reliability of the system. Due to exponentially decreased temperature the power utilization also reduces. DTM technique is a way to efficient to manage thermal responses of a processing systems now a days there are many techniques that are combined to manage temperature and thermal responses including “Dynamic Voltage and Frequency Scaling (DVFS)”, “Dynamic Power Management (DPM)”, “Dynamic Voltage Scaling (DVS)". These technique are very useful but they causes some reliability and performance issues. They are mostly used to resolve on chip temperature and power problem. Dynamic Voltage Scaling is used to control the gradual increase in on chip power consumption by decreasing the power. DVS also reduces the temperature of the system which improves the performance and reliability of the system by reducing errors by maintaining the systems voltage at run time it can manage the gradual increase in on chip power consumption. Dynamic voltage scaling is commonly applied in the active state while (DPM) technique is functional to operate a multi core processor when the power is in lower state. When the chip is in Ideal mode by following an appropriate procedure by following the appropriate policies the overall performance and system’s reliability increases as high temperature cycle can affect and decrease the overall system’s reliability if the policies that are followed are aggressive [13].

Joohno Kong, Sung Woo introduces power management that can have a very important impact in decreasing the temperature on chip because lower power consumption can affects the power densities there are many problems that occurs due to increase in temperature and power density e.g. electro migration is process that gets disturbed due to increase in temperature significantly electro-migration is affected by increased temperature while by reducing the temperature

dielectric breakdown process can be smoothly in working. On other hand for unmanaged thermal control thermal stabilization plays an important role to manage power [14].

Mehdi Kamal, discuss that that size of the chip is reduces certainly increasing the electronic element transistor on a chip. So the frequency and power densities are gradually increases that cause power consumption a most important issue.now a day's multicore systems are very efficent but due to increase in temperatue it can have power and thermal issues. Temperature gradients can be affected and imbalanced due to high peak temperature,the cooling cost can be increased due to high temperature the affect the system's performance and reliability so the power management technique and thermal management techniques can be used to have more reliable and high performance system on chip. Fan thermal packaging can be used for the thermal and power management but this is not a cost effective method while temperature aware energy efficient scheduling techniques is more efficient then fan thermal packaging because it is more reliable and lower in cost. A propose techniques is as follow dynamic thermal management techniques" DTM is both software and hardware low cost technique that can have decrease power utilization more reliable and it can have less impact on the system's performance. The most recent techniques like DTM, DVFS, DPM and integrated DVS doesn't account thermal cycle effects and also temperature gradients this is going to increases the systems reliability and performance while fetch toggling technique is a hardware technique which can increase the chip temperature because these hardware techniques such a clock gating do not consider appropriate information [16]. There are many dissimilar applications that perform differently and they have different temperature on chip machinery depending on their processing requirements. There are some application needs more intense CPU processing that creates more heat on chip and temperature on chip is increased as compared to those applications that doesn't need intense processing so the differentiation in temperature among the different chip components can be approximately 10℃.while there is a considerable difference in thermal characteristics of Individual core's in running mode in the chip can have different thermal characteristics for every individual core's because of the core's peak temperature [16].

Pratyush Kumar,Lothar Thiele introduces a power management techniques that can decrease the power consumption by turning off all the cores that are in idle state. A power management technique doesn't consider spatial gradients. Power management techniques can also reduces average power utilization and on chip temperature by keeping the idle cores turn off. Power management techniques can also enhance the performance and reliability and reduces gradually the hotspots that appear on the chip when the power consumption increase due to high power consumption the peak temperature on chip constantly increases. This technique doesn't consider Thermal cycles and temporal gradients which unfortunately affects the entire system reliability [17 18 19]. Embedded systems are those intelligent devices that are used due to the integration of software and hardware while software is working as a main graphical user interface that performs the smart system to perform specific jobs. Now a day's mostly embedded systems are operated on DC batteries. The design of embedded devices are facing few issues because the chip size is reduces so the chip can have certain challenges e.g. power consumption, reliability of the system, size and dimension of the embedded device, cost and performance. Processing unit needs to attain high performance by consuming less power is one of the most important design challenges in embedded systems. Moore's law states, 'in every eighteen months the electronic component transistors becomes double on chip and constantly increasing with time [20].

C. J. Lasance, describe that in a multi-core systems, a little difference in the temperature of the operating system from reduces almost 50% life span of embedded equipment because the difference in temperature can cool down the overall temperature on each core [21 22 23]. There are few deficiencies in previous studies like the effect of ambient temperature which leads temperature underestimation. Chips were designed without considering the ambient temperature. A study shows 1℃ increase in ambient temperature causes to increase the CPU and GPU temperature roughly 1.05℃ and 1.08℃ respectively an accurate prediction model to predict the temperature of destination core.

III. Problem Statement

The main objective and focus of this research work is chip (reliability) that is the most important issues in multi core embedded technologies. High temperature causes multiple performances and reliability issues. Task migration is the way to avoid high temperature and improve performance. However accurate prediction about the coolest core and the task which needs to migrate to control the chip temperature is the major design issue in task migration techniques. Our technique considers all types of tasks including hot and cold task to accurately predict the temperature of the core in running mode and also use preciously thermal history to precisely check the chip temperature for the selection of cold core. A task migration technique based on previous history by considering workload of running core to predict the future temperature and coolest cores. This technique improves the reliability by avoiding thermal issues.

III. Proposed Technique

A. Pseudo Code

Step1: Calculate the total number of tasks & divide the applications into periodic tasks
Step2: Determine Parameters include start time, worst case execution time, time period, priority, deadline and energy consumption
Step3:Count_time=0
Step4:Number_Core config_running=Select configuration of least used

1. (How many times a configuration is used)
2. (Which configuration is selected)
3. (Which configuration is currently running)
4. (Which core has maximum allowable temperature)
5. (Which core is in running mode)

TABLE 0:Pseudocode

```
Counter 1=Count_times
Config_k=number_core config
Config_R=number_core config_running
Config_N=next_core config_select
t1=max_temp_allowed of cores
t2=max_temp_running core
tmax=maximum_temp_configuration
minimum_counter=minimum value of counter
for(1 to total number of configuration)
If(number_coreconfig_running==number_core
config_Select)
Count_times++;
Else
No change in Values of counter
At each time Interval of Scheduler
If(Max_temp_Configuration < Max_temp_allowed)
{
No change}
elseif(Max_temp_configuration==Max_temp_allowed)
{
Continue with same
next_Core config_select <-Number_core config_select;
Change status from sleep mode to idle mode
}
else  if(Maximum_temp_Configuration==Max_temp_running
core)
Switch workload to next _core config-select;
{
number_core config_running=Next_core config_select
}
end if
end
```

IV. Experimental Technique

Experimental techniques contain the complete explanation regarding the experimental mechanism which is used in the research work. The block diagram of temperature controller model is shown in Figure 1. The major components include a task producer where user can creates random task sets in XML file that contains different parameter. This XML input file is used as an input for the simulation tool. The simulation tool for real-time multiprocessor scheduling can simulate the input file according to the scheduling policy and developed the power profiles according to the set of parameters given in XML file. These Power profiles generated from STORM can be saved in a text output file. The XML file contains all the information of task sets. A temperature model can also analyze the thermal responses of different scheduling algorithms. A statistical testing mechanism is used to test a many data sets. These data sets are already stored produces thermal profile when used with some hardware constraint in thermal model ATMI and a power model is used for each core comprises of static and dynamic power.

Total power = dynamic power + static power (I)

Dynamic power = $C \times F \times V$ (II)

Therefore C is the switching capacitance.

F is the frequency and V is the supply voltage

Static power = Leakage current × V (III)

TABLE I: The parameters of the chip

Parameters	Units	Meanings
z_1	M	Layer 1 Thickness
$d=z_2-z_1$	M	Layer 2 Thickness
K_1	W/mK	Layer 1 thermal conductivity
K_2	W/Mk	Layer 2 thermal conductivity
a_1	m^2/s	Layer 1 thermal diffusivity
a_2	m^2/s	Layer 2 thermal diffusivity
h_1	w/m^2k	Conductance b/w layer 1 & 2
h_2	w/m^2k	Conductance b/w layer 2 & ambient
L	M	Width

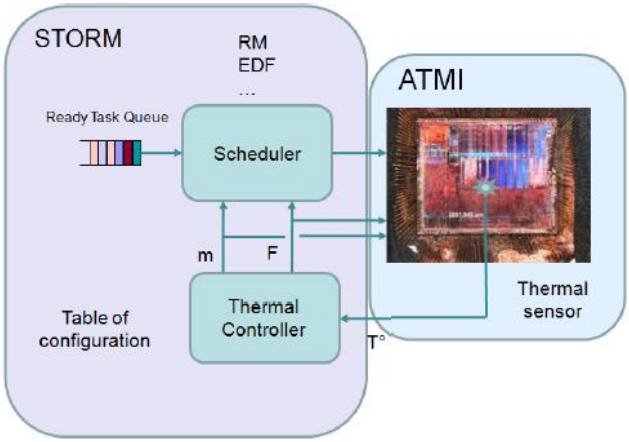

Figure 1: Block Diagram of Temperature controller Model

A. Flow chart

We have proposed technique for octa core multiprocessing Leat processor in which the scheduler will first check the number of task jobs that are running in an application. Primarily the value of counter is zero for all 8-cores in a multiprocessing leat processor. The scheduler is able to determine the constraint and values of every individual task. So the counter for all the cores is initially zero. The configuration of core will be selected on the basis of least temperature and lower Power of consumption among all other configurations once the core with least temperature is selected its counter in running mode is rapidly rising. In such case when the temperature of the core in running mode is less than the maximum allowable temperature then the scheduler will perform normal process of task execution. While in a situation when the core temperature in running mode is more than the thermal threshold value a temperature that is set maximum for the core in such situation select the configuration with least temperature and shift the selected configuration from idle mode to sleep mode and migrate all the tasks. The core is first shifted to idle mode from sleep mode to avoid delays and thermal threshold temperature value which is already set to reduce delays and migration cost. Once the workload will be migrated to the core that has least temperature the scheduler will start performing execution of job. In the proposed scheduler experiments are performed and set the ambient temperature at 25℃. The temperature of the core when it is in sleep mode is the current environmental temperature. When the value of current temperature is high then a

configuration with least temperature is used and all the other cores are remain in sleep mode.

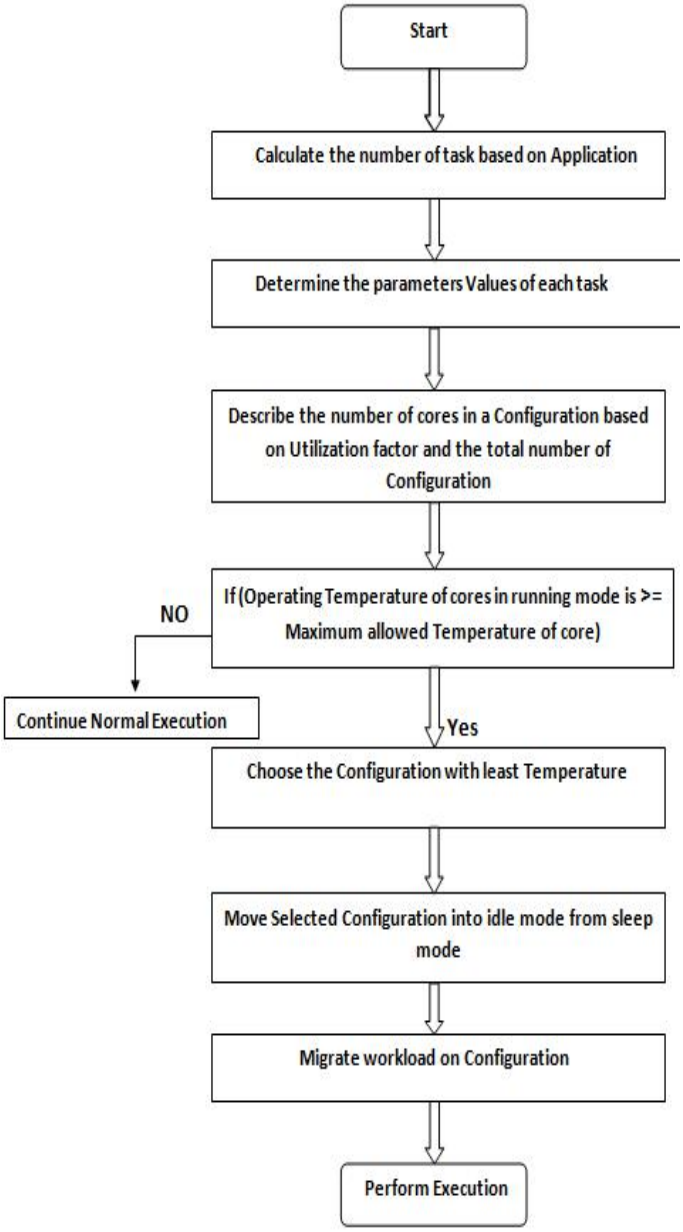

Figure 1.1: Flowchart

B. XML File

A XML input sample file is shown below. The simulation duration for this XML input file is 1000 that guides the simulation tool for a functional execution in milli seconds. A 'SCHED' scheduler is define, name and id's are assign to all 8-core that contains individual tasks and relevant parameter information given by the user in <TASKS> entity. The activation time, period, priority, Worst case execution and deadline of the entire task are given in XML file.

```
<SIMULATION duration="1000">
<SCHED
className="storm.Schedulers.EDF_P_Scheduler"></SCHED>
        <CPUS>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core1" id="1" ></CPU>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core2" id="2" ></CPU>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core3" id="3" ></CPU>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core4" id="4" ></CPU>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core5" id="5" ></CPU>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core7" id="7" ></CPU>
            <CPU
className="storm.Processors.LEATProcessor" name ="CPU
Core8" id="8" ></CPU>
        </CPUS>
        <TASKS>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T1"
id="9" period="10" activationDate="0" deadline="10"
WCET="1" priority="1"></TASK>s
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T7"
id="15" period="9" activationDate="2" deadline="4"
WCET="1" priority="6"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T8"
id="16" period="4" activationDate="4" deadline="20"
WCET="1" priority="7"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T9"
id="17" period="15" activationDate="0" deadline="40"
WCET="1" priority="8cl"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T10"
id="18" period="17" activationDate="2" deadline="20"
WCET="1" priority="5"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T11"
id="19" period="22" activationDate="4" deadline="20"
WCET="1" priority="10"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T12"
id="20" period="25" activationDate="0" deadline="30"
WCET="1" priority="1"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T13"
id="21" period="23" activationDate="2" deadline="20"
WCET="1" priority="5"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T14"
id="22" period="16" activationDate="4" deadline="20"
WCET="1" priority="10"></TASK>
            <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T15"
id="23" period="19" activationDate="2" deadline="20"
```

```
WCET="1"  priority="5"></TASK>
                    <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T16"
id="24" period="14" activationDate="4" deadline="10"
WCET="1"  priority="10"></TASK>
                    <TASK
className="storm.Tasks.PTask_NAM" name ="PTASK T1"
id="25" period="11" activationDate="0" deadline="15"
WCET="1"  priority="1"></TASK>
                    <TASK
   className="storm.Tasks.PTask_NAM" name ="PTASK T1"
id="26" period="14" activationDate="0" deadline="15"
WCET="1"  priority="1"></TASK>
                    <TASK
   className="storm.Tasks.PTask_NAM" name ="PTASK T1"
id="27" period="13" activationDate="0" deadline="11"
WCET="1"  priority="1"></TASK>
                    <TASK
   className="storm.Tasks.PTask_NAM" name ="PTASK T1"
id="28" period="15" activationDate="0" deadline="8"
WCET="1"  priority="1"></TASK>
                    <TASK
   </SIMULATION>
```

Figure: Sample XML File

V. Experimental Results

In this section we discuss our experimental results that illustrates the temperature variation between the curves of proposed EDF and Global EDF'. Proposed EDF considers reliability and performance parameter so only those cores are in running state that is in working condition. In the beginning exponentially temperature on chip rises and then arrive at a steady state level. At 10% utilization factor the global EDF has 5℃ more temperature on chip as compare to our proposed approach. Proposed EDF based on core configurations and using octa-core processor. At Low workload for 10%UF only 2-processors are in running mode while remaining 6-processors are in sleep mode. Our technique consumes less power than that of Global EDF and reduces almost 5℃ temperature on chip. X-axis depicts the time in milliseconds multiplied by 10^4 while y-axis represents the temperature in℃.

TABLE II: Configurations of cores

Frequency Mhz	Utilization Factor %	No of cores in running state	No of cores in sleep mode
100	0-9	1	7
100	9-18	2	6
100	18-24	3	5
100	24-34	4	4
100	34-45	5	3
100	45-54	6	2
100	54-62.5	7	1
100	>62.5	8	0

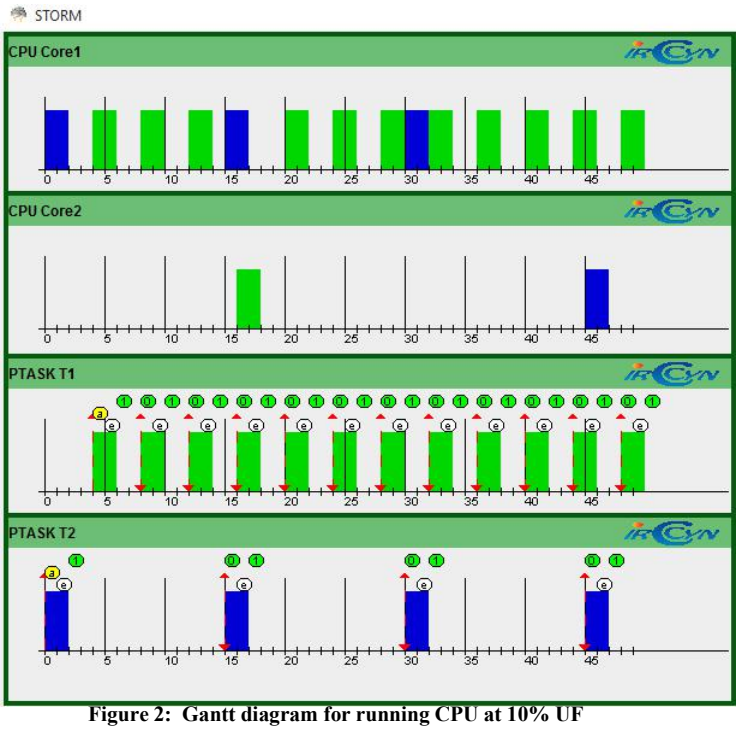

Figure 2: Gantt diagram for running CPU at 10% UF

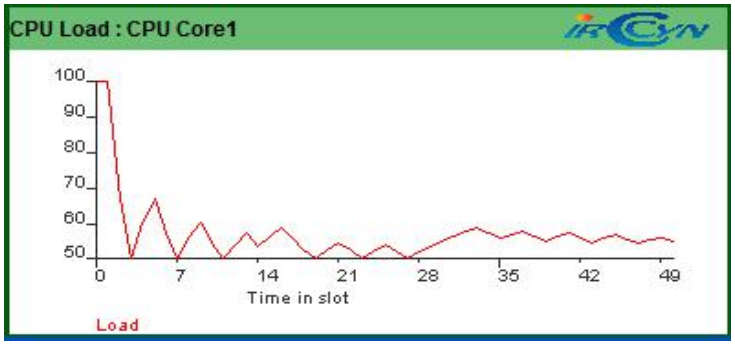

Figure 3: CPU Core 1 load at 10% UF

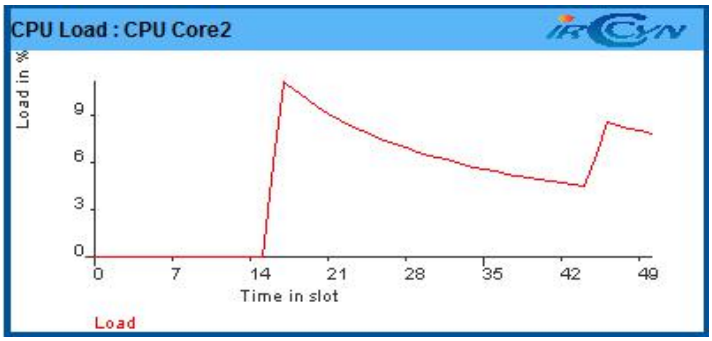

Figure 4: CPU Core 2 load at 10% UF

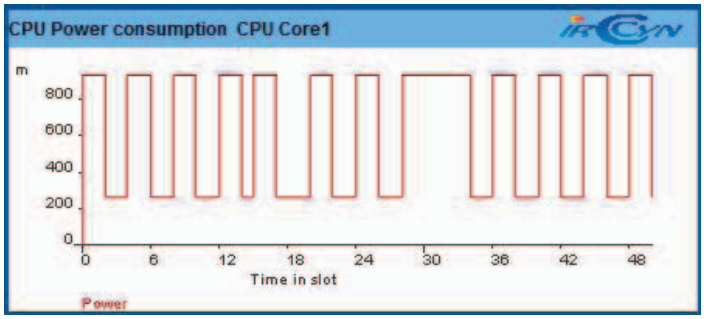

Figure 5 Power Consumption CPU Core 1 at 10% UF

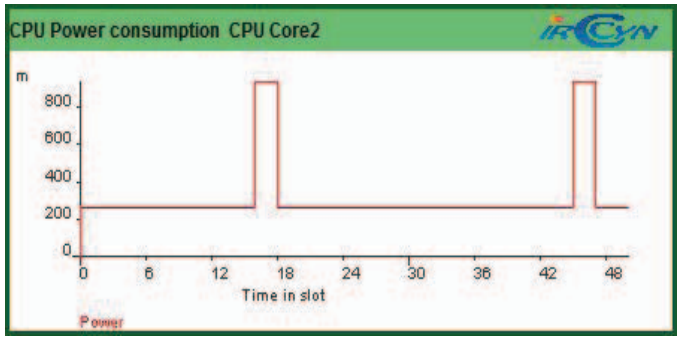

Figure 6 Power Consumption CPU Core 2 at 10% UF

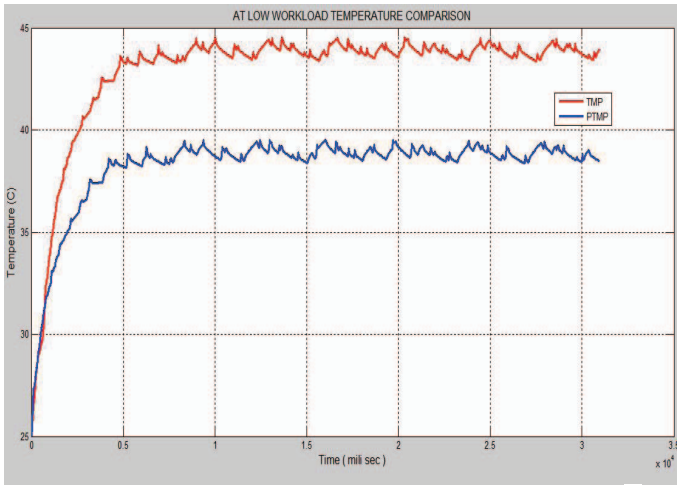

Figure 7: At low workload temperature's variation of core at 25℃ ambient temperature

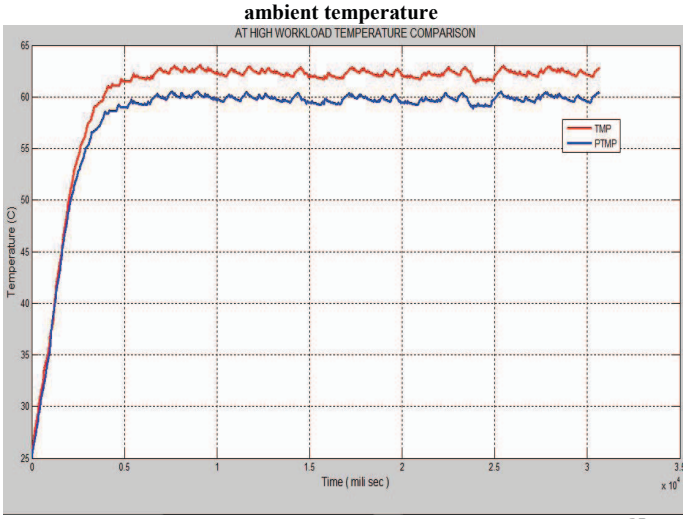

Figure 8: At high workload temperature's variation of core at 25℃ ambient temperature

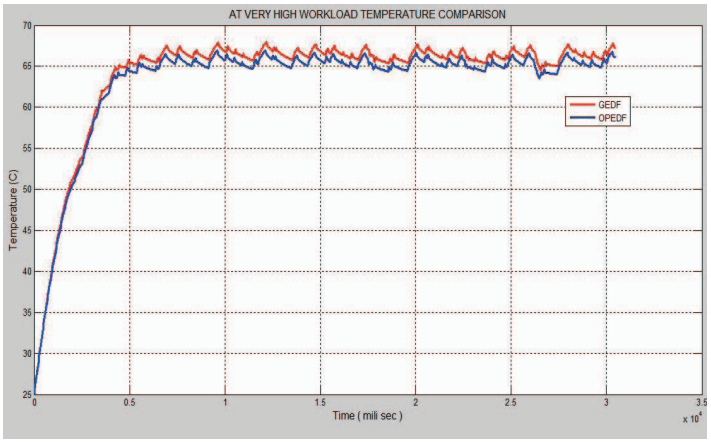

Figure 9: At very high workload temperature's variation of core at 25℃ ambient temperature

V I. Conclusion and Future Work

In this research work we have shown the significance of current ambient temperature variation when scheming a real times application systems by conside. a task migration mechanism is introduced that is based on multi core scheduling algorithm and also describes the overhead of this mechanism via functional simulation on STORM and thermal model and proved its practicability in the context of MPSoC. A large amount of techniques now a day's doesn't consider the affect of environmental temperature which can be investigated in future work. Majority of the current algorithms defines only for homogeneous multi-core systems which can be extensive to heterogeneous multi-core systems.

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References

[1] T. Afroze, "Temperature Sensitive Microprocessor Design to Reduce Heat Generation and Improve Performance," vol. 164, no. 3, pp. 1–8, 2017.

[2] H. Sun, P. Stolf, and J. Pierson, "Spatio-temporal thermal-aware scheduling for homogeneous high-performance computing datacenters," Futur. Gener. Comput. Syst., vol. 71, pp. 157–170, 2017

[3] A. Asad, O. Ozturk, M. Fathy, and M. R. Jahed-motlagh, "Microprocessors and Microsystems Optimization-based power and thermal management for dark silicon aware 3D chip multiprocessors using heterogeneous cache hierarchy," vol. 51, pp. 76–98, 2017.

[4] X. Mei, Q. Wang, and X. Chu, "A survey and measurement study of GPU DVFS on energy conservation ," Digit. Commun. Networks, vol. 3, no. 2, pp. 89–100, 2017.

[5] P. Wu and M. Ryu, “Best Speed Fit EDF Scheduling for Performance Asymmetric Multiprocessors,” vol. 2017, 2017.

[6] S. Chakraborty and H. K. Kapoor, “Towards Controlling Chip Temperature by Dynamic Cache Reconfiguration in Multiprocessors,” 2017.

[7] Inchoon Yeo and Eun Jung Kim, "Temperature-Aware Scheduler Based on Thermal Behaviour Grouping in Multicore Systems" in Proceedings of the Conference on Design, Automation and Test in Europe, pp. 946-951, 2009

[8] Khaled Baati, Michel Auguin, "Temperature-aware DVFS-DPM for Real Time Applications Under Variable Ambient Temperature," IEEE International Symposium on Industrial Embedded Systems, pp.13-20, 2013

[9] S. O. Mehik, R. Mukherjee,J. LONG, “Optimizing Thermal Sensor Allocation ForMicroprocessors”. IEEETransactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), vol. 27, no. 3,pp: 516-527 , 2008.

[10] E. Kursun, C. Y. Cher, Variation-Aware Thermal Characterization and Management Of Multi-Core Architectures. InProceedings of International Conference on Computer Design (ICCD ’08), 280-285, 2008.

[11] B. Calhoun and A. Chandrakasan. Ultra-dynamic voltage scaling (udvs) using subthreshold operation and local voltage dithering. In IEEE Journal of Solid-State Circuits, Vol. 41, No. 1, January 2006.

[12] T. Simunic, K. Mihic, G. De Micheli, “Reliability and Power Management of Integrated Systems", in Proceedings of Euromicro Symposium on Digital System Design, pp. 5–11, August, 2004.

[13] Inchoon Yeo and Eun Jung Kim, "Temperature Aware Scheduler Based on Thermal Behaviour Grouping in Multicore Systems" in Proceedings of the Conference on Design, Automation and Test in Europe, pp. 946-951, 2009

[14] Joohno Kong, Sung Woo Chung, Kevin Skadron, Recent Thermal Management Techniques for Microprocessors" ACM Computing Surveys, Vol. 44, No. 3, Article 13, pp. 13:1-13:42, June 2012

[15] Mehdi Kamal, A. Iranfar, A. Afzali-Kusha, M.Pedram,"A Thermal Stress-aware Algorithm for Power and Temperature Management of MPSoCs" In EDAA, 2015.

[16] J. Srinivasan, Jayanth, Sarita V.Adve, "Predictive Dynamic Thermal Management for Multimedia Applications," In ICS, pp. 23-26, 2003

[17] T. S. Rosing, K. Mihic, G. De Micheli, "Power and Reliability Management of SoCs,"In IEEE Transaction Very Large Scale Integrated System (VLSI), vol. 15. no.4, pp.391-403, 2007.

[18] Pratyush Kumar,Lothar Thiele,"Thermally Optimal Stop-GO Scheduling of Task Graphs with Real Time Constraints,"In ASP-DAC, IEEE Press, pp. 123-128, 2011.

[19] Alexandru Andrei, Petru Eles, Zebo Peng, Marcus T. Schmitz, Bashir M. Al Hashimi, "Energy optimization of multiprocessor systems on chip by voltage selection," IEEE Transaction on VLSI, vol 50, no.3, 2007.

[20] "1965 – "Moore's Law" Predicts the Future of Integrated Circuits". Computer History Museum, 2007

[21] C. J. Lasance, "Thermally Driven Reliability Issues in Microelectronic Systems: Status-quo and Challenges". Microelectronics Reliability, pp. 1969–1974, December 2003.

[22] C.H. Hsu, W. C. Feng, “ A power-aware run-time System for high-performance computing ,” In Proceedings of the 2005 ACM/IEEE conference e on Supercomputing. IEEE Computer Society,2005.

[23] G. Petrone, G. Seagnuolo, R. Teodorescu, '"Reliability Issues In Photovoltaic Power Processing Systems",IEEE Traansactions, July, 2008.