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Reliability study of high gain DC-DC converters based on RRPP I-IIA configuration for shipboard power system

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Abstract. This paper examines the family of high gain DC-DC converter derived from I-IIA configuration, primarily based on Reduced Redundant Power Processing (RRPP). The primary intention of this study is to determine the best topology for high voltage applications. The steady-state analysis of the proposed topologies is investigated and verified. The denominators of the voltage conversion ratio are observed to be similar for all the derived topologies, and they are in quadratic form. A comprehensive assessment is done based on voltage gain, voltage stress across storage element, switch stress voltage, switch utilization factor and inductor value. The best topology is identified and analyzed thoroughly in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Also, its performance evaluation and reliability study are also carried out. The advantage of that topology is validated using theoretical and simulation results. Finally, 40 W prototype is developed to verify the results.

Keywords. RRPP; I-IIA, voltage gain; voltage stress; efficiency; reliability.

1. Introduction

Currently, studies on Integrated Power System (IPS) for ships are increasing to integrate several modules such as Power Generation Modules (PGM), Power Distribution Modules (PDM), Power Conversion Modules (PCM), Energy Storage Modules (ESM), Propulsion Motor Modules (PMM) and Power Control Modules (PCON) in order to operate IPS efficiently [1]. DC zonal distribution in the shipboard power system is more advantageous compared to AC radial distribution owing to its difficulties in isolating the fault. Hence, an integrated power system with DC zonal distribution is the hot topic for researchers and the best option for shipboard power system [2]. The energy storage system in next-generation shipboard power supplies is batteries, ultra capacitor, fuel cell, etc. The Shipboard power system is given in figure 1.

All Electric Ship (AES) is the best way to power all the loads in the ship from the common electric platform [3]. IPS in all-electric ships will reduce the cost and provides flexibility in the system. Nowadays, submarines are incorporated with Medium Voltage DC (MVDC) integrated power system. DC-DC converter plays a vital role to supply power to the loads in the ship with MVDC shipboard power system. The presence of DC-DC converter can affect the power quality and stability of the system. So, PCM is designed to provide appropriate system stability [4]. Power electronic converter integrates the renewable energy sources and energy storage systems to the electric grid. Thus, it is necessary to work on the power electronic equipment to interface all the loads to the sources in the future AES.

Reduced Redundant Power Processing is introduced and used for PFC voltage regulator to improve its efficiency [5]. Prevention of reprocessing of power processed by one converter entirely by another converter is called Reduced Redundant Power Processing (RRPP). This technique is also used to derive quadratic step down DC-DC converters [6]. The attractive feature of this method is to avoid the power reprocessing and to improve the efficiency of the converter [7, 8]. A family of the quadratic step-up DC-DC converters is derived based on RRPP by avoiding the cascade connection in [9]. However, it is observed that in this case, the conversion ratio is quite low. The conversion ratios of the four derived topologies in [9] are equal to the voltage gain of the quadratic boost converter or lesser than QB converter. Modeling of the converters derived using RRPP is carried out in [10, 11], and its dynamic behavior is analyzed. Derivation of the high gain DC-DC converter using RRPP technique is not yet reported in the literature. The primary intent of this learning is to derive a topology using this method for high voltage applications. In this article, we derived four topologies (type I-IV) with RRPP based on I-IIA configuration in [5], and we analyzed the performance of all the topologies. Finally, we observed that type-IV topology is superior compared to other topologies. Type-IV topology is compared with the other

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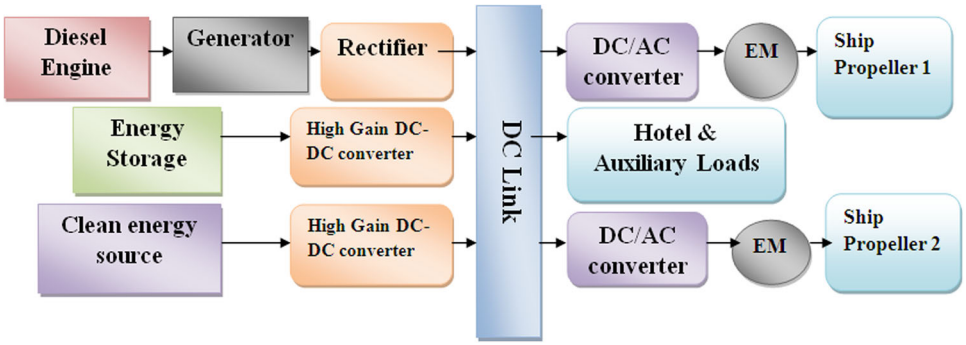


Figure 1. Shipboard power system.

high gain converter reported in the literature to prove its superiority.

This paper is organized as follows: In section 2, high gain dc-dc converter topologies are derived with RRPP based on I-IIA configuration. In section 3, the steady state operating conditions of the derived topologies are given. Type-IV topology is analyzed in section 4. In section 5, the comparative study is performed, and the best topology is obtained. Reliability study on type-IV topology is carried out and presented in section 6. Simulation and experimental results are offered in section 7. Conclusions are provided in section 8.

2. Proposed converters with RRPP

Figure 2 gives the I-IIA configuration chosen out of 16 possible configurations [5]. By using I-IIA configuration, four topologies are derived. They are shown in figures 3(a)-(d) and named as types I-IV.

Type-I topology is attained by using super lift boost converter [12] as converter A and Boost converter as converter B, and it is given in figure 3(a). Figure 3(b) shows the type-II topology, and it is derived by considering modified sepic converter [13] as converter A and Boost converter as converter B. Type-III is achieved by integrating elementary Luo converter [14] as converter A and Boost converter as converter B and it is presented in figure 3(c). Figure 3(d) shows the type-IV topology, and it is acquired by using boost converter as converter A and boost converter with Voltage Multiplier (VM) as converter B [15].

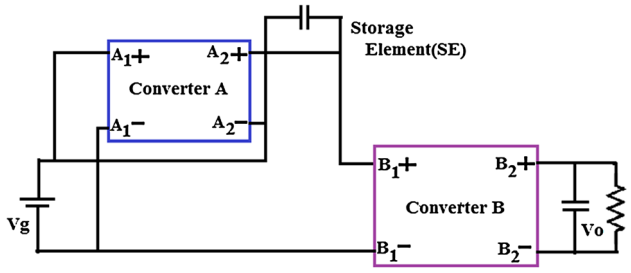


Figure 2. I-IIA configuration.

3. Steady state analysis of the proposed topologies

The steady state analysis is carried out for all the topologies (type-I-IV), and their modes of operation are given in figures 4-7. The voltage gain of the converter is obtained by applying volt-sec balance principle on the inductor. Figure 8 gives the voltage across the inductor, and figures 8(i)-(iv) present the inductor voltage of type-I –IV, respectively.

3.1 *Type-I topology*

Figure 4 is the type-I topology derived from the super lift converter and the boost converter. ON and OFF modes of the converter are given in figures 4(i) and (ii).

Mode (i): Inductors L_1 and L_2 are charged equivalently by the source voltage Vg in ON mode. Inductor L_3 is charged by the source voltage and capacitor voltage Vc. The voltage across the capacitor Co is delivered to the load. Diodes D_3, D_4, and D_O are OFF in this state.

Mode (ii): When the switches S_1 and S_2 are turned OFF in this mode, diodes D_1 and D_2 are reverse biased. The output voltage is equal to the sum of the source voltage and voltage across inductors L_1, L_2, and L_3.

Applying volt-sec balance principle on inductors L_1 and L_2

$$\frac{1}{T_S}\left[\int_0^{DT_s} 2V_g\,dt + \int_{DT_s}^{T_s} -V_C\,dt = 0\right] \quad (1)$$

Applying volt sec balance principle on the inductor L_3

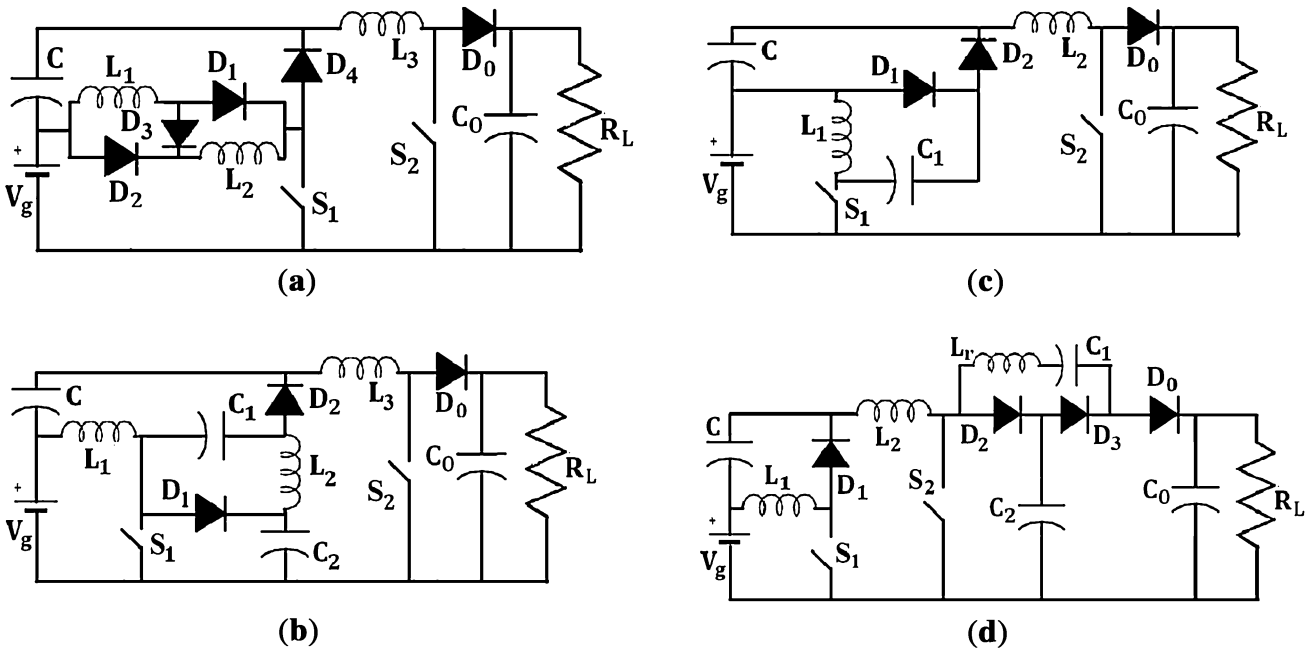


Figure 3. (**a**) Type-I topology, (**b**) Type-II topology, (**c**) Type-III topology and (**d**) Type-IV topology.

$$\frac{1}{T_S}\int_0^{DT_s}(V_g+V_C)dt+\int_{DT_s}^{T_s}(V_g+V_C-V_O)dt=0 \quad (2)$$

By simplifying (1) and (2), voltage conversion ratio is obtained as

$$V_C=\frac{2V_gD}{1-D} \quad (3)$$

$$G_{V-I}=\frac{V_O}{V_g}=\frac{1+D}{[1-D]^2} \quad (4)$$

3.2 *Type-II topology*

Figure 5 gives the type-II topology derived from the modified sepic and boost converter. ON and OFF modes are set out in figures 5 (i) and (ii), respectively.

Mode (i): Inductor L_1 is charged by the source voltage. Inductor L_2 is charged by the capacitors C_1 and C_2. Source voltage and capacitor voltage Vc charges the inductor L_3. The output voltage is delivered by the output capacitor Co.

Mode (ii): when the switch S_1 and S_2 are turned OFF, the reversed polarity of the voltage in the inductors L_1 and L_3 will forward bias the diodes D_1 and D_O, respectively. Diodes D_2 is turned on due to the voltage across capacitor C_1.

Applying volt-sec balance principle on the inductor L_1, L_2 and L_3

$$\frac{1}{T_S}\int_0^{DT_s}V_gdt+\int_{DT_s}^{T_s}(V_g-V_{C2})dt=0 \quad (5)$$

$$\frac{1}{T_S}\int_0^{DT_s}(V_{C1}-V_{C2})dt+\int_{DT_s}^{T_s}V_{C1}dt=0 \quad (6)$$

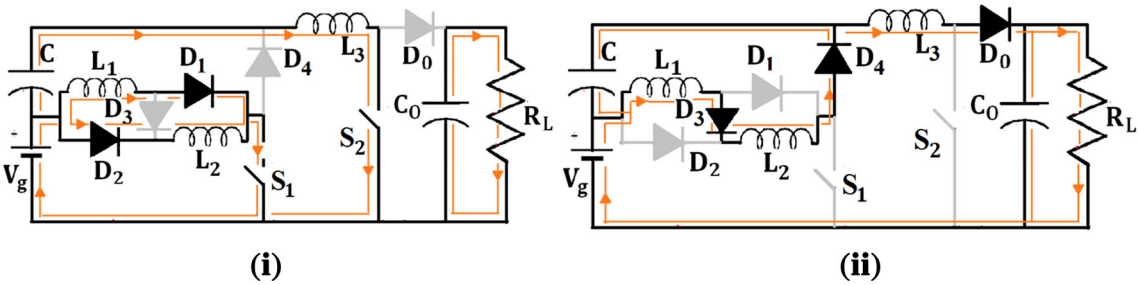


Figure 4. Type-I-Superlift/Boost converter; (i) ON mode and (ii) OFF mode.

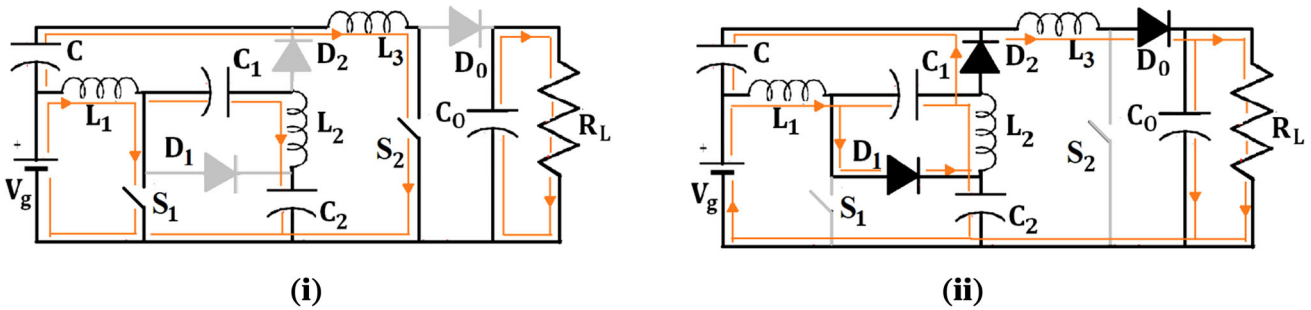


Figure 5. Type-II-Modified Sepic/Boost converter; (i) ON mode and (ii) OFF mode.

$$\frac{1}{T_S}\int_0^{DT_s}(V_g+V_C)dt+\int_{DT_s}^{T_s}(V_g+V_C-V_O)dt\ =0 \quad (7)$$

By simplifying (5), (6) and (7), voltage conversion ratio is obtained as

$$V_C=\frac{2V_gD}{1-D} \quad (8)$$

$$G_{V-II}=\frac{V_O}{V_g}=\frac{1+D}{[1-D]^2} \quad (9)$$

3.3 *Type-III topology*

Mode (i): Switches S_1 and S_2 are turned ON in this mode. Inductor L_1 is charged by the source voltage. Inductor L_2 is charged by the capacitor C and Source voltage Vg. The voltage across the capacitor forward biases the diode D_1. The output voltage is delivered by the output capacitor Co.

Mode (ii): When the switch S_1 and S_2 are turned OFF, the reversed polarity of the voltage in the capacitor C_1, forward bias the diode D_2 and reverse biases the diode D_1. Diode Do turns ON due to the voltage across the inductor L_2. Figures 6 (i) and (ii) give the current path of the shoot through and non- shoot through mode of the type-III topology.

Employing volt-sec balance principle on the inductors L_1 and L_2

$$\frac{1}{T_S}\int_0^{DT_s}V_gdt+\int_{DT_s}^{T_s}(V_{C1}-V_C)dt\ =0 \quad (10)$$

$$\frac{1}{T_S}\int_0^{DT_s}(V_g+V_C)dt+\int_{DT_s}^{T_s}(V_g+V_C-V_O)dt=0 \quad (11)$$

By simplifying (10) and (11), voltage conversion ratio is obtained as

$$V_C=\frac{V_g}{1-D} \quad (12)$$

$$G_{V-III}=\frac{V_O}{V_g}=\frac{2-D}{[1-D]^2} \quad (13)$$

3.4 *Type-IV topology*

There are multiple modes for type-IV topology. Only two predominant modes are taken for steady-state analysis to derive the voltage gain, and their modes of operation are given in figures 7 (i) – (iv). Currents through all the components in the type-IV topology are presented in figure 7 (v). Table 1 gives the average and maximum voltage of the

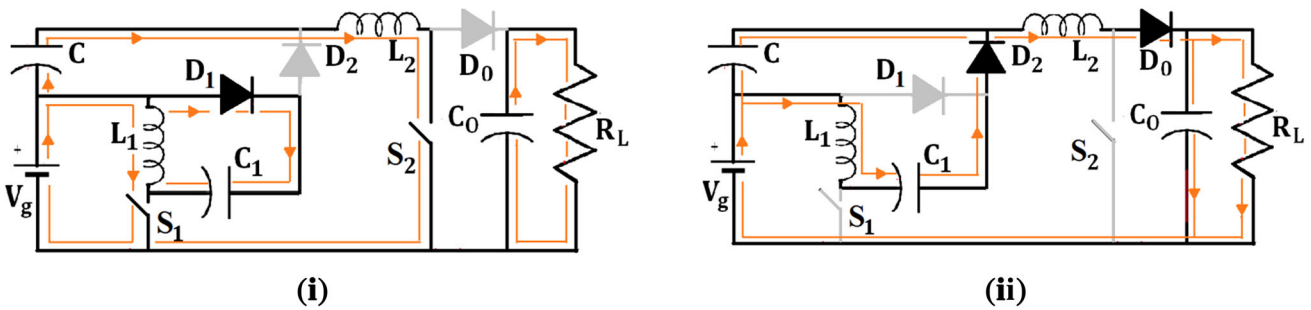


Figure 6. Type-III-Elementary LUO/Boost converter **(i)** ON mode and **(ii)** OFF mode.

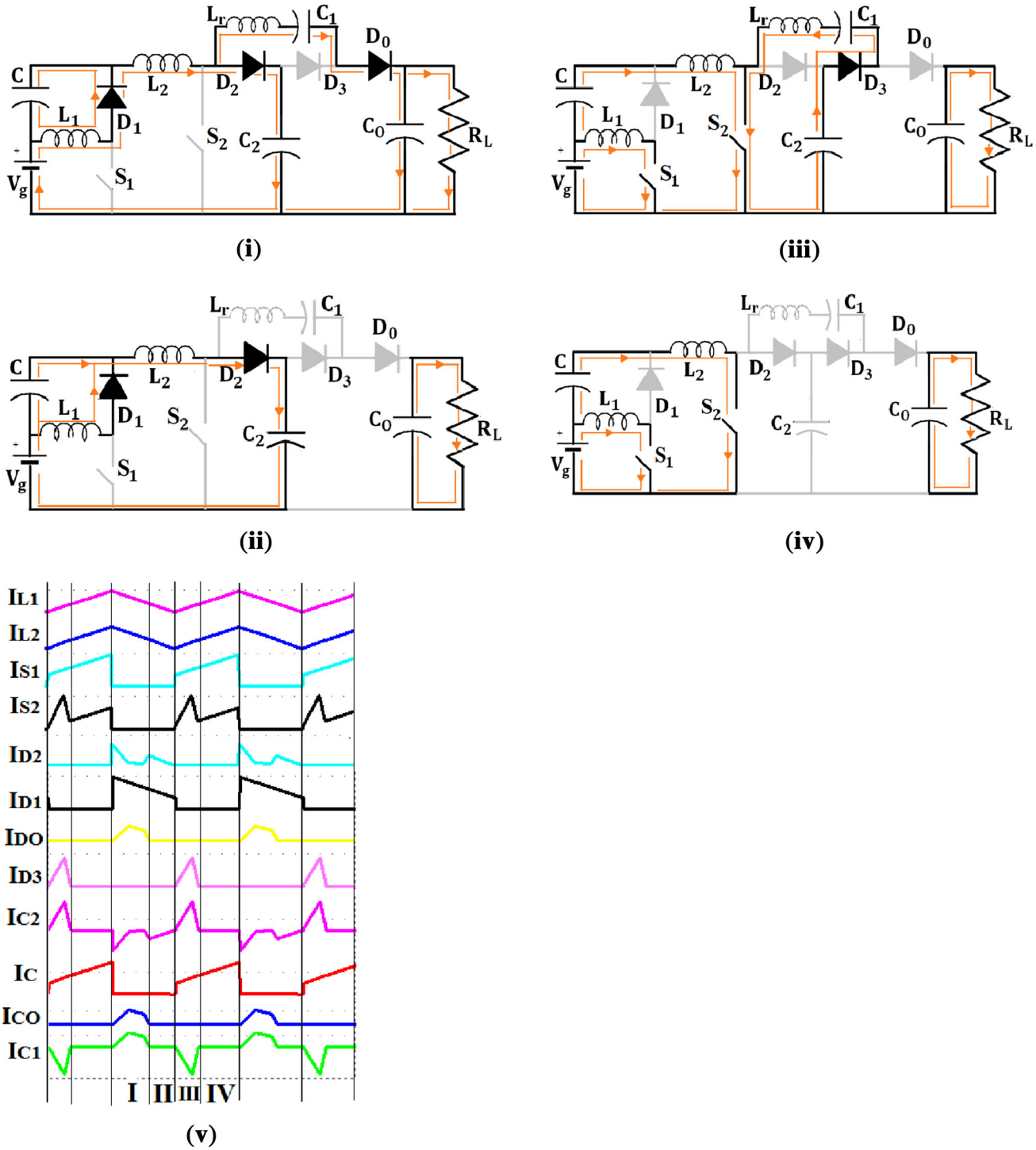


Figure 7. Type-IV topology-Boost/Boost with voltage multiplier converter; **(i)** Mode-I, **(ii)** Mode-II, **(iii)** Mode-III, **(iv)** Mode-IV and **(v)** Current waveforms of the components in Type-IV topology.

semiconductor devices and other components of the type-IV converter.

Mode (i): Switches S_1 and S_2 are OFF in this mode. Energy stored in the inductor L_1 is moved to the capacitor C. The energy stored in the inductor L_2 is transferred to the capacitor C_2, and to the output capacitor C_O through diode D_O. The voltage across C and C_2 forward biases the diode D_1 and D_2, respectively. The output voltage is equivalent to the sum of the voltages across capacitor C_1 and C_2.

Mode (ii): The current resonant inductor and capacitor C_1 go to zero. As a result of this, the current through the diode D_O goes zero, and it gets reverse biased. The voltage

Table 1. Average and maximum voltage and current of the components in the type-IV converter.

Parameter		Type-IV topology
Voltage stress of the diodes in voltage multiplier cell	D_2 D_3	$\frac{V_O}{M+1}$
Voltage stress of the Switch	S_1	$\frac{V_g}{1-D}$
	S_2	$\frac{V_O}{M+1}$
Voltage stress of the diodes in boost converter	D_1	$\frac{V_g}{1-D}$
Average voltage of the diodes in boost converter	D_1	$\frac{V_gD}{1-D}$
Average voltage of the diodes in voltage multiplier cell	D_2	$\frac{V_OD}{M+1}$
	D_3	$\frac{V_O[1-D]}{M+1}$
Average voltage of the switch	S_1	$\frac{V_gD}{1-D}$
	S_2	$\frac{V_OD}{M+1}$
Average current of the switch	S_1	$\frac{2I_OD}{[1-D]^2}$
	S_2	$\frac{2I_O[2-D]D}{1-D}$
Average Inductor current	L_1	$\frac{2I_O}{[1-D]^2}$
	L_2	$\frac{2I_O}{1-D}$
Average current of the diodes in voltage multiplier cell	D_2 D_3	$2I_OD$
Average current of the diodes in QB	D_1	$\frac{2I_O}{1-D}$
Average current of the output diodes	D_O	$2I_O[1-D]$

across the capacitor Co is applied across the load. Energies in the inductor L_1 and L_2 are transferred to the capacitor C and C_2, respectively.

Mode (iii): Switches S_1 and S_2 are turned ON in this mode. The voltage across C and C_2 reverse bias the diodes D_1 and D_2, respectively. Diode D_3 is forward biased due to the upper plate positive of the capacitor C_2 and the diode D_O is blocked. Inductor L_1 is charged by the source voltage Vg. Inductor L_2 is charged by the source voltage Vg and the capacitor voltage Vc. Inductor L_r is used to minimize the commutation loss. The voltages across C_1 and C_2 are equal. The voltage across the capacitor Co is connected to the load.

Mode (iv): Current through the resonant inductor is zero, and the diode D_3 is still blocked. Inductors L_1 and L_2 store the energy through the switches S_1 and S_2, respectively.

Employing volt-sec balance principle on the inductors L_1 and L_2

$$\frac{1}{T_S}\int_0^{DT_s} V_g dt + \int_{DT_s}^{T_s} -V_C dt = 0 \tag{14}$$

$$\frac{1}{T_S}\int_0^{DT_s} (V_g + V_C)dt + \int_{DT_s}^{T_s} \left(V_g + V_C - \frac{V_O}{2}\right)dt = 0 \tag{15}$$

By simplifying (14) and (15), voltage conversion ratio is obtained as

$$V_C = \frac{V_gD}{1-D} \tag{16}$$

$$G_{V-IV} = \frac{V_O}{V_g} = \frac{M+1}{[1-D]^2} \tag{17}$$

4. Analysis of Type-IV topology

Since the gain of the type-IV topology is high compared to other topologies, the analysis is carried out to test the superiority of this topology.

4.1 *Steady-state analysis in DCM*

Figure 9 shows the inductor waveform of the proposed converter in discontinuous conduction mode. The condition for inductor L_1 to operate in CCM as follows,

$$I_{L1} > \frac{\Delta i_{L1}}{2} \tag{18}$$

$$\frac{[M+1]I_O}{[1-D]^2} > \frac{V_O[1-D]^2D}{2[M+1]f_SL_1}$$

$$\frac{2L_1f_S}{R_L} > \frac{D}{G_{V-IV}^2} \tag{19}$$

$$K_{L1} > \frac{D}{G_{V-IV}^2}; K_{CRIC}(D) = \frac{D}{G_{V-IV}^2} \tag{20}$$

The condition for inductor L_2 to operate in CCM as follows,

$$I_{L2} > \frac{\Delta i_{L2}}{2} \tag{21}$$

$$\frac{[M+1]I_O}{[1-D]} > \frac{V_O[1-D]^2D}{2[M+1][1-D]f_SL_2}$$

$$K_{L2} > \frac{D}{[M+1]G_{V-IV}^2}; K_{CRIC}(D) = \frac{D}{[M+1]G_{V-IV}^2} \tag{22}$$

The proposed converter enters into DCM when the K_{L1} and K_{L2} values are less than the K_{CRIC} as given in equations (20) and (22). Applying volt-second balance principle, the conversion ratio of the proposed converter in DCM is obtained as follows,

The dc component of the voltage applied to an inductor L_1 is equal to zero.

$$V_gD - V_CD_C = 0 \tag{23}$$

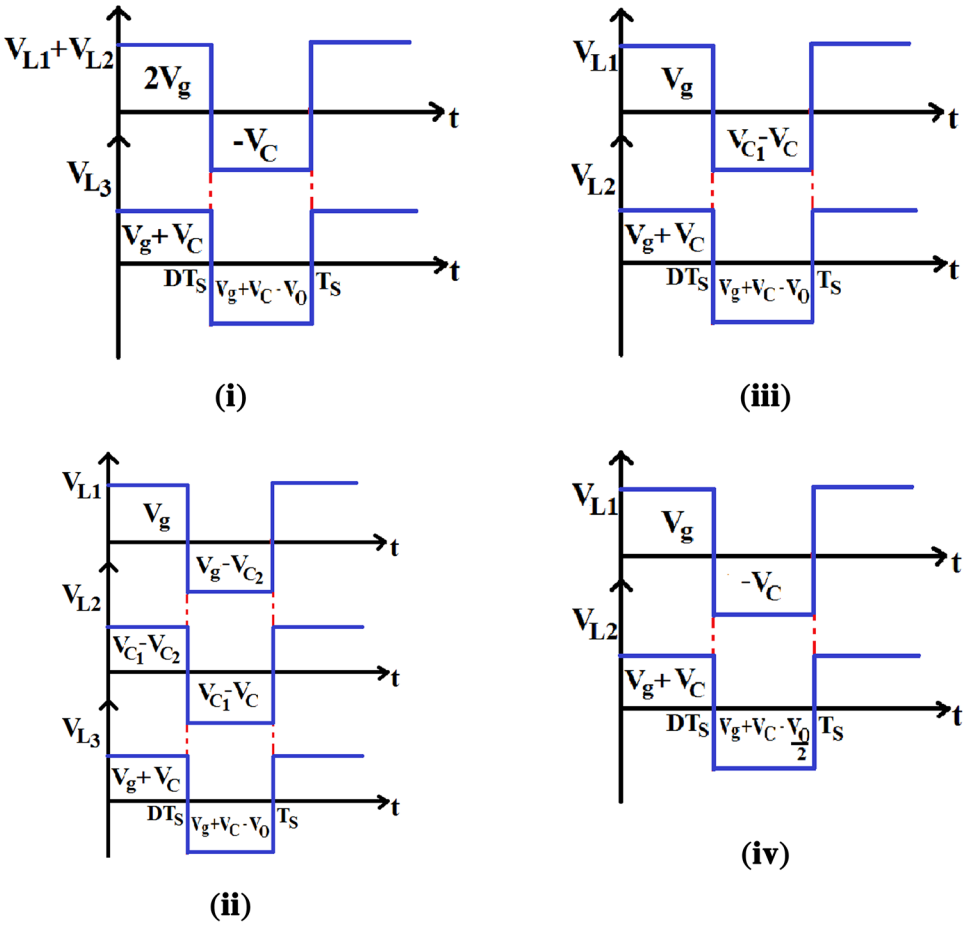


Figure 8. Inductor Voltages; **(i)** Type-I, **(ii)** Type-II, **(iii)** Type-III and **(iv)** Type-IV.

$$V_C = \frac{V_g D}{D_C}$$

The dc component of the voltage applied to an inductor L_2 is equal to zero.

$$[V_g + V_C]D + [V_g + V_C - V_{C2}] = 0 \tag{24}$$

$$V_{C2} = \frac{V_g[D + D_C]^2}{D_C^2}$$

Since the output voltage is equal to the sum of capacitor voltage C_1 and C_2 .The voltage conversion ratio in DCM is obtained as

$$\frac{V_O}{V_g} = [M + 1]\left[1 + \frac{D}{D_C}\right]^2 \tag{25}$$

4.2 *Efficiency and transient analysis*

Figure 10 presents the circuit diagram of type-IV topology with parasitic resistance to perform efficiency analysis. To determine the efficiency of the proposed converter, RMS current through all the components are determined, and losses are calculated.The RMS current switches S_1 and S_2 are

$$i_{S1rms} = \frac{2I_O\sqrt{D}}{[1 - D]^2} \tag{26}$$

$$i_{S2rms} = \frac{2I_O[2 - D]\sqrt{D}}{1 - D} \tag{27}$$

Hence, the conduction power loss in switch is

$$P_{SW} = i_{S1rms}^2 r_{DS} + i_{S2rms}^2 r_{DS} \tag{28}$$

The RMS current through the diodes are given as

$$i_{D1rms} = \frac{2I_O}{[1 - D]\sqrt{1 - D}} \tag{29}$$

$$i_{D2rms} = 2I_O\sqrt{D} \tag{30}$$

$$i_{D3rms} = \frac{2I_O D}{\sqrt{1 - D}} \tag{31}$$

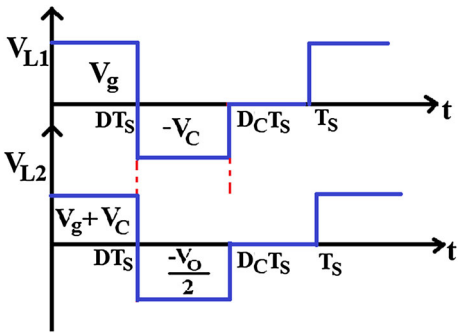


Figure 9. Inductor voltage waveform in DCM.

$$i_{D0rms} = 2I_O\sqrt{1-D} \tag{32}$$

The power loss due to forward resistance in diode is

$$P_{RF} = \left[i^2_{D1rms} + i^2_{D2rms} + i^2_{D3rms} + i^2_{D0rms}\right]R_F \tag{33}$$

The average current through the diode can be given by

$$i_{D1avg} = \frac{2I_O}{1-D} \tag{34}$$

$$i_{D2avg} = 2I_OD \tag{35}$$

$$i_{D3avg} = 2I_OD \tag{36}$$

$$i_{D0avg} = 2I_O[1-D] \tag{37}$$

The power loss owing to forward voltage drop in diode is given by

$$P_{VF} = V_F\left[i_{D1avg} + i_{D2avg} + i_{D3avg} + i_{D0avg}\right] \tag{38}$$

From equations (25), (30) total power loss in diodes is obtained as

$$P_D = P_{RF} + P_{VF} \tag{39}$$

RMS value of the inductor currents are

$$i_{L1rms} = \frac{2I_O}{[1-D]^2}; i_{L2rms} = \frac{2I_O}{1-D}; i_{Lrms} = 2I_O \tag{40}$$

Power loss related to inductor is drawn from the equation (40)

$$P_L = i^2_{L1rms}r_{L1} + i^2_{L2rms}r_{L2} + i^2_{Lrms}r_{Lr} \tag{41}$$

Capacitor power losses can be derived similarly, and it is given as

$$P_C = i^2_{Crms}r_C + i^2_{C1rms}r_{C1} + i^2_{C2rms}r_{C2} \tag{42}$$

Total power loss of the type-IV topology is

$$P_{LOSS} = P_{SW} + P_D + P_L + P_C \tag{43}$$

The efficiency of the proposed high step-up converter is given by

$$\text{Efficiency} = \eta = \frac{P_0}{P_{in}} = \frac{1}{1 + (P_{LOSS}/P_0)} \tag{44}$$

Figure 11(a) presents the simulation results of type-IV topology for the step change in input voltage. It is identified that overshoot is not much high and the settling time of the converter is also very low. Figure 11(b) shows the losses of the type-IV topology in percentage for the chosen power rating. The efficiency of the converter for that power rating is 90.5%. Since the number of the diode is more compared to other components, the diode loss is the significant loss in the proposed topology. In addition to that, the efficiency analysis is also carried out for 200 W, 220 V and it is observed that the efficiency decreases slightly with the higher power rating and it is approximately equal to 87.5%.

5. Comparison of the proposed topologies

In this phase, the proposed topologies are compared with the few converters reported in the literature and additionally among the derived topologies. All the derived

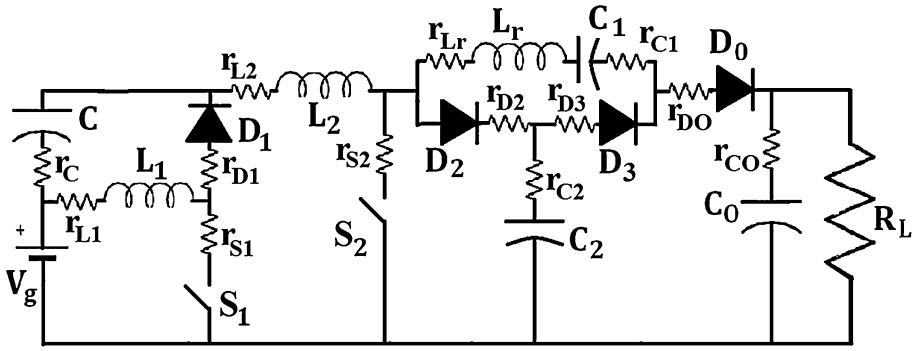


Figure 10. Efficiency analysis circuit of type-IV topology.

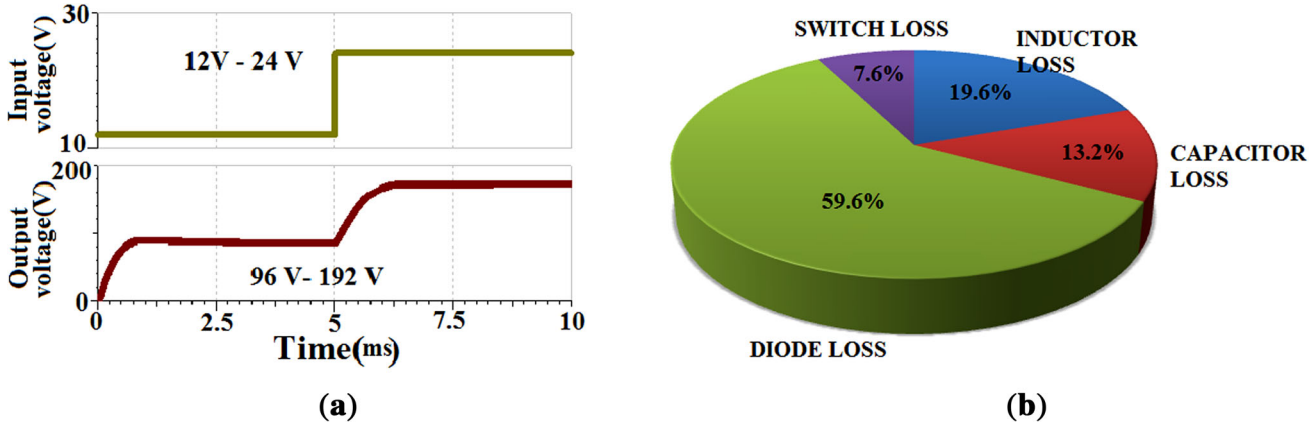


Figure 11. (**a**) Output response of type-IV topology with step change in input, **(b)** Power loss analysis.

Table 2. Comparison of proposed topologies with converters reported in literature.

Converters	Voltage gain	Number of Inductor	Number of switch	Number of diode	Number of capacitor	Total number of components
Type-I	$\frac{1+D}{[1-D]^2}$	3	2	5	2	**12**
Type-II	$\frac{1+D}{[1-D]^2}$	3	2	3	4	**12**
Type-III	$\frac{2-D}{[1-D]^2}$	2	2	3	3	**10**
Type-IV	$\frac{M+1}{[1-D]^2}$	2	2	4	4	**12**
Converter in [16]	$\frac{2}{1-D}$	3	2	3	4	**12**
Converter in [17]	$\frac{5-D}{1-D}$	4	4	5	5	**19**
Converter in [18]	$\frac{2}{[1-D]^2}$	3	2	5	4	**14**

topologies from type-I-IV are compared with voltage lift converters reported in [16–18]. Table 2 gives the comparison of the proposed topologies with the converters in literature. From the comparison, it is observed that,

- The voltage conversion ratios of type-I to type-IV are found to be well-compared to the converters in [16, 18].
- The entire device components of all the derived topologies are less than or equal to the converters in [16–18]. In type-IV topology, resonant inductor Lr is

Table 3. Comparison of voltage stress across semiconductor devices.

Parameter	Converter in [16]	Converter in [17]	Converter in [18]	Type-IV topology
Po = 40 W, Vg = 12 V, Vo = 96 V				
Switch Voltage stress	$V_{S1} = \frac{V_g}{1-D}$ $V_{S2} = \frac{V_g}{1-D}$	$V_{S1} = \frac{V_g}{1-D}$ $V_{S2} = V_O$	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = \frac{V_O - V_g}{4}$	$V_{S1} = \frac{V_g}{1-D}$ $V_{S2} = \frac{M+1}{[1-D]^2}$
	48V, 48V	24 V,96 V	21 V(switches)	24 V, 48 V
Diode Voltage stress	$V_{D1} = V_{D1} = \frac{V_g}{1-D}$ $V_{D3} = V_O$	$V_{D1} = V_{D1} = V_{D3} = V_{D4} = \frac{V_g}{1-D}$ $V_{D5} = V_O$	$V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{V_O - V_g}{4}$ $V_{D5} = V_O - V_g$	$V_{D1} = \frac{V_g}{1-D}$ $V_{D2} = V_{D3} = V_{DO} = \frac{V_O}{M+1}$
	48V,(2diodes),96V	24 V(4diodes), 96 V	21V(4 diodes), 84V	24 V,48V(3 diodes)

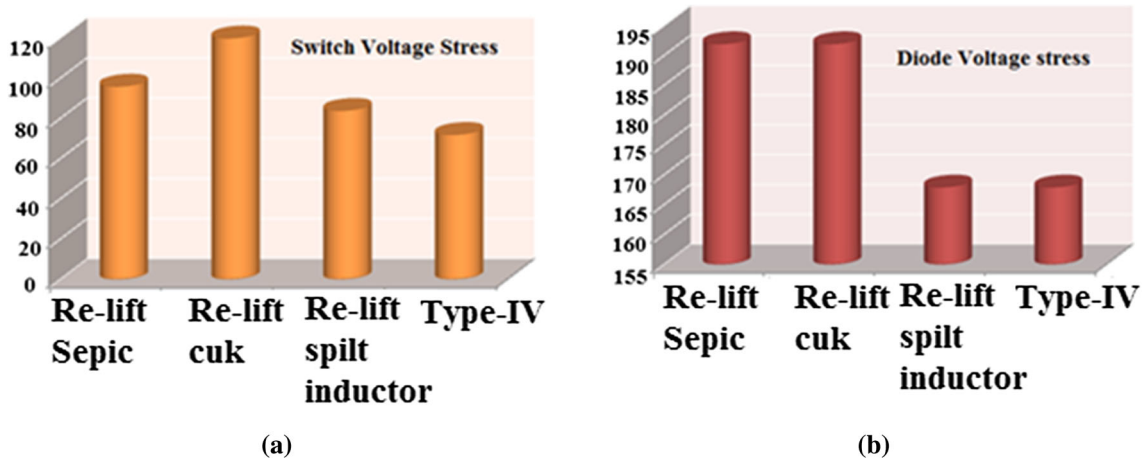


Figure 12. (**a**) Switch voltage stress, **(b)** Diode voltage stress.

Table 4. Comparison of proposed topologies.

Parameter	Type-I	Type-II	Type-III	Type-IV
No. of Inductor	3	3	2	2
No. of Capacitor	2	4	3	4
No. of Diode	5	3	3	4
No. of switch	2	2	2	2
Voltage gain	$\frac{1+D}{[1-D]^2}$	$\frac{1+D}{[1-D]^2}$	$\frac{2-D}{[1-D]^2}$	$\frac{M+1}{[1-D]^2}$
Voltage across Storage Element (SE) V_C	$\frac{2V_gD}{1-D}$	$\frac{2V_gD}{1-D}$	$\frac{V_g}{1-D}$	$\frac{V_gD}{1-D}$
Switch voltage stress (S_1)	$\frac{V_g[1+D]}{1-D}$	$\frac{V_g}{1-D}$	$\frac{V_g}{1-D}$	$\frac{V_g}{1-D}$
Switch voltage stress (S_2)	V_O	V_O	V_O	$\frac{V_g}{[1-D]^2}$
CAPACITOR VOLTAGE				
V_{C1}	$\frac{2V_gD}{1-D}$	$\frac{2V_gD}{1-D}$	$\frac{V_g}{1-D}$	$\frac{V_gD}{1-D}$
V_{C2}	—	$\frac{V_gD}{1-D}$	V_g	$\frac{V_g}{[1-D]^2}$
V_{C3}	—	$\frac{V_g}{1-D}$	—	$\frac{V_g}{[1-D]^2}$
V_{C0}	V_O	V_O	V_O	V_O
INDUCTOR CURRENT				
I_{L1}	$\frac{I_O}{[1-D]^2}$	$\frac{[1+D]I_O}{[1-D]^2}$	$\frac{I_O}{[1-D]^2}$	$\frac{2I_O}{[1-D]^2}$
I_{L2}	$\frac{I_O}{[1-D]^2}$	$\frac{I_O}{1-D}$	$\frac{I_O}{1-D}$	$\frac{2I_O}{1-D}$
I_{L3}	$\frac{I_O}{1-D}$	$\frac{I_O}{1-D}$	—	—
INDUCTOR DESIGN				
L_1	$\frac{R_L[1-D]^4D}{2[1+D]f_S}$	$\frac{R_L[1-D]^4D}{2[1+D]^2f_S}$	$\frac{R_L[1-D]^4D}{2[2-D]f_S}$	$\frac{R_L[1-D]^4D}{4f_S}$
L_2	$\frac{R_L[1-D]^4D}{2[1+D]f_S}$	$\frac{R_L[1-D]^3D}{2[1+D]f_S}$	$\frac{R_L[1-D]^2D}{2f_S}$	$\frac{R_L[1-D]^2D^2}{4f_S}$
L_3	$\frac{R_L[1-D]^2D}{2f_S}$	$\frac{R_L[1-D]^2D}{2f_S}$	—-	—
SWITCH ULTILIZATION FACTOR Vg = 12 V; V_O = 84 V;Po = 40 W				
Switch Voltage(S_1, S_2)	27.28 V, 84 V	25.64 V, 84 V	26.31 V, 84 V	22.42 V,41.92 V
Switch current (S_1, S_2)	5.6 A, 1.33 A	4.55 A, 1.16 A	4.05 A, 2.063 A	1.9 A, 1.68 A
SUF	0.1512	0.2241	0.14309	0.353
INDUCTOR VALUE Vg= 12 V; V_O= 84 V;Po= 40 W				
L_1	24.4 uH	15.9 uH	23.7 uH	27.9 uH
L_2	24.4 uH	52.2 uH	165.69 uH	45.38 uH
L_3	170.89 uH	170.89 uH	—	—

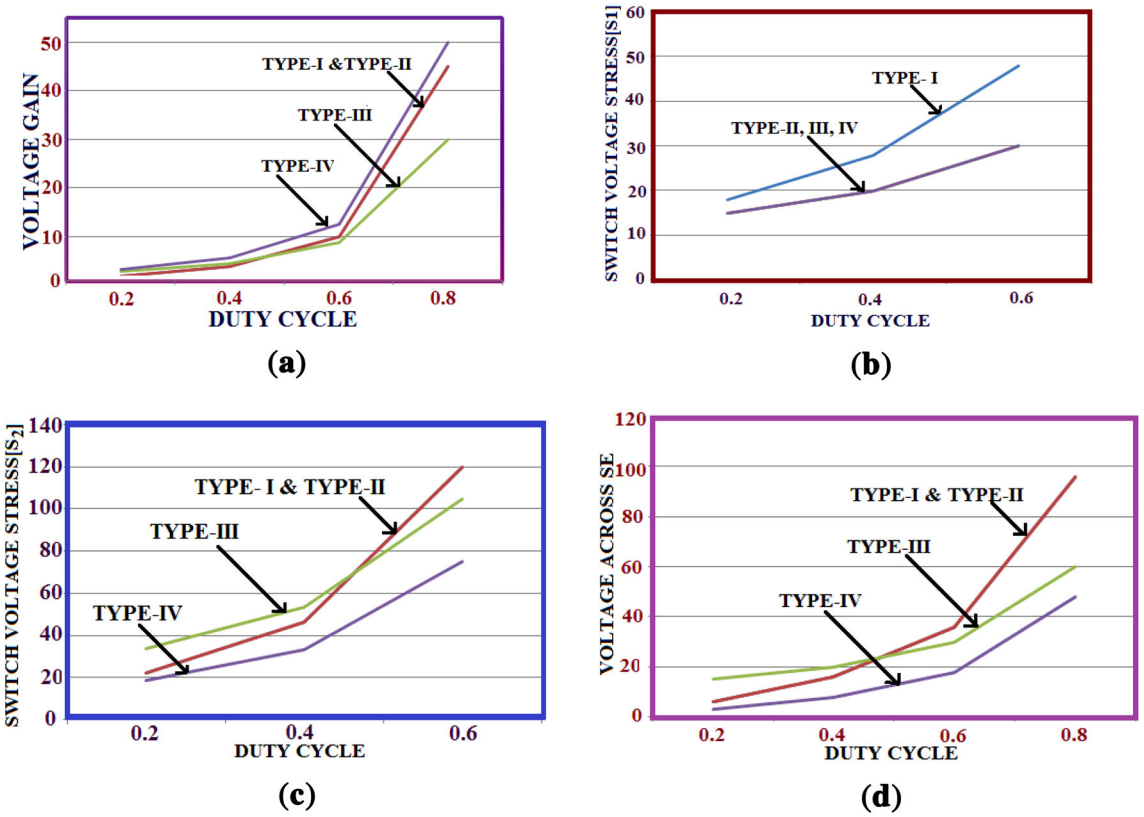


Figure 13. Comparative study; **(a)** Voltage gain Vs duty cycle, **(b)** Switch voltage [S_1] Vs Duty cycle, **(c)** Switch voltage [S_2] Vs Duty cycle and **(d)** SE voltage Vs Duty cycle.

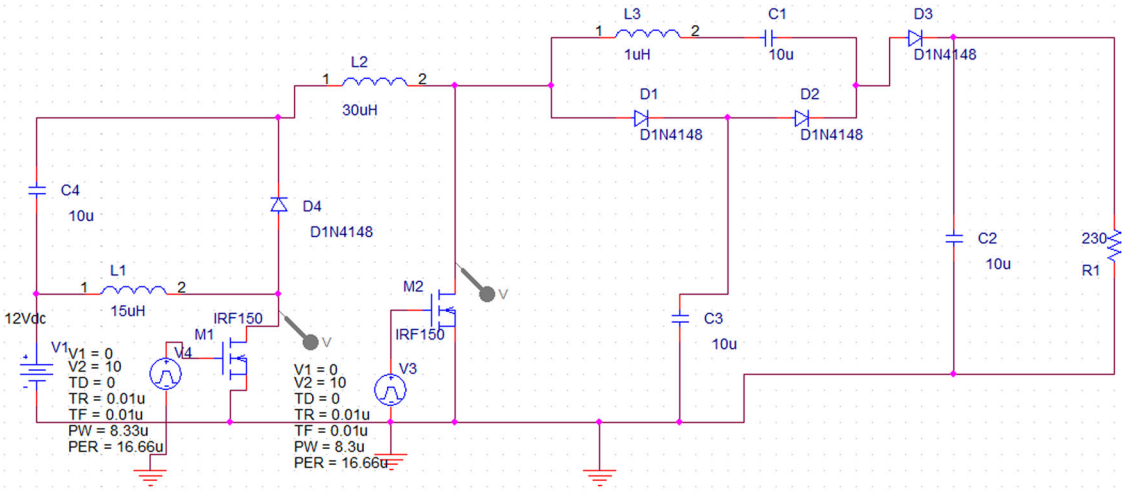
optional and it is used to reduce the commutation loss. It is not taken in to account for component analysis.

- The voltage gain of converter [17] is high compared to the proposed converters. However, the type-IV topology achieves the same voltage gain with two multiplier cell (M = 2) and the device count increases to 15 which is less when compared to the component count in the converter [17].
- Table 3 presents the expression of maximum voltage stresses across the switches and diodes in the type-IV topology and the converters taken for comparison. Figures 12 (a) and (b) give the delineated comparison of stresses across the semiconductor devices of type-IV and other converters. It is found that in the proposed type-IV topology voltage stresses are less compared to the converters in [16–18].
- To complete the analysis, the efficiency comparison is carried out for the converter taken for comparison. It is investigated that the type- IV topology's efficiency is high when compared with the converter in [16]. Components in converter [17, 18] are high when compared to type-IV topology. Hence, the efficiency of those converters will be less compared to type-IV.

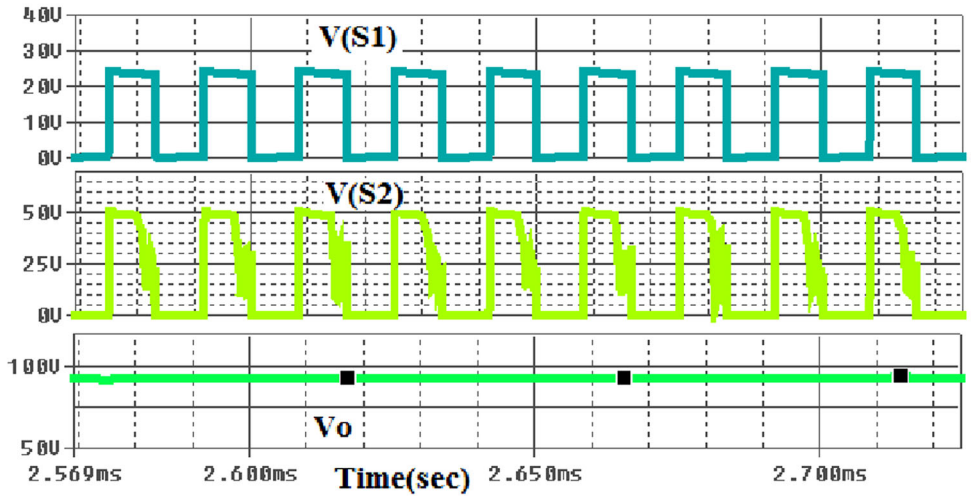
Table 4 gives the comparison of the proposed topologies. A comprehensive assessment is accomplished to determine the best topology from the derived one. Figures 13 (a)-(d) present the graphical comparison created on the derived topologies regarding voltage gain, voltage stress and the voltage across the storage element. From the detailed analysis of the proposed topologies, it is concluded that

Table 5. Factors considered for failure rate calculation.

	Power loss equation	λ_b	Π_A	Π_Q	Π_E/ Ns	Π_T	Π_C	Π_S	Tc (°C)	Θjc (°C/W)	Θja (°C/W)	Environment
MOSFET	Eqn (28)	0.0045	10	2.4	9	9.1	–	–	45	1.5	62	Naval,
Diode	Eqn (39)	0.069	–	2.4	9	50.3	1	0.19	45	1	70	Sheltered



(a)



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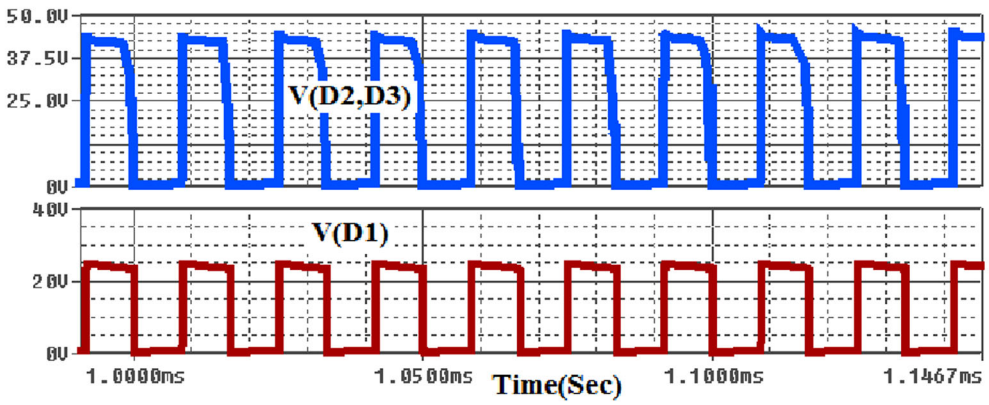
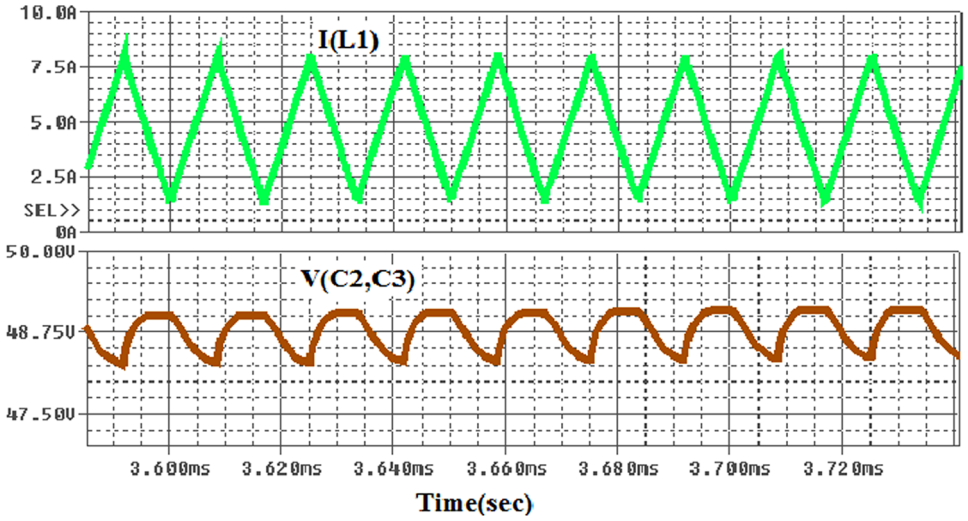
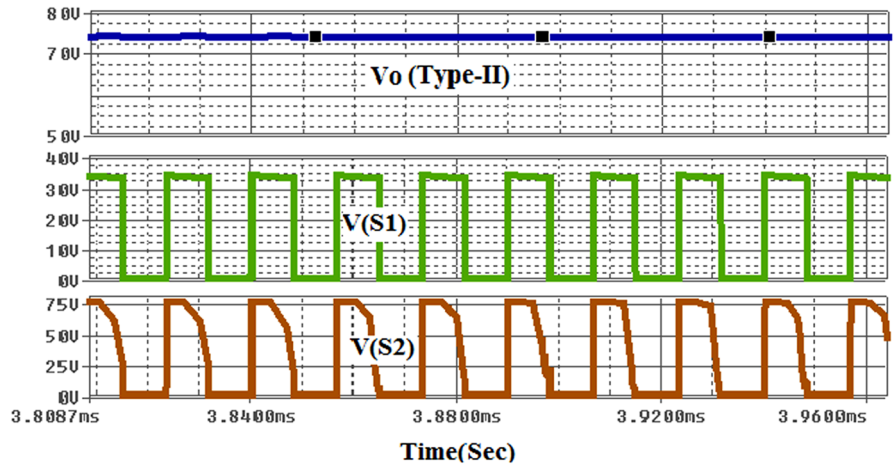


(c)

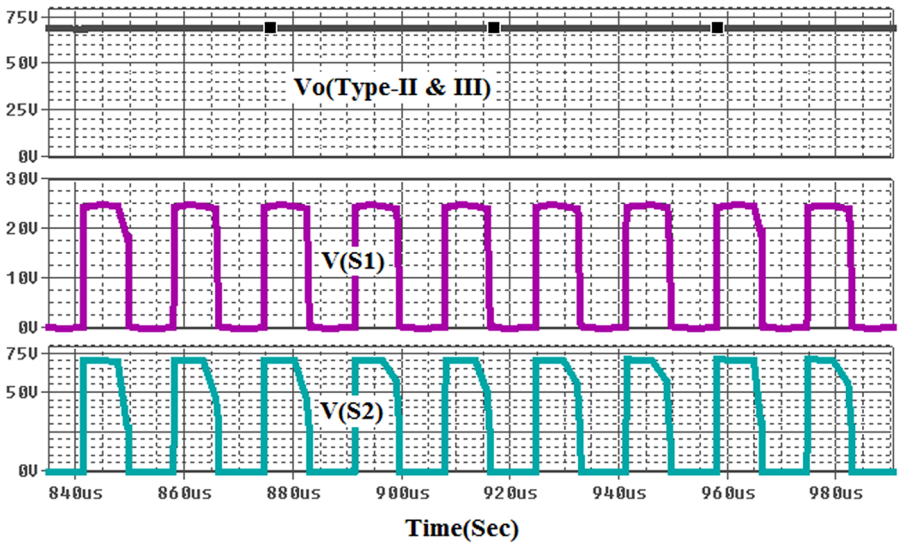
Figure 14. (**a**) Simulated circuit in Pspice, **(b)** Output voltage and switch voltage stress for type-IV topology (D = 0.5), **(c)** Maximum stress voltages across the diodes of type-IV, **(d)** Maximum stress voltages across capacitors and inductor current waveform of type-IV, **(e)** Output voltage and switch voltage stress of type-I topology (D = 0.5) and **(f)** Output voltage and switch voltage stress of type-II & III topology (D = 0.5).



(d)



(e)



(f)

Figure 14. continued

- The voltage gain of type-IV topology is much more compared to other types of the proposed topology, and its gain can be increased by adding the voltage multiplier cell.
- Switch voltage stress (S_1 and S_2) are decidedly less as compared to the other converters. The losses in the switches are reduced, and it will boom the efficiency of the converter.
- The voltage across the storage element (SE) is likewise less as compared to different derived topologies.
- Inductor value is calculated for the identical duty cycle of all of the proposed topologies, and it is examined that the values are substantially much less in comparison.

6. Reliability study of the Type-IV topology

The anticipated lifetime of the device can be easily analyzed by reliability study. The failure rate of power semiconductor devices in any converter depends on the power dissipation across the devices and the working atmosphere, i.e., temperature and environmental stress conditions. In this work, the topology is proposed for shipboard power supply application. So, all the factors are considered as naval, sheltered ecological condition as mentioned in MIL-HDBK-217F handbook [19]. This guide is used to determine the reliability of the electronic components for all the working conditions. Table 5 provides the parameters and equation used for the failure rate calculation of power semiconductor devices used for this application.

The ambient temperature of all the control and instrumentation equipment in the shipboard system is 55°C. The power dissipation across the switches and the diodes are calculated using the equation (28) and (39), respectively. For 40 W power rating with 96 V output voltage, the power losses are determined as Psw = 1.99 W and P_D = 2.17 W. The junction temperature is calculated using the relation

$$Tj = Ta + \Theta ja\, P_{loss} \tag{45}$$

The failure rate model of switch (MOSFET) is

$$\lambda_P = \lambda_b \Pi_A \Pi_T \Pi_Q \Pi_E \tag{46}$$

The failure rate model of diode is

$$\lambda_P = \lambda_b \Pi_A \Pi_T \Pi_S \Pi_C \Pi_Q \Pi_E \tag{47}$$

By substituting the table 5 values in the equation (46) and (47), the failure rates of the switches and diodes are $\lambda_{SWITCHES} = 8.84 \times 10^{-6}$ and $\lambda_{DIODES} = 9.513 \times 10^{-6}$. Failure rates of the diode are found to be high when compared to the switches for type-IV topology.

7. Simulation and experimental results of Type-IV topology

A prototype of type-IV topology is developed with the circuit parameters as P = 40 W, Vg = 12 V, D = 0.46, R_L = 170 Ω. The proposed converter is operated in continuous conduction mode. For simplicity, single voltage multiplier cell is selected. The design of the inductors for all the proposed topologies is given in table 4. According to the derived equations, the values of inductors L_1 = 30 uH, L_2 = 45 uH, capacitor value is 10 uF, and the multiplier capacitor value is 10 uF.

Figure 14 indicates the simulation circuit and results of the proposed type-IV topology obtained by Pspice. The circuit simulated in Pspice is given in figure 14(a). The acquired output voltage is 96 V for D = 0.5 which is given in figure 14(b). According to equation (17) with M = 1, the output voltage calculated matches with the simulated results. Maximum voltage stresses of the semiconductor devices and capacitor are given in figures 14(a)-(d). Figures 14(e) and (f) offer the output voltage and maximum voltage across the switches for type- I, II and III topology.

Figure 15 presents the photograph of the developed hardware. Figures 16 (a)-(c) display the output voltages obtained from the hardware circuit for the same duty cycle, and it closely matches the simulated and theoretical results. Due to the parasitic parameters, the experimental results are quite smaller than the theoretical outcomes. Type-IV topology can be realized as single switch converter by modifying the topology with an additional diode. For the prototype, IRF840 MOSFET is employed with the R_{DS} = 0.85 Ω and diodes IN4003 are used. PIC microcontroller PIC168F77A is used to provide pulses to the MOSFET. Isolation between the power and gate drive circuit is provided by TLP250.

Figures 16 (d)-(f) are component stress voltages obtained from the hardware circuit. The overall performance intently

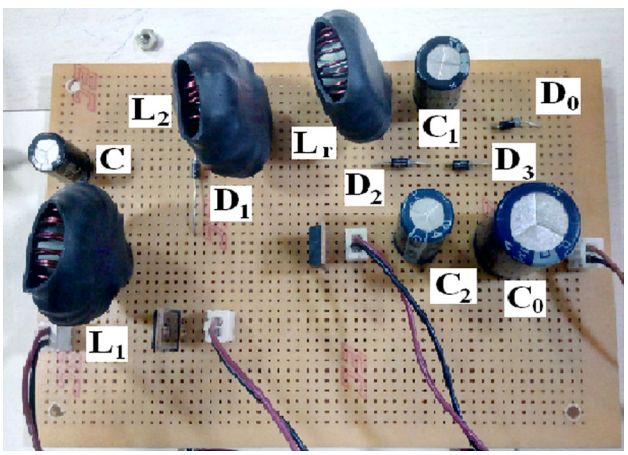


Figure 15. Photograph of the hardware.

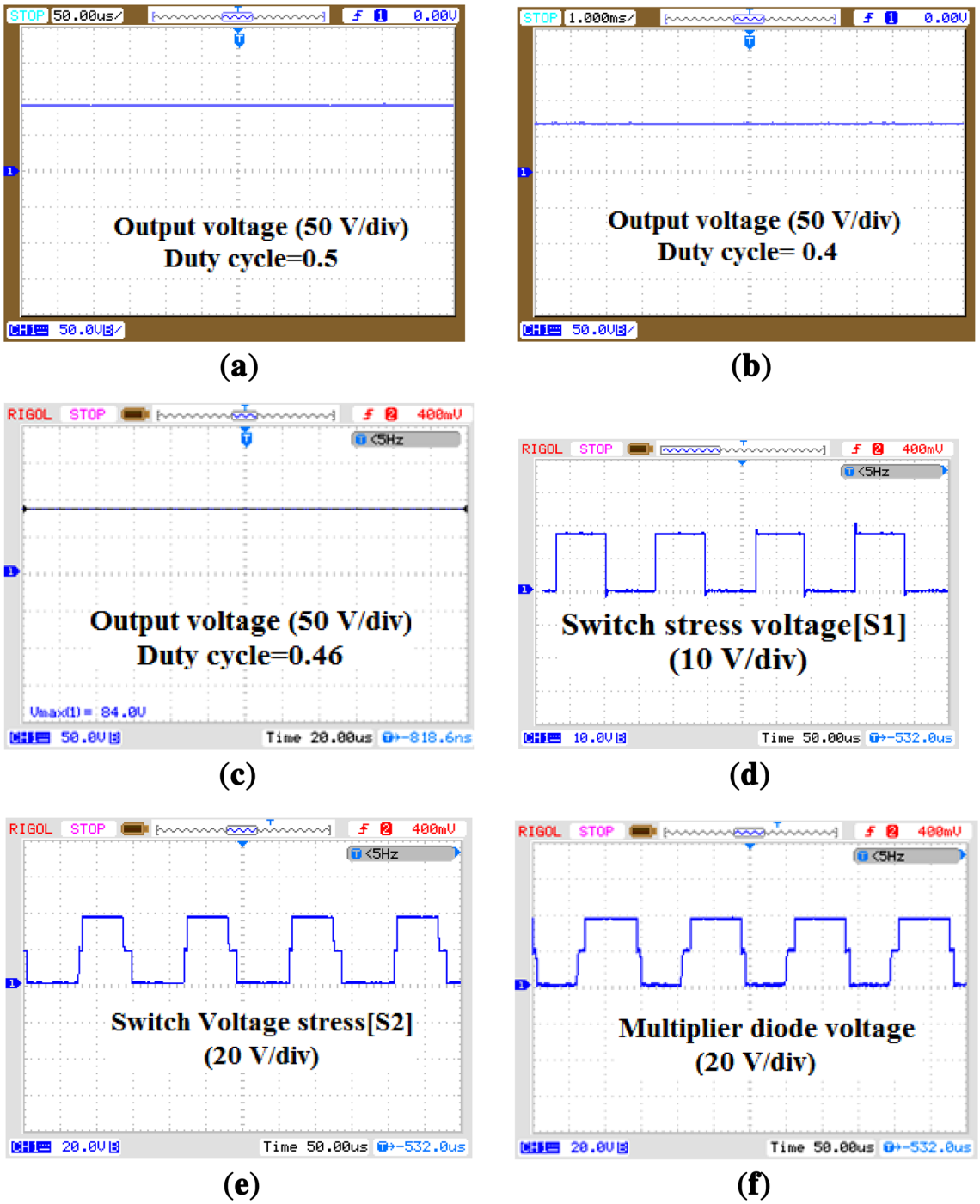


Figure 16. Experimental results **(a)** Output voltage for D = 0.5, **(b)** Output voltage for D = 0.4, **(c)** Output voltage for D = 0.46, **(d)** Maximum switch voltage [S_1] for D = 0.46 and **(e)** Maximum switch voltage [S_2] for D = 0.46 (f) Multiplier diode voltage for D = 0.46.

matches with the theoretical analysis of the type-IV topology as given in table 2. Figures 16 (d) and (e) provide the maximum voltage stress across the switches, and it is equal to 20 V for switch S_1 and 40 V for switch S_2. Figure 16 (f) affords the voltage across the multiplier diode, and it is equal to the switch S_2 voltage which is proved by this result.

8. Conclusion

A family of high step-up quadratic boost converter is proposed in this paper. All the topologies are derived by I-IIA structure with RRPP technique. Type-IV topology is the most compelling candidate within the derived one. Voltage conversion ratio is increased by increasing the VM cell.

Subsequently, a model is made for the type-IV topology owing to its high gain. The ratings of the circuit elements such as the inductor and capacitor are lesser compared to other topologies. The diode and switch voltage stress are substantially low. Hence, the rating of semiconductor devices is reduced, and as a result of this, the converter cost reduces. The experimental results prove that the type-IV topology has higher voltage gain with reduced voltage stress across the semiconductor devices. The structure of the type-IV converter is simple, since the converter is non-isolated and it uses less inductance value. Thus the type-IV topology can be used fruitfully in several high voltage applications.

Nomenclature

Vg	Input voltage
V_O	Output voltage
D	Duty cycle
G_V	Voltage gain
M	Number of multiplier cell
f_S	Switching frequency
I_O	Output current
I_L	Inductor current
R_L	Output resistance
I_{Drms}	RMS diode current
I_{Davg}	Average diode current
I_{Srms}	Switch RMS current
I_{Crms}	Capacitor RMS current
Psw	Switch loss
P_D	Diode loss
P_L	Inductor loss
P_C	Capacitor loss
λ_P	Part failure rate
λ_b	Base failure rate relating the influence of electrical and temperature stresses
Π_E	Environmental factors that affect the part reliability
Tj	Junction temperature (°C)
Tc	Case temperature (°C)
Ta	Ambient temperature (°C)
Θjc	Junction to case thermal resistance (°C/W)
Θ_{CA}	Case to ambient thermal resistance (°C/W)
Θ_{jA}	Junction to ambient thermal resistance (°C/W)
Π_A	Application factor
Π_Q	Quality factor
Π_S	Electrical stress factor
Π_C	Contact construction factor

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