



A novel single switch dc-dc converter with high voltage gain capability for solar PV based power generation systems

Nilanjan Tewari, V.T. Sreedevi*

School of Electrical Engineering, VIT Chennai, Tamil Nadu, Chennai 600127, India

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ABSTRACT

This paper presents a single switch non-isolated DC-DC converter with high voltage gain capability for solar photovoltaic (PV) applications. The proposed converter is synthesized from passive switched inductor (SI) and switched capacitor (SC) topologies and integrated with an additional voltage boost capacitor to enhance the voltage gain. Due to the converter structure and adopted gain extension technique, the voltage stress on the switch and three diodes is 50% of the output voltage, while the remaining diodes experience a voltage stress of only 25% of the output voltage. Experimental results obtained from a 34 V/380 V, 200 W prototype converter validate the proposed concept, adopted design procedure and illustrates the fact that the proposed converter operates at a full load efficiency of 93%. Further, the proposed converter provides better component utilization compared to some existing converters.

1. Introduction

In recent years, distributed power generation using renewable energy sources has received greater attention due to the rapid exhaustion of fossil fuels and increased emission of greenhouse gases (Jacobson and Delucchi, 2011). Solar energy is one of the promising and clean renewable energy resources for electric power generation (Bennett et al., 2012). However, the output from solar panel is low and many panels have to be connected in series-parallel combination (Singh and Banerjee, 2015). The voltage available from the different series-parallel combination of solar PV cell is of the order of 20–60 V (Rajesh and Carolin Mabel, 2015). Hence, a suitable power converter is required to interface the PV panels with the load (Shuhui et al., 2011). In many applications like solar based generation system, comparatively high voltage is achieved by dc-dc boost derived converter (Forouzes et al., 2017; Li and He, 2011) as shown in Fig. 1.

Isolated dc-dc converters are not preferable solution for high voltage gain applications like, solar based power generation system due the problems like saturation in high frequency transformer core, low efficiency, bulk in size etc (Gonzalez et al., 2007; Fathabadi, 2016; Kima et al., 2010). However, conventional non-isolated dc-dc boost converter suffers from the problem of high voltage stresses on switch and reverse recovery problem of diodes during high duty ratio operations in order to achieve high voltage gain. The problems of isolated converter

topologies can easily be overcome in non-isolated topologies (Meneses et al., 2013; Sivakumar et al., 2016; Li and He, 2011). Many non-isolated high gain dc-dc converter topologies which use different combinations of voltage lifting techniques for PV application are discussed (Revathi and Prabhakar, 2016; Taghvaei et al., 2013). One of the simple methods to achieve high voltage gain is cascaded technology. But cascaded boost converter suffers from the problems of high voltage stress on second stage switch and diode, reverse recovery issue and instability (Vighetti et al., 2012).

Quadratic boost converters and their derivatives also provide higher voltage gain at the expense of extreme duty ratios ($D > 0.8$), diode reverse recovery problems and associated higher power losses (Divya Navamani et al., 2017; Zhang et al., 2015).

The concept using multilevel is introduced to achieve high voltage gain (Zhang et al., 2013). No of levels in multilevel boost converter is limited due to high switching loss, poor voltage regulation, high voltage and high current stress on switch. Voltage multiplier cell technology offers high voltage gain (Al-Saffar and Ismail, 2015; Nouri et al., 2013). Unfortunately, the power handling capability reduces when voltage gain is more than 10 (Tseng et al., 2013; Tseng and Huang, 2014).

Coupled inductor based topologies also offer high voltage gain (Chen et al., 2012; He and Liao, 2015). However, leakage inductance causes serious problems like resonance and EMI in the power circuit. At times, voltage lifting techniques like, voltage multiplier cells, switched

Abbreviations: PV, photovoltaic; SI, switched inductor; SC, switched capacitor; MPPT, maximum power point tracking; CCM, continuous conduction mode; DCM, discontinuous conduction mode

* Corresponding author.

E-mail address: sreedevi.vt@vit.ac.in (V.T. Sreedevi).

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Nomenclature

Symbols used

| | |
|------------------|----------------------------------|
| S | switch |
| L_1, L_2 | switched inductors |
| C_1, C_2 | switched capacitors |
| C_B | boost capacitor |
| C_0 | output capacitor |
| D_1, D_2 | passive switched inductor diodes |
| D_{C1}, D_{C2} | switched capacitor diodes |
| D_0 | output diode |
| R_0 | load resistance |
| V_{in}, V_0 | input voltage and output voltage |
| V_{L1}, V_{L2} | voltage across L_1 and L_2 |

| | |
|--|--|
| $V_{C1}, V_{C2}, V_{CB}, V_{C0}$ | voltage across C_1, C_2, C_{CB} and C_0 |
| $V_{D1}, V_{D2}, V_{DC1}, V_{DC2}, V_{D0}$ | voltage across D_1, D_2, D_{C1}, D_{C2} and D_0 |
| V_S | voltage across switch S |
| I_{L1}, I_{L2} | current through L_1, L_2 |
| I_{CB}, I_{C1}, I_{C2} | current through C_B, C_1, C_2 |
| D | duty cycle of the switch S |
| T_{ON} | ON time period of switch S |
| G_{CCM}, G_{DCM} | voltage gain during CCM and DCM |
| T_S | switching time period |
| f_s | switching frequency |
| τ, τ' | normalized inductor time constant and boundary normalized inductor time constant |
| ΔI_L | ripple current of inductor |
| $\Delta V_{C1}, \Delta V_{C2}, \Delta V_{CB}, \Delta V_{C0}$ | ripple voltage of C_1, C_2, C_B and C_0 |

capacitor cells etc. are also integrated with coupled inductor based topologies to achieve high voltage gain (Ye et al., 2017).

Switched capacitor based boost converters can provide high voltage gain at reduced voltage stress on switch by charging the capacitors in parallel and discharging in series. But the voltage regulation of these types of converter is poor (Axelrod et al., 2008; Wu et al., 2015). Zeta derived converters integrated with SC cells also provide high voltage gain (Ismail et al., 2008). But the discontinuous input current makes it inappropriate for solar PV applications. Switched inductor based boost converters are simple and enhance the voltage gain with high component count by charging the inductors in parallel and discharging in series (Axelrod et al., 2008; Yang and Liang, 2009). In passive switched inductor based converters, the entire switched inductor cell is connected in series with the single active switch (Axelrod et al., 2008) while in active switched inductor network, each inductor is connected with an individual active switch to reduce the voltage stress on active switches at the cost of high component count (Yang and Liang, 2009). Combined active and passive SI cells can also deliver high gain but at the expense of large no of active switches as well as large no of total component counts leading to high switching and conduction losses (Maheri et al., 2017).

This paper presents a novel single switch non-isolated dc-dc converter with high voltage gain capability. The proposed converter is a combination of switched inductor and switched capacitor technology integrated with an additional boost capacitor. Combination of passive switched inductor and switched capacitor cells provides high voltage gain. Incorporation of an additional boost capacitor instead of diode in the discharging path of switched inductor cell ensures additional voltage gain with reduced voltage stress on switch and diodes. Low voltage

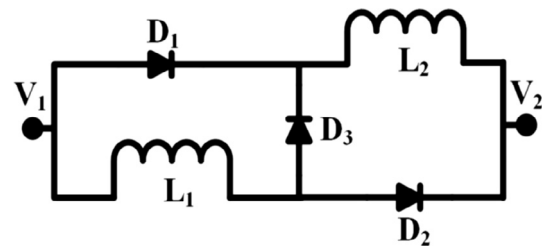


Fig. 2. Passive switched inductor cell.

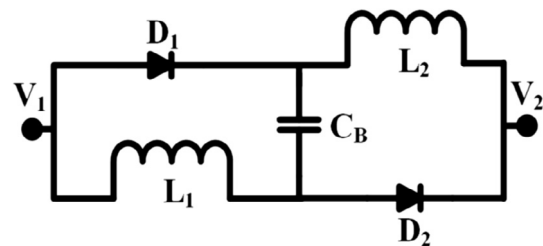


Fig. 3. Proposed modified switched inductor cell.

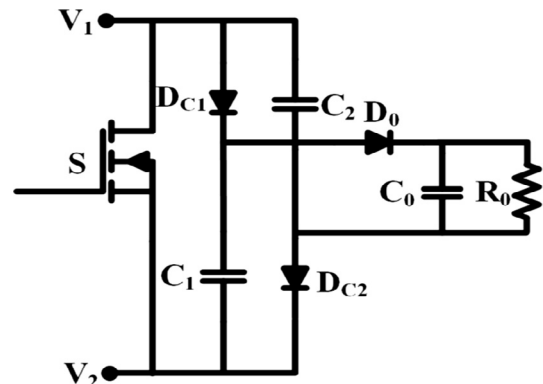


Fig. 4. Switched capacitor cell.

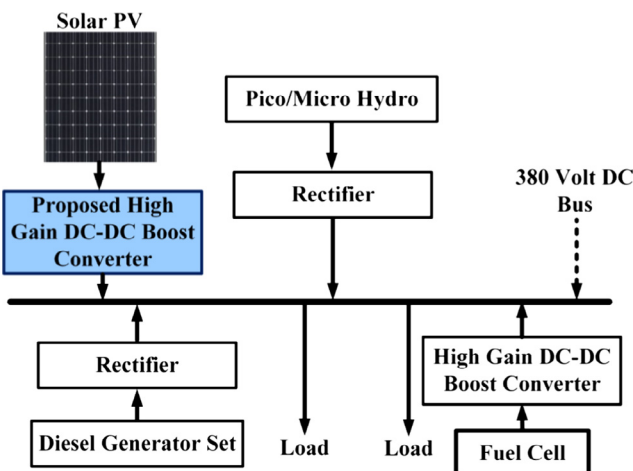


Fig. 1. Block diagram of solar PV integrated standalone DC Micro grid.

stress on diodes helps to eliminate the problem of reverse recovery in the proposed converter. It also supports for further reduction of conduction and switching losses of the diodes leading to improved efficiency of the converter. As the proposed converter is a hybrid combination of SI and SC technology, it overcomes the problem of poor voltage regulation of conventional SC based converter. The paper also includes an extensive comparative study with similar types of high gain converters which ensures the high voltage gain and better component utilization capability of the proposed converter than the other

converters mentioned. Implementation of control algorithm, like MPPT, is comparatively easy due to the presence of single switch in the proposed converter. Single switch with low voltage stress on it makes it suitable for solar PV applications.

The paper is organized as follows. Section 1 introduces the proposed research work. The topological derivation and structure of the proposed converter is discussed in Section 2. Operating principle of the proposed converter is discussed during continuous conduction mode (CCM) and discontinuous conduction mode (DCM) in Section 3. Steady state analysis is derived in Section 4. Section 5 includes the simulation and experimental results. Comparison with other similar types of high gain converters is presented in Section 6. Conclusions of the work are provided in Section 7.

2. Proposed converter

2.1. Topological derivation of the proposed converter

Fig. 2 represents the passive switched inductor cell (Axelrod et al., 2008). In this topology, diode D_1 & D_2 become forward biased when the voltage V_1 is higher than the V_2 . During this period inductor L_1 & L_2 charge in parallel. Diode D_3 is forward biased and L_1, L_2 discharge in series when V_1 is less than V_2 . Diode D_1 & D_2 is reversed biased during this interval. This type of cell provides a voltage gain of $(1 + D)/(1 - D)$.

Switched capacitor cell is presented in Fig. 4 (Wu et al., 2015). Capacitor C_1 & C_2 discharge in series to the load through switch S and output diode D_0 , when the switch S is ON. During the OFF period of switch S , diode D_{C1} & D_{C2} become forward biased and capacitors C_1 & C_2 charge in parallel.

In the proposed modified switched inductor cell shown in Fig. 3, diode D_3 is replaced by a boost capacitor C_B which ensures an increased voltage gain of $2/(1 - D)$. When V_1 is greater than V_2 , diode D_1 & D_2 are forward biased and L_1, L_2 & C_B charge in parallel. When V_1 is less than V_2 , then D_1 & D_2 are reversed biased and L_1, C_B & L_2 discharge in series. As one power diode D_3 is replaced by capacitor in the proposed cell, the total power loss in semiconductor devices is reduced. This modified switched inductor cell is connected with the SC cell to enhance the voltage gain further.

2.2. Power circuit diagram of the proposed converter

Fig. 5 shows the circuit diagram of the proposed converter. The circuit consist of one active switch (S), two switched inductors (L_1, L_2) with equal values, one boost capacitor (C_B), two switched capacitors (C_1, C_2) of same values, one output capacitor (C_0), two passive switched inductor diodes (D_1, D_2), two switched capacitor diodes (D_{C1}, D_{C2}) and one output diode (D_0).

3. Operating principle

The operating principle of the proposed converter is discussed

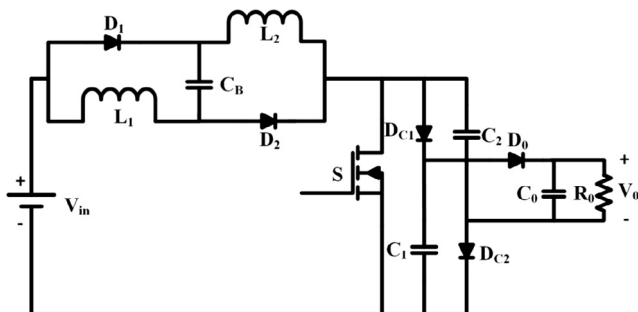


Fig. 5. Circuit diagram of proposed converter.

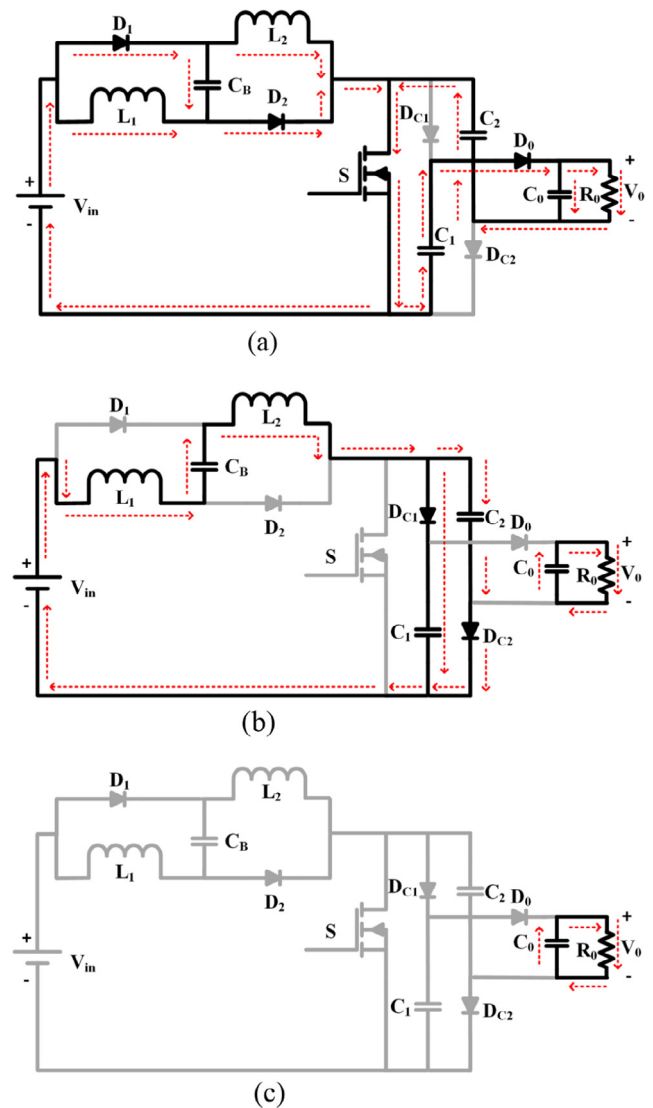


Fig. 6. (a)–(c) Equivalent circuits during CCM and DCM.

during continuous conduction mode (CCM) as well as during discontinuous conduction mode (DCM). The following assumptions are made for easier understanding of the power circuit operation.

- (i) All semiconductor devices and passive elements are ideal.
- (ii) Values of switched inductors (L_1 & L_2) and the values of switched capacitors are (C_1 & C_2) are same.

3.1. Continuous conduction mode (CCM)

The operation in CCM can be explained by two modes of operation. Fig. 6(a) and (b) represent the equivalent circuits during CCM of operation. Fig. 7 shows the characteristics waveforms during CCM.

3.1.1. Mode 1: When both the switches are turned ON

Switch S is turned ON during this mode of operation. Fig. 6(a) represents the equivalent circuit during this mode. Inductors L_1, L_2 and boost capacitor C_B charge in parallel. Energy stored across C_1 & C_2 gets transferred to C_0 . During the energy transfer process, capacitors C_1 & C_2 discharge in series and forward bias diode D_0 . The voltage across inductor and boost capacitor is,

$$V_{in} = V_{L1} = V_{L2} = V_{CB} \tag{1}$$

Similarly the voltage across the output capacitor is given by,

$$V_{C0} = V_0 = V_{C1} + V_{C2} \tag{2}$$

As C_1 and C_2 are with same values then (2) can be written as

$$V_{C1} = V_{C2} = \frac{V_0}{2} \tag{3}$$

3.1.2. Mode 2: When both the switches are turned OFF

Switch S is turned OFF during this mode of operation. Inductors L_1 , L_2 and C_B are connected in series and discharge together to charge C_1 and C_2 . C_1 and C_2 are connected in parallel during this mode. Diode D_1 , D_2 and D_0 are reversed biased. The voltage across inductor L_1 and L_2 is

$$V_{L1} = V_{L2} = \frac{V_{in} + V_{CB} - V_{C1}}{2} \tag{4}$$

Applying volt-second balance principle on L_1 and L_2 , the voltage gain (G_{CCM}) can be obtained as

$$\int_0^{DT_s} V_{in} dt + \int_{DT_s}^{T_s} (V_{in} - \frac{V_0}{4}) dt = 0 \tag{5}$$

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{4}{(1-D)} \tag{6}$$

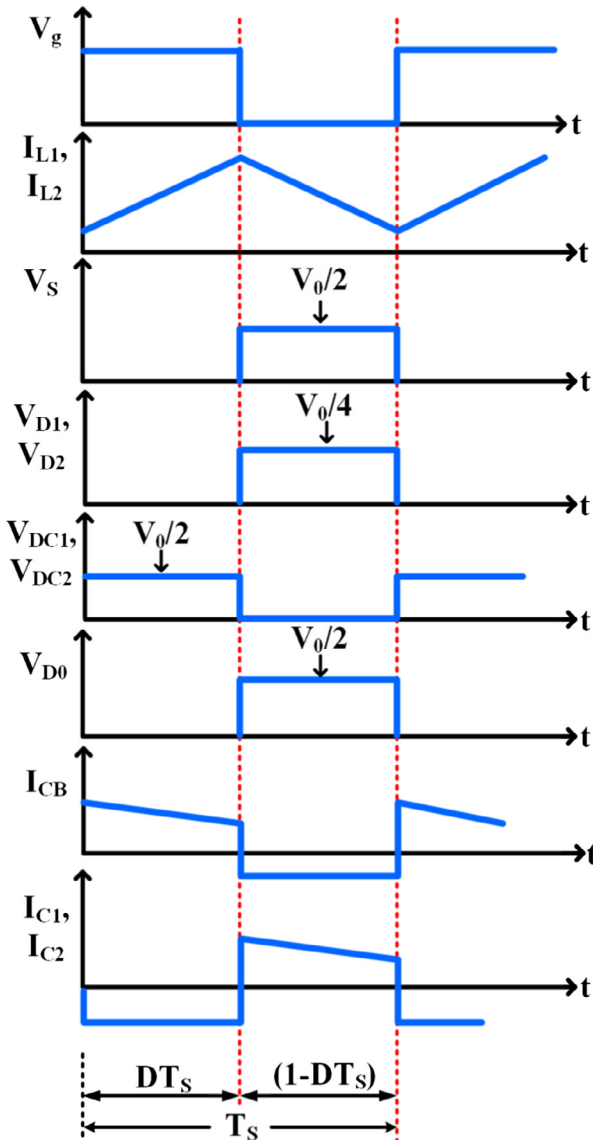


Fig. 7. Characteristics waveform in CCM.

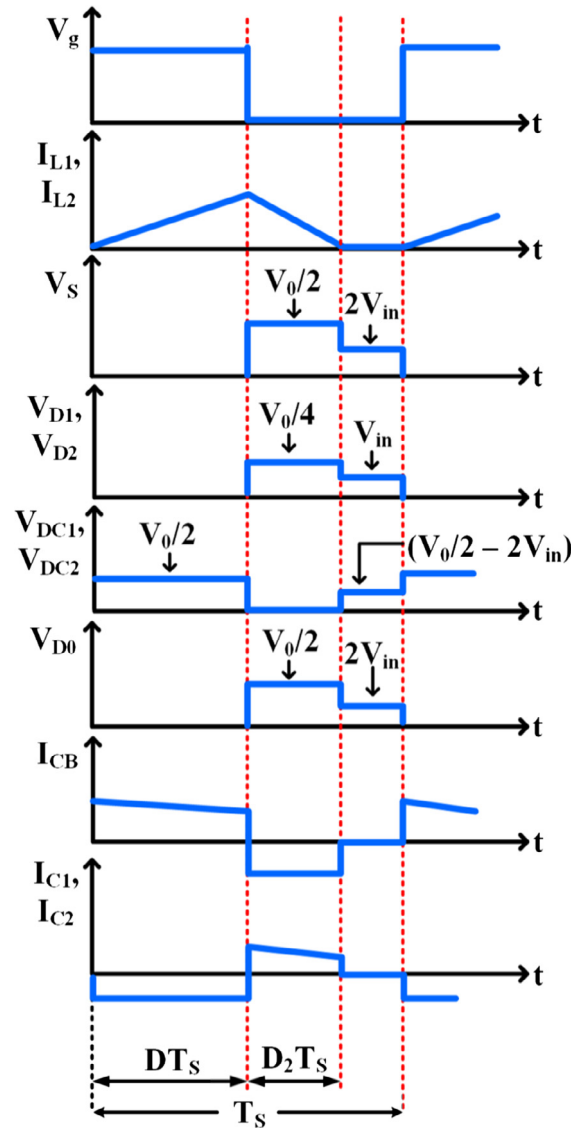


Fig. 8. Characteristics waveform in DCM.

3.2. Discontinuous conduction mode (DCM)

The operation of the proposed converter can be explained during DCM by three modes of operation. Fig. 6(a)–(c) represent the equivalent circuits during DCM operation. The characteristics waveforms during DCM are shown in Fig. 8.

3.2.1. Mode 1: When both the switches are turned ON

This mode of operation is similar to Mode 1 operation of CCM. Equivalent circuit during this time interval is presented in Fig. 6(a). During this interval, the peak inductor currents can be written as,

$$I_{L1peak} = I_{L2peak} = \frac{V_{in}DT_s}{L} \tag{7}$$

3.2.2. Mode 2: When both the switches are turned OFF

This mode is also similar to Mode 2 operation of CCM. But the inductor currents decreased to zero at the end of this interval. Fig. 6(b) represents the equivalent circuit of this interval. During this interval, the peak values of inductor currents can be represented as,

$$I_{L1peak} = I_{L2peak} = \frac{(\frac{V_0}{4} - V_{in})D_2T_s}{L} \tag{8}$$

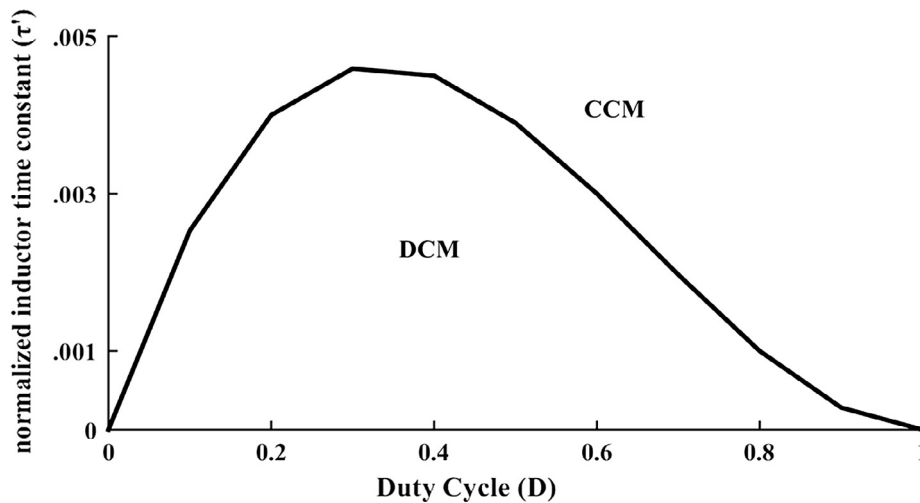


Fig. 9. Boundary condition of the converter.

3.2.3. Mode 3: When both the switches are turned OFF and inductors are fully discharged

During this mode of operation, only the output capacitor C_0 discharges to the load R_0 . The equivalent circuit during this mode is shown in Fig. 6(c). During this mode the voltage across the output capacitor is

$$V_{C_0} = -V_0 \tag{9}$$

From (7) and (8), D_2 can be represented as,

$$D_2 = \frac{4V_{in}D}{(V_0 - 4V_{in})} \tag{10}$$

Combining (7), (8) and (9), voltage gain in DCM is derived as,

$$G_{DCM} = \frac{V_0}{V_{in}} = \sqrt{\frac{D}{2\tau}} \tag{11}$$

The normalized inductor time constant ‘ τ ’ is defined as,

$$\tau = \frac{Lf_s}{R_0} \tag{12}$$

3.3. Boundary condition between CCM and DCM

When the converter operates at the boundary between CCM and DCM, the voltage gain of the converter under both modes is same. Hence, the boundary normalized inductor time constant can be found out by combining (6) and (10). The variation of normalized inductor time constant (τ') with the duty cycle (D) is represented in Fig. 9. The boundary normalized inductor time constant is represented as,

Table 1
Specification of the proposed converter during CCM.

| Parameters | Specifications |
|---|---------------------------|
| Maximum output power, P_0 | 200 W |
| Input voltage, V_{in} | 34 V |
| Output voltage, V_{out} | 384 V |
| Switching frequency, f_s | 50 kHz |
| Duty cycle, D | 0.65 |
| Inductors, L1, L2 | 180 μ H, 8 A |
| Boost capacitor and switched capacitors C_B, C_1, C_2 | 10 μ F, 150 V |
| Output capacitor, C_0 | 4.7 μ F, 450 V |
| Switch ‘S’ | IRFP4332PBF (300 V, 57 A) |
| Diodes D_1, D_2 | MUR1515G (150 V, 15 A) |
| Diodes D_{C1}, D_{C2}, D_0 | MUR1560G (400 V, 15 A) |

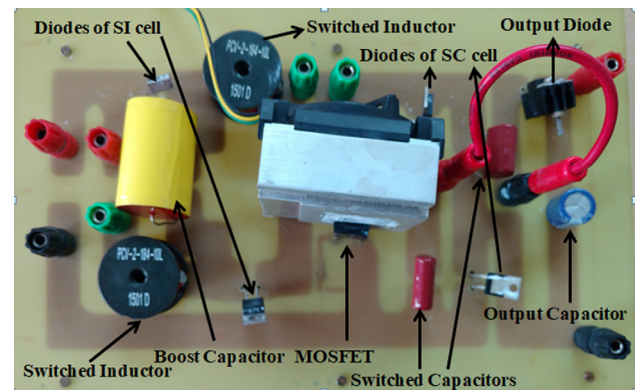


Fig. 10. Hardware prototype of proposed converter.

$$\tau' = \frac{D(1-D)^2}{32} \tag{13}$$

4. Steady state analysis and design details

4.1. Design of magnetic elements

In case of switched inductor based converter, voltage stress on diodes and switches is high with different values of inductors. So, in the proposed converter both the inductor L_1 and L_2 are chosen with equal values. The value of both the inductors can be evaluated by considering the ripple current of inductors (ΔI_L) and switching frequency (f_s) as,

$$L_1 = L_2 = \frac{DV_{in}}{\Delta I_L f_s} \tag{14}$$

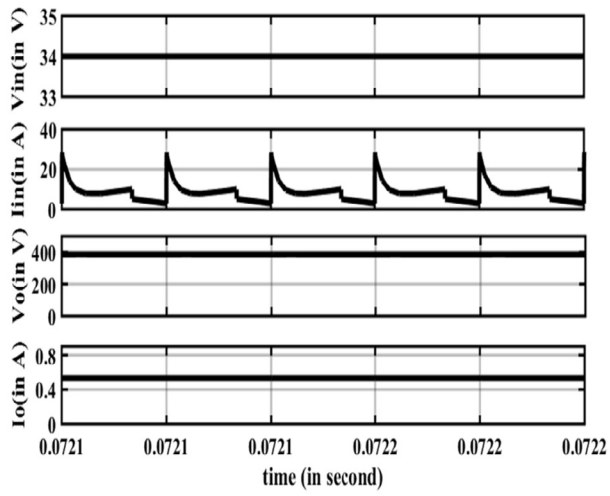
4.2. Capacitors design

Similarly, the design of capacitors depends on the ripple in capacitor voltage (ΔV_C) and switching frequency (f_s). The output capacitor can be designed by the equation given as,

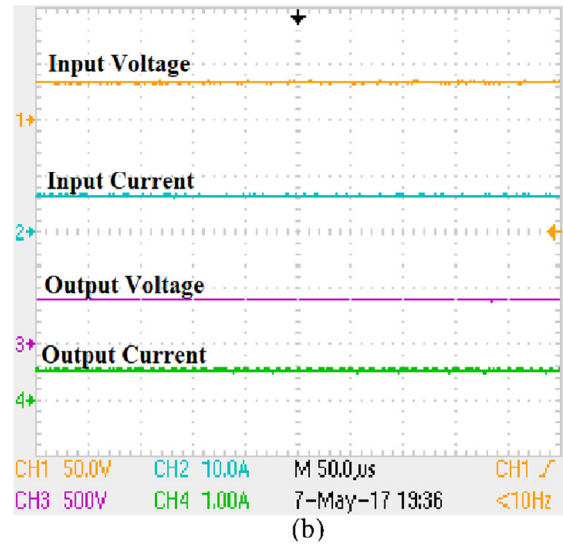
$$C_0 = \frac{V_0(1-D)}{R_0 f_s \Delta V_{C_0}} \tag{15}$$

The values of switched capacitors can be found out as,

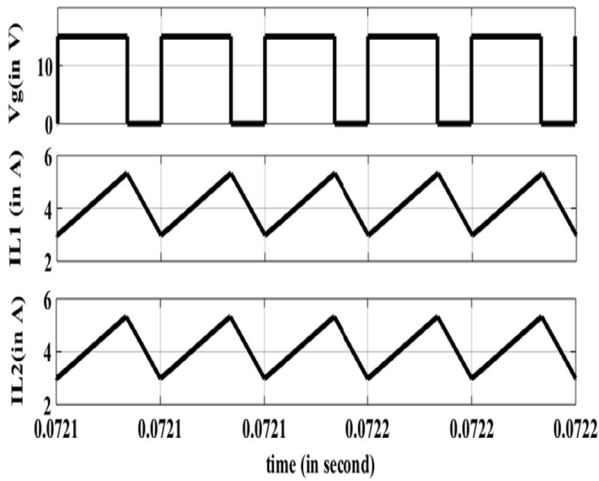
$$C_1 = C_2 = \frac{I_{in}(1-D)}{2f_s \Delta V_{C_1}} \tag{16}$$



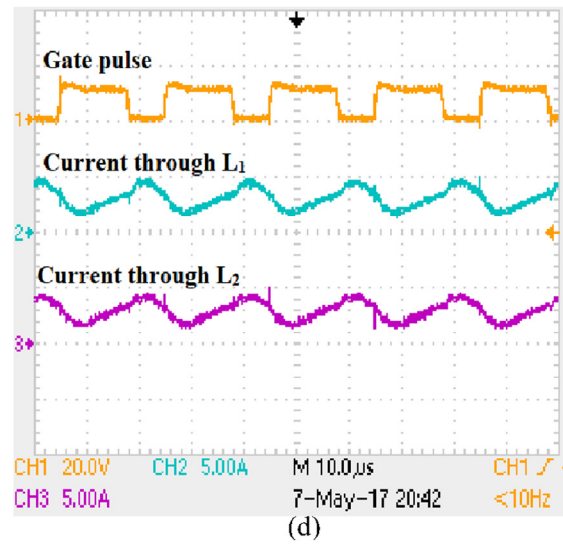
(a)



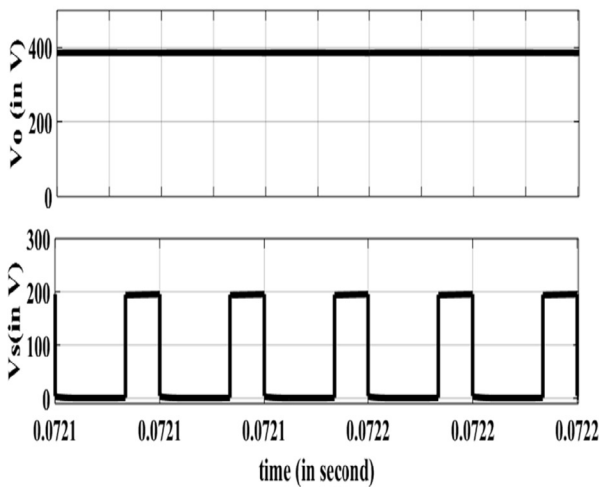
(b)



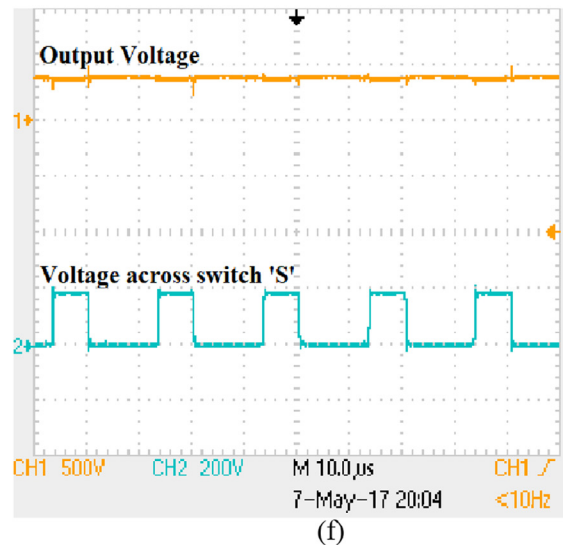
(c)



(d)



(e)



(f)

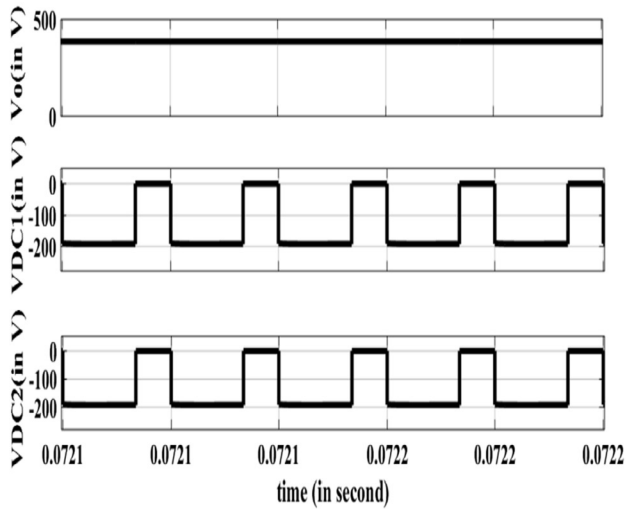
Fig. 11. Simulation and experimental waveforms of the proposed converter.

where $\Delta V_{C1} = \Delta V_{C2}$. Considering a lossless converter, in (16) I_{in} is replaced by,

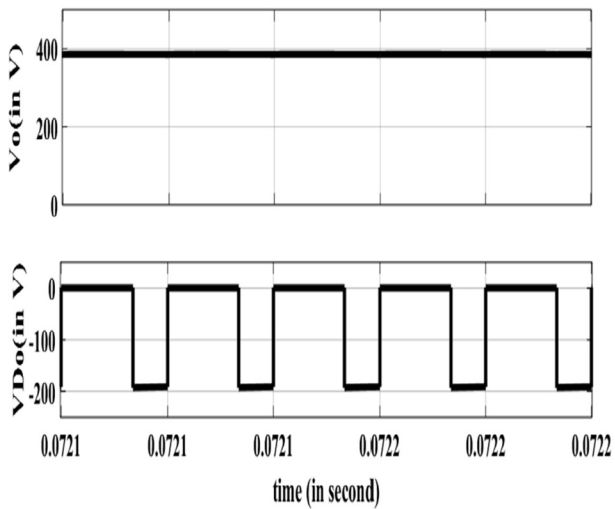
$$I_{in} = \frac{4V_o}{(1-D)R_o}$$

(17)

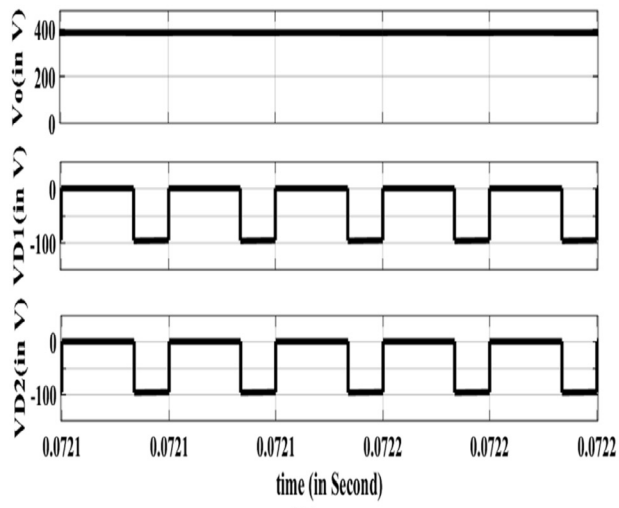
Replacing the value of I_{in} from (16) by (17), it becomes,



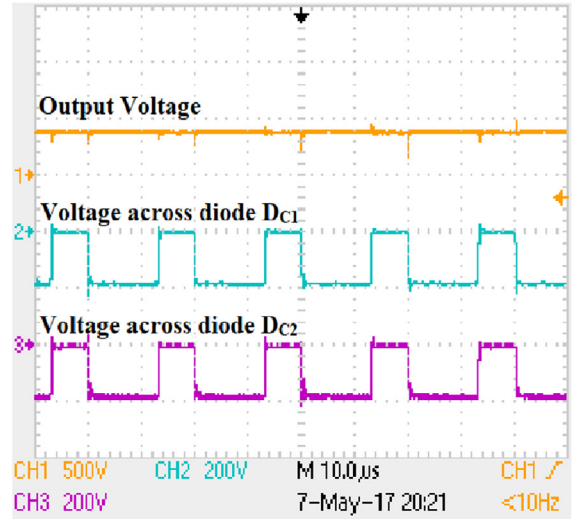
(g)



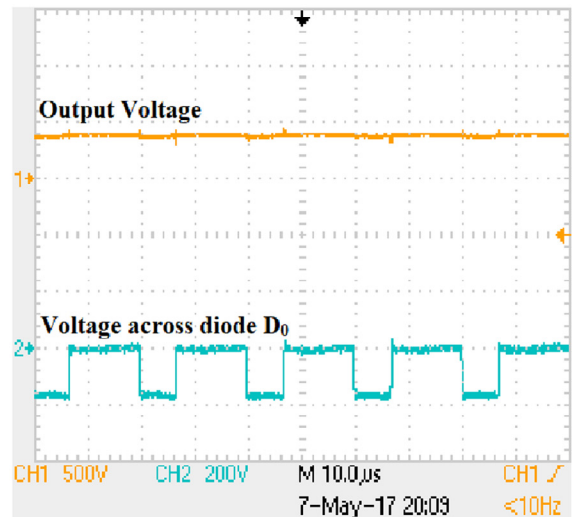
(i)



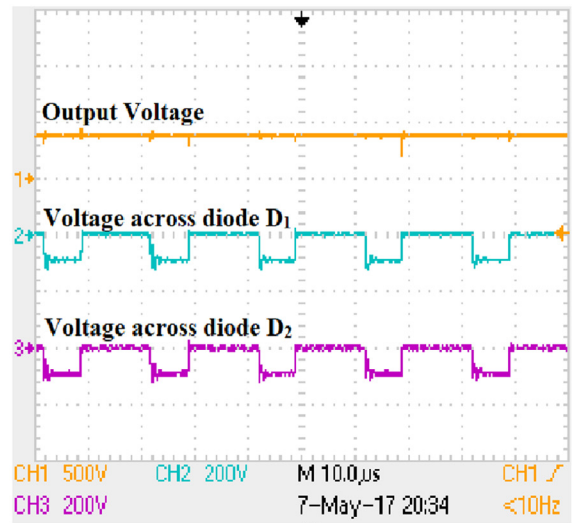
(k)



(h)



(j)



(l)

Fig. 11. (continued)

$$C_1 = C_2 = \frac{2V_0}{R_{of5}\Delta V_{C1}}$$

(18)

$$C_B = \frac{4V_0}{R_{of5}\Delta V_{CB}}$$

(19)

Similarly the value of C_B is selected by the equation,

4.3. Voltage stress on diodes and switch

The voltage stress on diodes D_1 and D_2 during CCM operation can be expressed as,

$$V_{D1} = V_{D2} = \frac{V_0}{4}, T_{ON} \leq t \leq T_S \tag{20}$$

Similarly the voltage stresses on D_{C1} , D_{C2} and D_0 during CCM are given in (21) and (22) respectively,

$$V_{DC1} = V_{DC2} = \frac{V_0}{2}, 0 \leq t \leq T_{ON} \tag{21}$$

$$V_{D0} = \frac{V_0}{2}, T_{ON} \leq t \leq T_S \tag{22}$$

Voltage stresses on D_1 , D_2 , D_{C1} , D_{C2} , D_0 during DCM is expressed as,

$$V_{D1} = V_{D2} = \begin{cases} \frac{V_0}{4}, & T_{ON} \leq t \leq D_2 T_S \\ V_{in}, & D_2 T_S \leq t \leq T_S \end{cases} \tag{23}$$

$$V_{DC1} = \begin{cases} \frac{V_0}{2}, & 0 \leq t \leq T_{ON} \\ \frac{V_0}{2} - 2V_{in}, & D_2 T_S \leq t \leq T_S \end{cases} \tag{24}$$

Similarly,

$$V_{DC2} = \begin{cases} \frac{V_0}{2}, & 0 \leq t \leq T_{ON} \\ \frac{V_0}{2} - 2V_{in}, & D_2 T_S \leq t \leq T_S \end{cases} \tag{25}$$

$$V_{D0} = \begin{cases} \frac{V_0}{2}, & T_{ON} \leq t \leq D_2 T_S \\ 2V_{in}, & D_2 T_S \leq t \leq T_S \end{cases} \tag{26}$$

The voltage stress on switch ‘S’ during CCM and DCM is given by (27) and (28) respectively,

$$V_S = \frac{V_0}{2}, T_{ON} \leq t \leq T_S \tag{27}$$

$$V_S = \begin{cases} \frac{V_0}{2}, & T_{ON} \leq t \leq D_2 T_S \\ 2V_{in}, & D_2 T_S \leq t \leq T_S \end{cases} \tag{28}$$

5. Test results for proposed converter: Simulation and experimentation

The performance of the proposed converter has been verified by simulation in MATLAB/SIMULINK and through testing of a hardware prototype. The specification of the proposed converter used in simulation and hardware is given in Table 1. As the proposed converter is developed for solar PV based dc micro grid application, the output voltage is marginally higher than 380 V to ensure power flow from converter to grid. The duty ratio is maintained at 0.65 for the performance evaluation of the converter through simulation and hardware

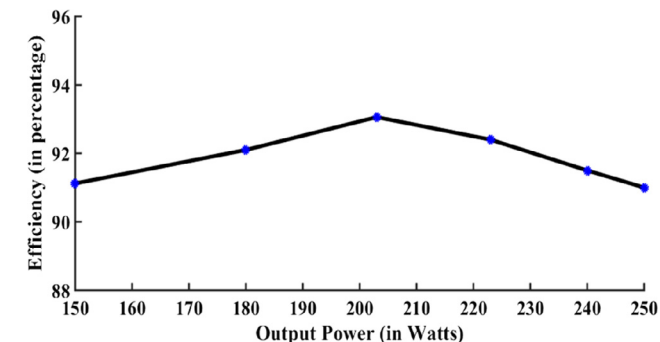


Fig. 12. Output power vs. efficiency curve.

experiment.

Simulation results are represented in Fig. 11(a), (c), (e), (g), (i), (k). Ripples in input current in Fig. 11(a) are due to the switching of inductors. These ripples can be avoided by connecting a large capacitor across the input voltage source of the converter. Simultaneous charging of the inductors during switch ON period and simultaneous discharge of both the inductors during switch OFF period is represented in Fig. 11(c). Fig. 11(e), (i), (g), (k) represent the voltage stress on active switch S, output diode D_0 , switched capacitor cell diodes D_{C1} & D_{C2} and switched inductor cell diodes D_1 & D_2 respectively. Output voltage, current and voltage stress on active switch and diodes are closed to theoretical predicted values.

A hardware prototype of the proposed converter has been developed in laboratory to verify the predicted theoretical results and performance of the converter. The developed prototype converter is shown in Fig. 10. Hardware results are represented in Fig. 11(b), (d), (f), (h), (j), (l). Fig. 11(b) presents input voltage, input current, output voltage and output current. For an input voltage of 34 V and input current of 6.42 A, the output voltage is 384 V and output current is 0.529 A. Fig. 11(d) confirms the simultaneous charging and discharging of the two inductors. The current through both the inductors are 3.09 A. The percentage ripple content matches closely with the desired value for the chosen application. In Fig. 11(f), the voltage stress on switch ‘S’ is shown, which is almost half of the output voltage i.e 194 V. Voltage stresses on diodes are presented in Fig. 11(j), (h) and (l). From Fig. 11(j) and (h), it is clear that the voltage stress on D_0 , D_{C1} and D_{C2} is equal to half of the output voltage. The voltage stress on switched inductor diodes D_1 and D_2 is 96 V which is approximately 25% of the output voltage. The full load efficiency of the converter is 93.06% which is shown in Fig. 12.

The prototype of the converter is connected to solar PV panel and tested in different time duration to check the voltage gain capability of the converter (at required power level) when the output from the solar PV panel varies. Fig. 14(a)–(c) show the output voltage obtained at the output port and the current delivered to the load when the input voltage from the PV panel varies. During the entire operation, when the input voltage varies between 31 V and 38 V, the duty ratio D is adjusted to obtain the required 380 V at the output. The range over which d varies is between $D = 0.67$ and $D = 0.61$. Even when the output from the PV panel reduces to 31 V, the converter is able to provide the required output voltage and deliver the required power to the load at a very safe duty ratio value of $D = 0.67$. Thus, the ability of the proposed converter to yield the required voltage gain when the input voltage undergoes variation and at safe duty ratio value is clearly demonstrated. Fig. 13 represents the test bench setup of the proposed converter connected with solar PV panel.

6. Comparison between the proposed converter and other high gain converters

The performance of the proposed converter is experimentally verified and compared with the other similar types of high gain converters proposed by Axelrod et al. (2008), Wu et al. (2015), Maheri et al. (2017) and Yang and Liang (2009) in Table 2.

6.1. Voltage gain enhancement technique

Passive switched inductor technique is used in the converter proposed by Axelrod et al. (2008) to increase the voltage gain. Switched capacitor technique has been used in Wu et al. (2015) to enhance the voltage gain capability of the converter, whereas a hybrid technique including active switched inductor and switched capacitor method is adopted for the converters proposed by Yang and Liang (2009). Combined active and passive switched inductor technique is implemented in the converter proposed by Maheri et al. (2017) to achieve high voltage gain. The proposed converter uses a combination of modified passive

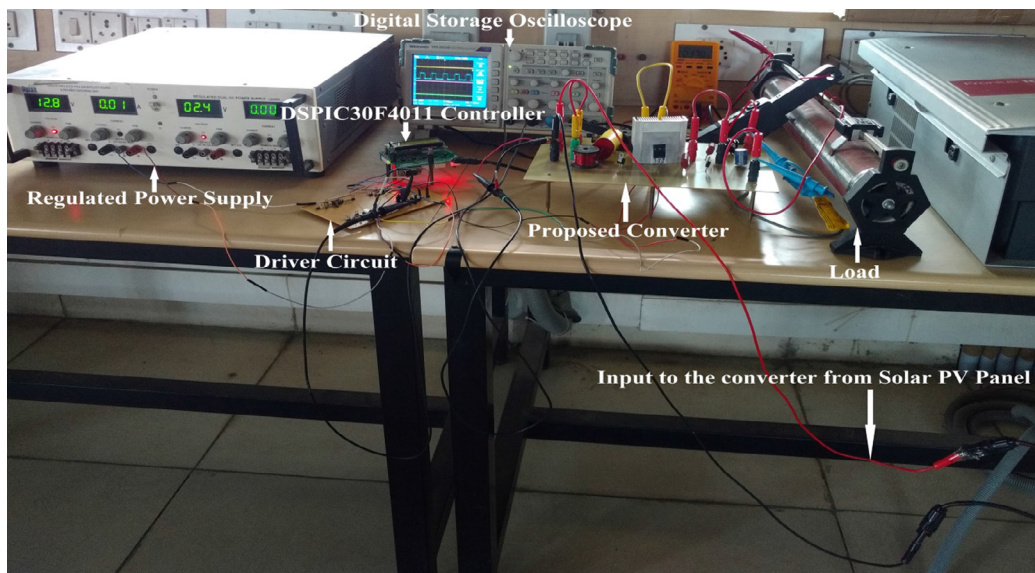
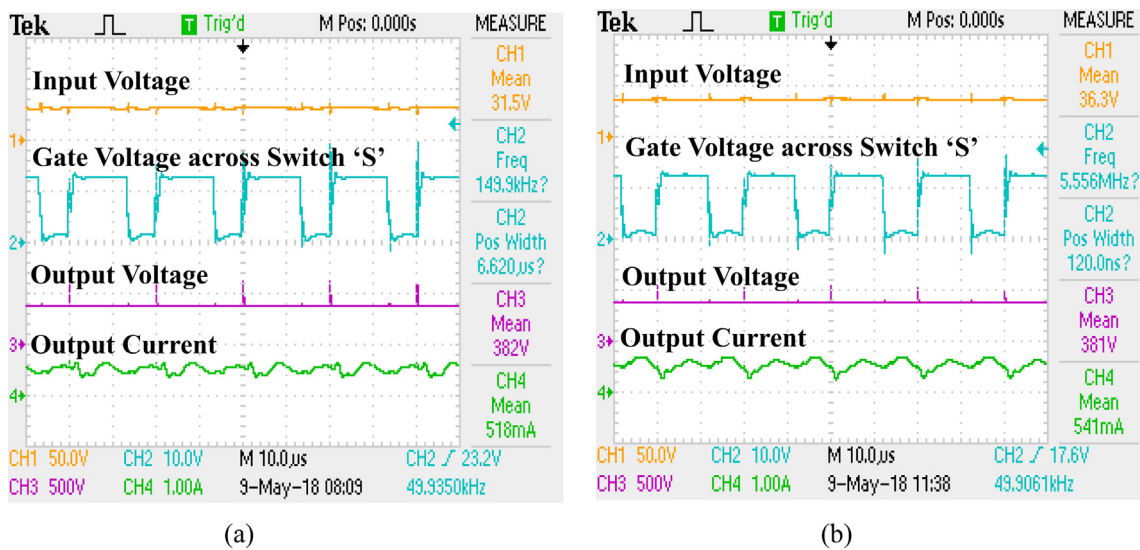
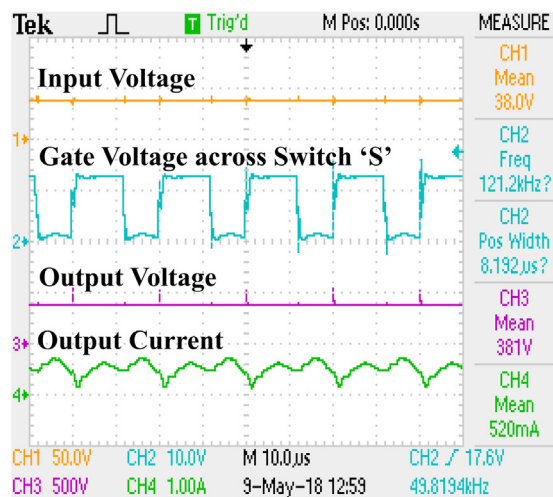


Fig. 13. Test bench setup of the proposed converter connected with solar PV panel.



(a)

(b)



(c)

Fig. 14. Experimental waveforms of the proposed converter for different voltages of solar PV panel.

Table 2
Comparison between the proposed converter and other high gain converters.

| Parameters | SI converter (Axelrod et al., 2008) | SIESC-SC converter (Gang Wu et al., 2015) | Converters in (Yang and Liang, 2009) | | | Combined passive and active SI converter (Maheri et al., 2017) | Proposed converter |
|--|-------------------------------------|---|--------------------------------------|--------------------|-------------------------|---|--------------------|
| | | | Converter I | Converter II | Converter III | | |
| Voltage gain | $\frac{(1+D)}{(1-D)}$ | $\frac{2}{(1-D)}$ | $\frac{(1+D)}{(1-D)}$ | $\frac{2}{(1-D)}$ | $\frac{(3-D)}{(1-D)}$ | $\frac{(1+3D)}{(1-D)}$ | $\frac{4}{(1-D)}$ |
| Voltage stress on active switches | V_0 | $\frac{V_0}{2}$ | $\frac{V_0+V_{in}}{2}$ | $\frac{V_0}{2}$ | $\frac{V_0-V_{in}}{2}$ | $V_{S1} = V_{S2} = \frac{V_0+3V_{in}}{4}$ $V_{S3} = \frac{V_0+2V_{in}}{4}$ $V_{S4} = \frac{3V_0+V_{in}}{4}$ | $\frac{V_0}{2}$ |
| Voltage stress on active switches (% of output voltage at 0.65 duty) | 100 | 50 | 62.9 | 50 | 42.55 | 33.9 (for S_1 & S_2) 27.9 (for S_3) 77.9 (for S_4) | 50 |
| Voltage stress on output diodes | V_0 | $\frac{V_0}{2}$ | V_0-V_{in} | V_0 | V_0-V_{in} | $V_0 + V_{in}$ | $\frac{V_0}{2}$ |
| Voltage stress on passive SI diodes | $\frac{V_0-V_{in}}{2}$ | - | - | - | - | - | $\frac{V_0}{4}$ |
| Voltage stress on active SI diodes | - | - | - | - | - | $V_{D_UP} = V_{in}V_{D_LOW} = \frac{V_0-V_{in}}{4}$ | - |
| Voltage stress on SC diodes | - | $\frac{V_0}{2}$ | - | $\frac{V_0}{2}$ | $\frac{V_0-V_{in}}{2}$ | - | $\frac{V_0}{2}$ |
| Number of active switches | 1 | 1 | 2 | 2 | 2 | 4 | 1 |
| Number of diodes | 4 | 3 | 1 | 2 | 3 | 5 | 5 |
| Number of capacitors | 1 | 3 | 1 | 2 | 3 | 1 | 4 |
| Number of inductors | 2 | 1 | 2 | 2 | 2 | 4 | 2 |
| Voltage gain to total number of component count (TCC) ratio | $\frac{(1+D)}{8(1-D)}$ | $\frac{1}{4(1-D)}$ | $\frac{(1+D)}{6(1-D)}$ | $\frac{1}{4(1-D)}$ | $\frac{(3-D)}{10(1-D)}$ | $\frac{(1+3D)}{14(1-D)}$ | $\frac{1}{3(1-D)}$ |
| Voltage gain to total number of TCC ratio at D = 0.65 | 0.589 | 0.714 | 0.785 | 0.714 | 0.671 | 0.602 | 0.952 |

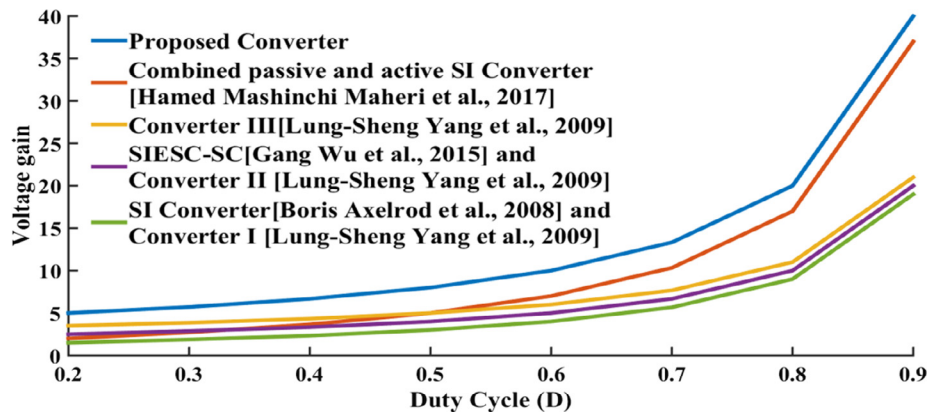


Fig. 15. Comparison of voltage gain of different high gain converters and the proposed converter.

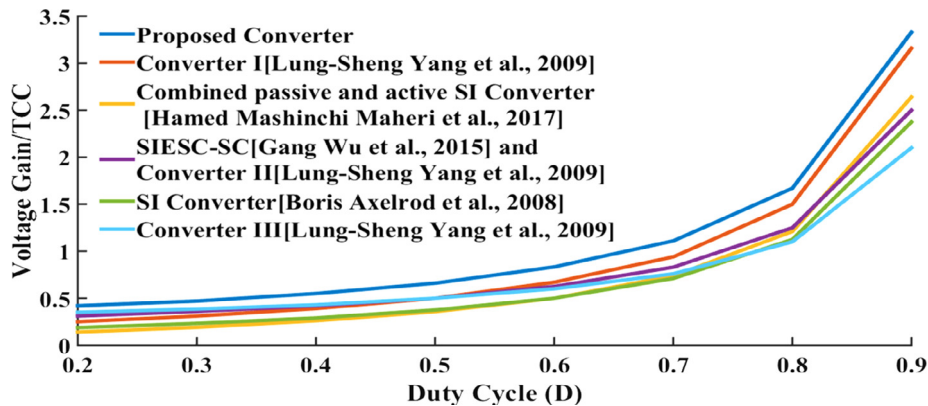


Fig. 16. Comparison of voltage gain to total component count (TCC) ratio at different D.

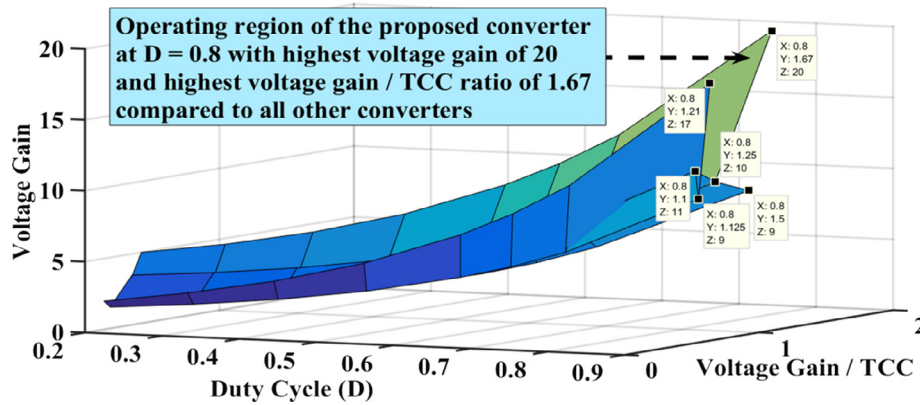


Fig. 17. Plot showing the operating region of the proposed converter and comparison of G_{CCM} and G_{CCM}/TCC with other converters.

switched inductor technology with an additional capacitor and switched capacitor technology to achieve high voltage gain. In the proposed converter, due to the use of switched capacitors, significant amount of energy is stored across the energy storage elements. Consequently, besides providing a practical voltage gain of 11.29, the proposed converter utilizes the benefit of having little output voltage ripple due to the switched capacitors.

6.2. Voltage gain

The voltage gain of the proposed converter is significantly higher than other converters due to the voltage lifting method adopted for all the values of D . The theoretical voltage gain of the proposed converter at $D = 0.65$ is 11.43 whereas the other converters provide a theoretical gain in the range of 4.7–8.43 at $D = 0.65$. Fig. 15 represents a comparative study of the voltage gain of the proposed converter and other high gain converters mentioned.

6.3. Voltage gain/total component count (G_{CCM}/TCC) ratio

It is also confirmed from Table 2 that a high voltage gain can be achieved with less number of component counts in the proposed converter as compared to other converters. Further, for the proposed converter high power handing capability and better component utilization factor of the converter is ensured. Fig. 16 confirms that the proposed converter offers high voltage gain with less numbers of components involved in the circuit. Fig. 17 shows the three dimensional plot of voltage gain, G_{CCM}/TCC ratio and duty cycle. The operating points of all the converters considered for comparison are marked. The proposed converter offers the highest voltage gain of 11.29 and G_{CCM}/TCC ratio of 0.952 at $D = 0.65$. Though Converter I of Yang and Liang (2009) uses the least number of components, the voltage gain offered by this converter is only 4.70. Further, the proposed converter offers larger operating area compared to other converters with high G_{CCM}/TCC ratio as envisaged from Fig. 17.

6.4. Voltage stress on semiconductor devices

In case of passive switched inductor based topology, the voltage stress on active switch is equal to output voltage. In the proposed converter, interfacing the switched capacitor cell between the modified switched inductor cell and output diode results in reduced voltage stress on the active switch. The active switch experiences a voltage stress which is 50% of output voltage. Further, the voltage stress is independent of duty ratio. In converter I, converter III of Yang and Liang (2009) and combined passive and active SI converter of Maheri et al. (2017), the voltage stress on the switches are dependent on duty ratio. Though, one of the switches in Maheri et al. (2017) is subjected to

the least stress which is about 27.9% of V_0 at $D = 0.65$ and with two active SI networks, increment in value of duty ratio (to meet the voltage gain requirement) is expected to cause an increment in the switch voltage stress also. But the last switch (S4) of Maheri et al. (2017) experiences very high (77.9% of V_0 at $D = 0.65$) voltage stress on it. Converter III (Axelrod et al., 2008) and combined passive and active switched inductor converter (Maheri et al., 2017) use additional switches to reduce the voltage stress at the expense of reduced voltage gain and G_{CCM}/TCC ratio.

In Wu et al. (2015) and the proposed converter, the voltage stress on output diode is about 50% of the output voltage and is the lowest among all the converters. The diodes present in modified passive switched inductor cell (D_1, D_2) of proposed converter is subjected to a stress of only 25% of the output voltage, whereas the diodes present in SC cell is exposed to a voltage stress of 50% of the output voltage.

7. Conclusion

A non-isolated high step-up switched inductor-switched capacitor based DC-DC converter is presented in this paper. The structure of the proposed converter is obtained by judiciously modifying basic SI-SC converter. The modifications are (i) introduction of boost capacitor in passive switched inductor cell and (ii) combination of this arrangement with basic SC cell. The novel voltage gain technique adopted in the proposed converter yields a voltage gain of 11.29. Since SI and SC were used along with a boost capacitor, the voltage stress experienced by the switch is reduced to 50% which is only a fraction of the output voltage. Experimental results obtained from a prototype converter prove that the converter handles 200 W power at 93% efficiency and provides a voltage gain of 11.29. As only single active switch is used, the proposed converter offers better component utilization besides being amenable for implementing control algorithms easily. The salient features of the proposed converter make it a promising candidate for interfacing the input PV source with a 380 V DC bus or a DC micro grid.

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