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Carrier extraction based synchronization scheme for distributed DC–DC converters in DC-Microgrid

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ABSTRACT

In this paper, a novel PWM carrier synchronization method is proposed for distributed DC–DC converters in DC-Microgrids. The synchronization method is based on carrier frequency extraction from DC-bus voltage ripple. In addition, an advanced phase shift control algorithm for the synchronized carriers is implemented to reduce the DC bus voltage ripple contents. A DC-Microgrid encompassing different distributed energy resources with their DC–DC converters is modeled using Matlab\Simulink to test the proposed synchronization method and control algorithm. Then, a small power scale experimental testbed is built in order to validate the simulation results. The simulation and the experimental results demonstrated that the proposed method and algorithm are very promising to minimize DC-bus ripple contents in DC-Microgrid applications.

1. Introduction

The new trend in future power generation systems is developing toward Distributed Generators (DGs), which means that energy conversion systems are situated close to energy consumers and large units are substituted by smaller ones [1]. The integration of these DGs, energy storage systems, and distributed electric loads through the point of common coupling is called a Microgrid (MG) [2]. MGs can be configured into DC (DCMG) and AC (ACMGs) based on the power electronics interface circuits that will be used [3].

Recently, there has been a general upsurge of interest in using DCMGs being described as flexible, intelligent, and active power networks [4]. In addition, they are able to improve system reliability, efficiency, and security leading to promote and increase the renewable energy sources integration [5]. In DCMGs, a DC–DC boost converter is a key element to interface DGs to the MG's DC-bus [6]. Various DC–DC boost converters topologies have been studied in Refs. [7–12]. DCMGs along with their DC–DC boost converters still face numerous challenges such as ripple contents of the MG DC-bus voltage and current [13]. Indeed, voltage and current ripple are among the various phenomena that contribute to a reduction in lifespan of power sources and energy storage devices interfaced to the DC-bus [14,15].

Multi-Phase Interleaved Boost Converters (MP-IBCs) are introduced in applications such as electric vehicles to interface different DC power sources to a common DC bus achieving low ripples contents in the input current and the output voltage [16,17]. The pulse width modulation (PWM) signals of these converters are generated based on multiple carriers with the same frequency and different phase angles. The synchronization of these multiple PWM carriers are quite easy since all the PWM modulators are driven from the same controller and hence the same oscillator [18]. In addition, the phase angles can be easily considered as 360/N where N is the number of converters as mentioned in Ref. [19].

In applications such as DCMGs, each DG along with its converter has its own local controller (LC) and hence its own oscillator which makes the PWM carriers synchronization is a big challenge. This challenge is related to the frequency drift of each oscillator due to temperature and component tolerance. This drift will create a continuous change in the phase shift angle between PWM carriers of each converter [20,21]. To ensure the most accurate synchronization process, it should be taking into account clock drift and start latency by using the available real-time system integration [22]. In

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Nomenclature

ACMGs	AC Microgrids
BPF	Band pass filter
BPSO	Binary Particle Swarm Optimization
DCMG	DC Microgrids
DGs	Distributed Generators
$f_{v_{cr}}$	DC-bus's carrier frequency
LC	Local software oscillator (controller)
MGEMC	Microgrid energy management center
MP-IBCs	Multi-Phase Interleaved Boost Converters
PLL	Phase Locked Loop
PSCA	Phase shift control algorithm
PWM	Pulse width modulations
v_{cr}	DC-bus's ripple carrier
v_{cr_lc}	Local oscillator's PWM carrier
v_{cr_RMS}	The root mean square value of DC-bus's ripple magnitude
$T_{S_{\theta_i}}$	Sampling time of the step angle variation of converter number i
$\theta_{v_{cr}}$	DC-bus's carrier angle
$\theta_{v_{cr\_lc}}$	The carrier phase angle of each local oscillator
θ_i	Phase angle during perturbation of converter number i
θ_{i_opt}	Optimum phase angle reached after perturbation for converter number i
$\Delta\theta$	Phase step angle

Ref. [23], a theoretical study has been presented for DC-bus voltage ripple minimization of distributed DC–DC converters based on phase shifting theory. However, there is no experimental study to validate that theory.

In this article, a simulation study as well as an experimental investigation for the aforementioned study is presented. The proposed method is investigated based on extracting the carrier frequency information from the DC-bus voltage ripples to generate a very accurate and stable time reference in order to generate synchronized PWM carriers for DC–DC converters. One of the DCMGs converters will be chosen by the Microgrid energy management center (MGEMC) to work as a master converter. This converter will be responsible to regulate the carrier frequency of the DC-bus. The other converters, slave converters, interfaced to the DC-bus will receive the carrier frequency component based on measurements from the bus ripples and will synchronize their local frequency to this carrier. Following the synchronization process, LC based on DC-bus voltage measurements will run its phase shift control algorithm (PSCA) in order to deliver the optimum phase angle of PWM carriers and minimize the DC-bus ripple.

The proposed method is implemented using software only and does not need special communication networks between distributed converters for the synchronization process since all converters are already interfaced to the same DC-bus. In addition, it has the ability to reduce the ripple and DC-link capacitor size, which will improve system EMI and power efficiency. Moreover, it eliminates the need for a high input filtering system in the converter design which will decrease its size and cost.

The paper is organized as follows: Section 1 describes the proposed MG power system. In Section 2, the PWM generation process is presented with the new phase shift control algorithm. The simulation results are introduced in Section 4 and the experimental setup with its results are presented and discussed in Section 5.

2. DCMG system description

The schematic diagram of DCMG and control hierarchy is depicted in Fig. 1. It shows x number of parallel DC–DC converters connecting x number of DGs to the DCMGs DC-bus. The MG under consideration has three conventional DC–DC boost converters connected in parallel to interface the three different DGs to the DCMG's DC-bus; (x = 3). In this work, the LC of each DG should have two layers. The first layer, the carrier extraction and synchronization algorithm, aims to generate synchronized PWM carriers based on carrier frequency extracted from DC-bus voltage ripples and optimum phase shift angles obtained by PSCA. The second layer, voltage and current controllers, is responsible to control the duty cycle of its converter based on the measured power and the reference power which is sent by the MGEMC [24]. The MGEMC should deliver these reference values using robust and fast optimization algorithm in order to achieve the optimal power allocation in real-time. In this work, the proposed optimization model is solved using Binary Particle Swarm Optimization algorithm (BPSO) considering two inconsistent objectives where the total DCMG operating costs and the associated pollutant emission were analyzed. Constraint functions were added to the optimization problem to reflect some of the additional considerations often found in a small-scale generation system such as load power balance and supply capacity limits. More details regarding MGEMC methodology are mentioned in Ref. [25]. The following sections will present the main work of each LC to generate the appropriate PWM signal in order to minimize DC-bus ripples which is considered the main objective of the paper work.

3. PWM carrier generation

In this section, the PWM carrier generation process of distributed DC–DC converters will be illustrated and discussed. One of these converters will be chosen by MGEMC to work as a master converter to regulate the DC-bus voltage. The switching frequency of this converter will be chosen considering MG's power level, converters design and safe operation. The other converters, slave converters, will receive the carrier frequency component based on measurements from the bus ripples and will synchronize their local frequency to this carrier. The LC of these converters will perform the PWM generation process using three steps which will be discussed in the following sub-sections.

3.1. Step1: DC-bus frequency and angle extraction

The DC-bus's voltage consists of the DC average value and the AC switching frequency component. The AC component is the one responsible for the voltage ripple. To extract the carrier frequency based on the AC component, the LC of each slave converter will use a band pass filter (BPF) to isolate the ripple component produced by the carrier frequency from the measured DC-bus voltage. The BPF will be tuned to pass only carrier frequency and reject all other harmonics, this is necessary to reject any harmonics produced by nonlinear loads. The filter output will have the same switching frequency of the master converter and fixed phase angle with respect to the master carrier. The upper and lower bands of the BPF are chosen 2.1 kHz and 1.9 kHz based on the switching frequency which is set for 2 kHz for all converters presented in this paper. The output of the BPF will be considered as the DC-bus's carrier (v_{cr}). This carrier will be fed to the Phase Locked Loop (PLL) to extract the DC-bus's carrier frequency ($f_{v_{cr}}$) and the DC-bus's carrier angle ($\theta_{v_{cr}}$) as shown in Fig. 2. Since the carrier frequency has the highest magnitude of the DC-bus voltage ripple, the root mean square value (v_{cr_RMS}) is calculated from the output of the BPF to be used as an indicator for the DC-bus's ripple magnitude.

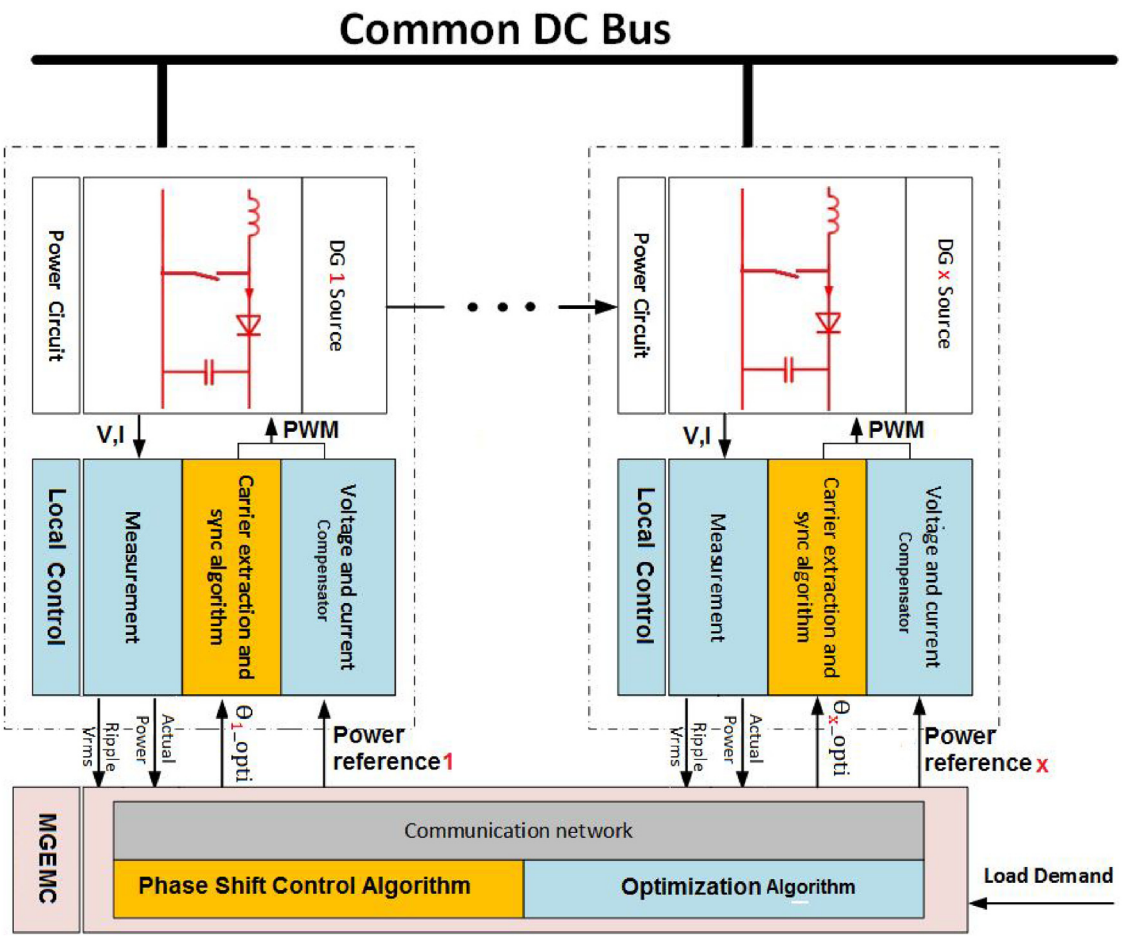

Fig. 1. DCMG scheme.

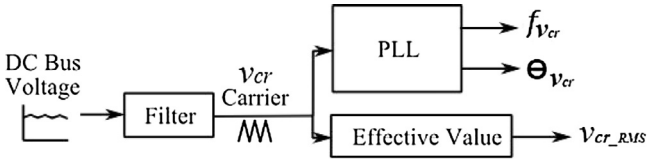

Fig. 2. DC-bus ripple measurements unit of each LC.

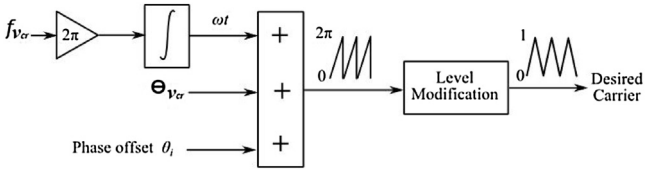

Fig. 3. Initial PWM carrier generation block of each LC.

3.2. Step 2: PWM carrier synchronization

In this step, the LC will start to generate its initial PWM carrier (v_{cr_lc}) with frequency equal to $f_{v_{cr}}$ and phase angle equal to $\theta_{v_{cr}}$ as shown in Fig. 3. This step is essential in order to keep all PWM carriers synchronized to the DC-bus's carrier frequency. Initially, the phase offset angle (θ_i) is set to zero and will be controlled and optimized to minimize DC-bus ripple in Section 3.3. This step will not impose impractical restrictions for other converters in MG power system since all power converters in low power MGs should be designed usually to operate in the range of thousands Hz to tens of kHz.

3.3. Phase shift control algorithm implementation

Following the PWM carrier synchronization process, the PSCA implemented by MGEMC will work to minimize DC-bus ripple magnitude. The following three steps will present the operation of PSCA.

3.3.1. Perturbation and observation

The PSCA will start to perturb the $\theta_{v_{cr}}$ by adding an incremental θ_i from 0 to 360° with fixed step angle ($\Delta\theta$) for each converter and observe the change in the v_{cr_RMS}. $\Delta\theta$ is set to 30° in our case study. For successful coordination between local controllers, each LC will start with the same step angle but with different sampling time ($T_{S_{\theta_i}}$). This sampling time will be arranged between different sources according to the dynamics response of each system. $T_{S_{\theta_i}}$ will be calculated based on the step angle $\Delta\theta$ as in the following equation:

$$T_{S_{\theta_{i+1}}} = T_{S_{\theta_i}} * \left(\frac{\Delta\theta}{360}\right) \quad (1)$$

where i is the converter number and should be ≥2.

3.3.2. Optimum angle and minimum ripple detection

The second step is used for the online detection of the lowest level of v_{cr_RMS} which represents the lowest ripple contents of DC-bus. Once the lowest level is detected, the corresponding θ_i will be

Table 1
The experimental test-bed parameters.

Parameters	Values
Inductance ($L_1 = L_2 = L_3$)	750 μH
Inductor resistance (R_l)	20 mΩ
Capacitance (C)	312 μF
Capacitor resistance (R_c)	0.575 mΩ
DC bus voltage	50 V
DC source 1 voltage	25 V
DC source 2 voltage	22 V
DC source 3 voltage	20 V
Load resistance	4 Ω
Switching frequency (f_s)	2 kHz
$\Delta\theta$	30°
Ts_{θ_2}	0.6 s
Ts_{θ_3}	0.05 s

considered as the optimum one (θ_{i_opt}) and the final local carrier phase angle can be calculated by adding the θ_{i_opt} to the $\theta_{v_{cr}}$.

3.3.3. Final PWM generation

In the last step of PSCA operation, the LC will generate v_{cr_lc} with frequency equal to $f_{v_{cr}}$ and phase angle equal to ($\theta_{i\_opt} + \theta_{v_{cr}}$).

The main advantage of this method can be summarized as follows:

- Generating a PWM carrier signal in synchronization with the DC-bus carrier frequency.
- Detecting the global minimum of the DC-bus ripple magnitude.
- Obtaining the optimum phase shift of the local converter PWM carrier.
- The method does not effect on the stability of the converters' controllers.
- The method could be processed online without interrupting the operation of the converter.

A simplified flowchart explaining the step techniques that are employed to generate PWM carriers for DC–DC converters is described in Fig. 4.

4. Simulation results and discussion

4.1. DCMG modeling

In this section, the MG model shown in Fig. 1 and PWM signals generation process shown in Figs. 2 and 3 are built based on MATLAB/SIMULINK® to test and validate the robustness of the proposed methods. The SIMULINK model has three DC voltage control sources to represent the DGs of the studied DCMG. These sources are interfaced to a common DC-bus through a distributed DC–DC boost converter as shown in Fig. 5. The DC–DC converters parameters are mentioned in Table 1.

It is assumed that all converters will be controlled simultaneously. The local control of each DG is implemented to control the converter's duty ratio (d) and its PWM carriers. To control the duty cycle of the master DC-DC converter, the voltage $C_v(s)$ and current $C_i(s)$ compensators based on an advanced lead-lag controller are employed during transient and steady-state conditions as shown in shown in Fig. 6. On the other hand, the current compensator is employed for the slave converters as shown in Fig. 7. The theory and derivations of the compensators are discussed and analyzed in details in Refs. [26,27] where the small signal model $H_i(s)$ and $H_v(s)$ of each converter can be found in detail in Refs. [28,29].

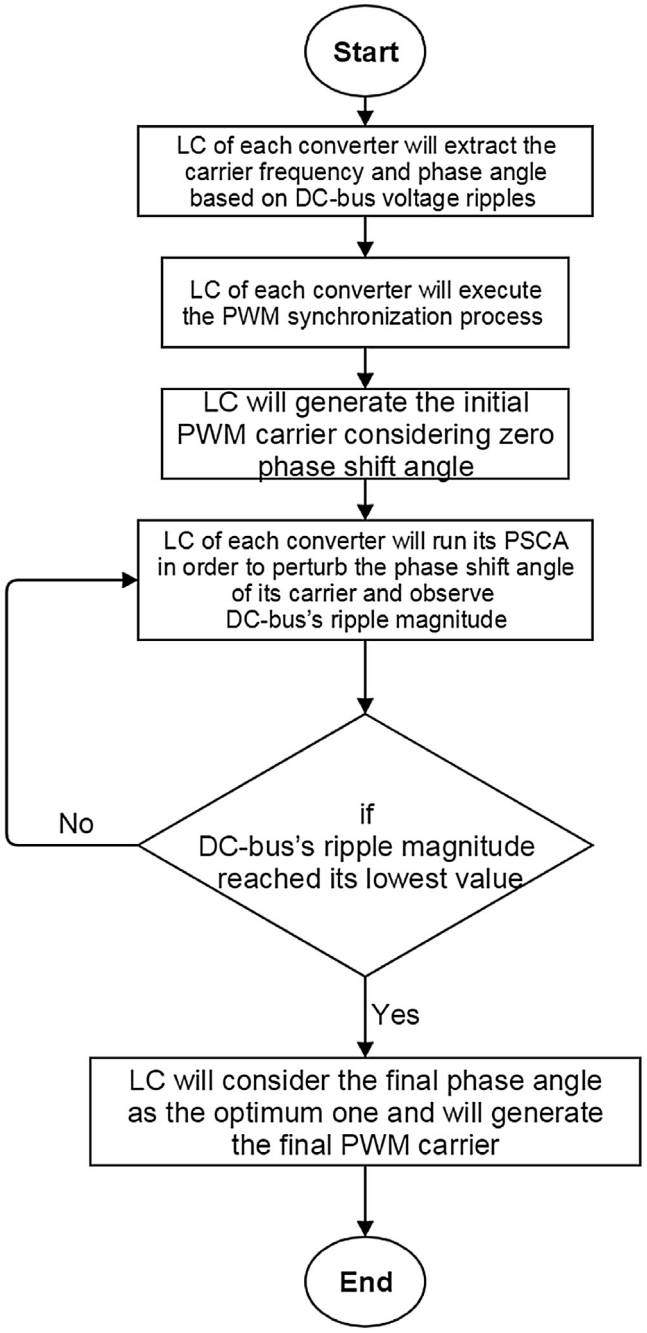

Fig. 4. The steps techniques employed for generating PWM.

4.2. Simulation results

This section will discuss and analyze the simulation results of the proposed DCMG. Fig. 8 shows the DC-bus voltage (V_o) which is well regulated at 50 V using master converter's voltage control.

Based on the regulated DC-bus voltage, each LC will start the synchronization process by extracting frequency from DC-bus voltage ripple as shown in Fig. 9 and as described in Section 3.1. Following this step, LC will generate the initial PWM carrier based on the extracted frequency as shown in Fig. 10.

In order to obtain the lowest ripple magnitude, LC using its PSCA will start to perturb the phase offset angle of its carrier and monitor the DC-bus ripple magnitude. In this work, the PSCA considered the $\Delta\theta$ equal to 30° and the variation sampling time is set to 0.05 s for converter 3 and 0.6 s for converter 2 (see Eq. (1)). The phase angle

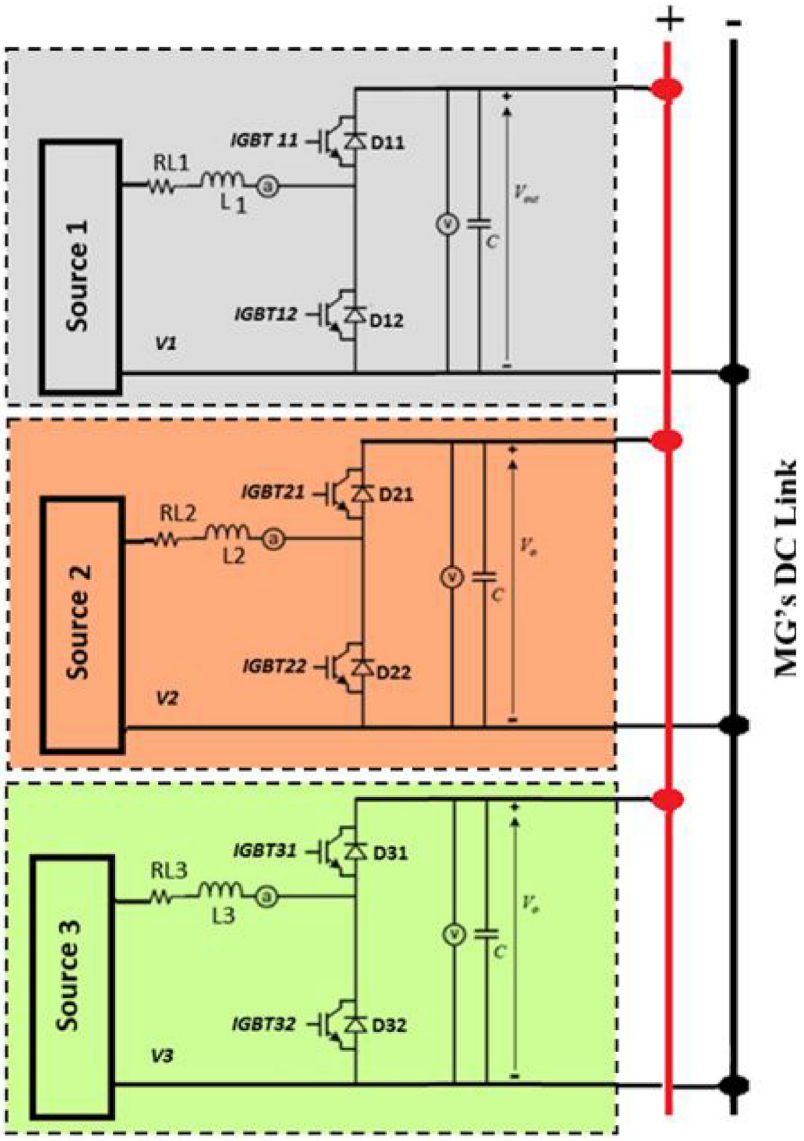

Fig. 5. DC–DC converters interfaced to MG' DC bus.

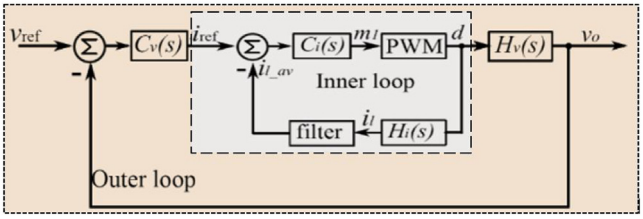

Fig. 6. Voltage and current control scheme.

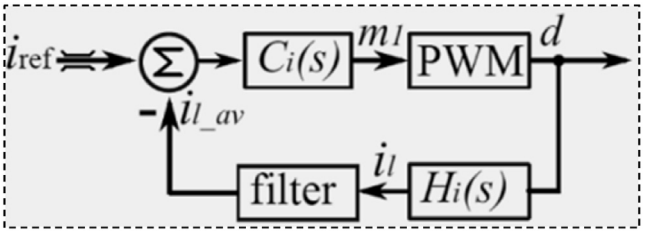

Fig. 7. Current control scheme.

variation for both converters is shown in Fig. 11. The overall time of the perturbation process is set to 7.2 s in order to use all possibilities of $\Delta\theta$ for both converters. According to the perturbation of $\theta_{v_{cr}}$, the v_{cr_RMS} and its instantaneous value will be also varied as shown in Fig. 12.

PSCA will start the observation process in order to detect the lowest magnitude of the DC-bus ripple. It can be noticed from Fig. 13 that the lowest ripple magnitude is detected at the time interval between 3.95 s and 4 s. The corresponding phase angle at this interval will be defined as θ_{2_opt} for converter 2 and θ_{3_opt} for converter 3. These values are recorded equal to 180° and 210°. By sending θ_{2_opt} and θ_{3_opt} to local controller two and three respectively, the final PWM carrier of both converters can be generated and will be considered as the steady state carriers after the test period as shown in Fig. 14.

Fig. 15 shows the ripple contents of the DC-bus voltage during and after the PSCA operation. It is clear from this figure that PSCA after 7.2 s is succeeded to minimize the voltage ripple (ΔV) contents from 9 V to 0.8 V. As a result, these results showed that the

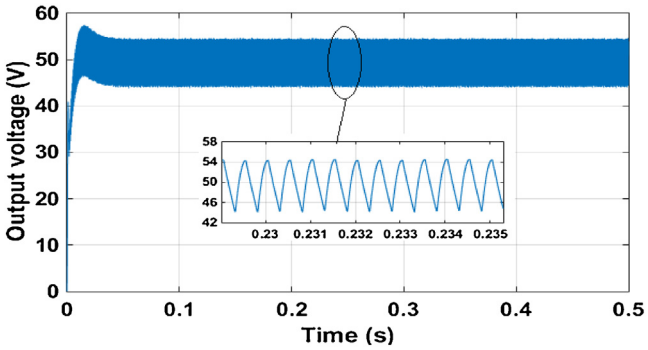

Fig. 8. DC-bus voltage before using PSCA.

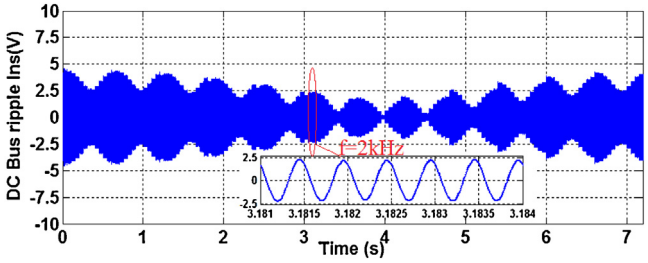

Fig. 9. DC-bus carrier frequency.

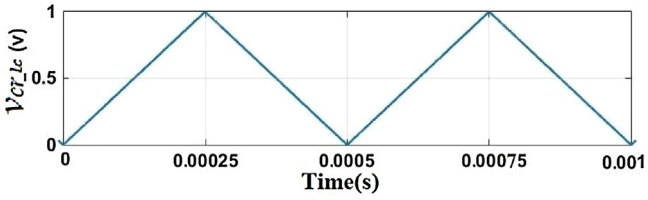

Fig. 10. Initial PWM carrier for all DC–DC converters.

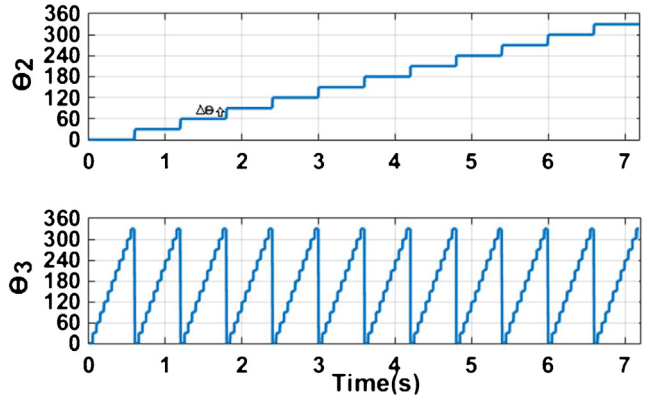

Fig. 11. Variation of θ_i for converter 2 and converter 3.

proposed method is very efficient and effective in DC-bus ripple minimization.

5. Hardware implementation

In order to implement the proposed algorithm in real-time, an experimental test bench, shown in Fig. 16, has been designed. Three DC programmable power supplies, i.e., EA-SI8080 and GEC5000, are used as three different DGs. The N3300A–1800 W Programmable Electronic load is used as load. Three modules of DC–DC boost converters are connected in parallel to have the same structure of

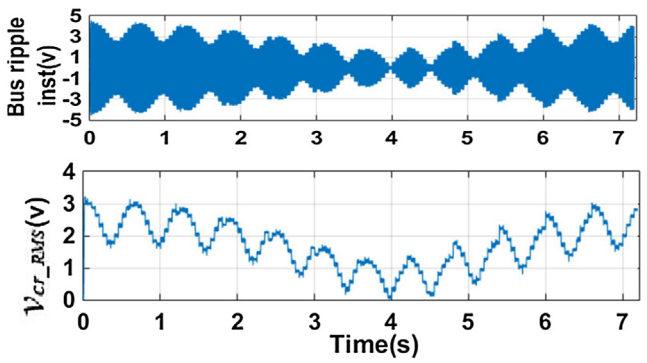

Fig. 12. Ripple variation according to the perturbation in θ_i.

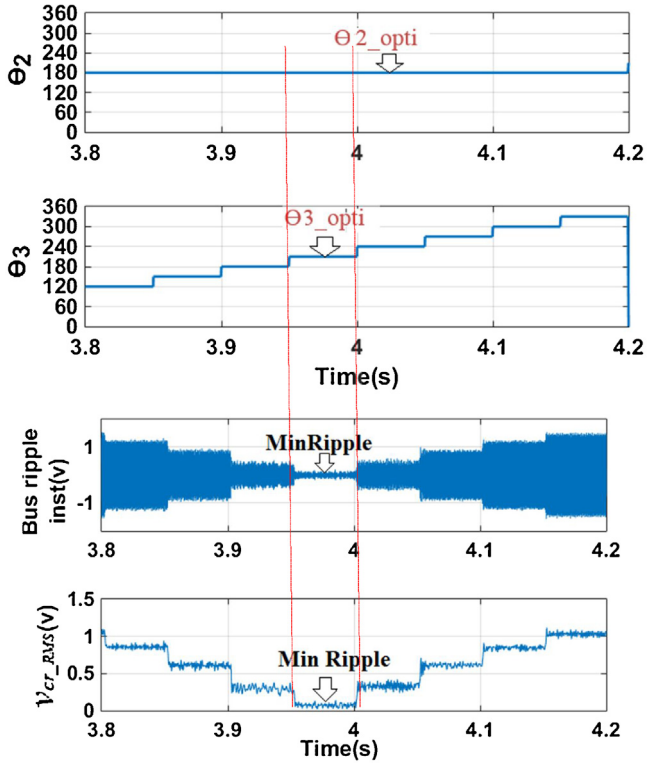

Fig. 13. Minimum ripple and optimum phase shift detection.

distributed converters in order to integrate all sources to common DC-bus. The parameters of the boost converters and PSCA are listed in Table 1. Moreover, MTX1032 is used respectively as differential voltage probes to measure the actual voltage signal. On the other hand, the Tektronix dpo2014 digital storage oscilloscope is used to display the results.

5.1. Control design and implementation

The control system is divided based on the speed and functions to two layers, low (local) and high level control (MGEMC) layers as shown in Fig. 17.

5.1.1. Low level (local) control design

In this work, the ARM Cortex M4 Microcontroller is used to implement the functions of the local controller. This control layer performs fast computation for the control action and protection function which requires high bandwidth with a fast and predictable time response. The DSP extension for the ARM Cortex M4 assists in fast computation of the control output. The built in dedicated

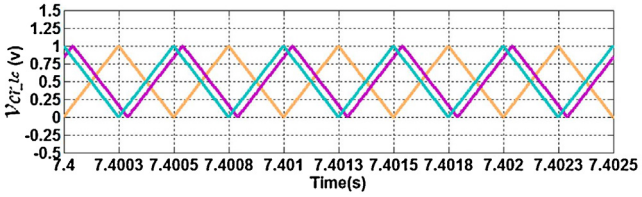

Fig. 14. PWM carriers based on optimum phase shift angles. (Orange: converter 1; Cyan: converter 2; Magenta: converter 3). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

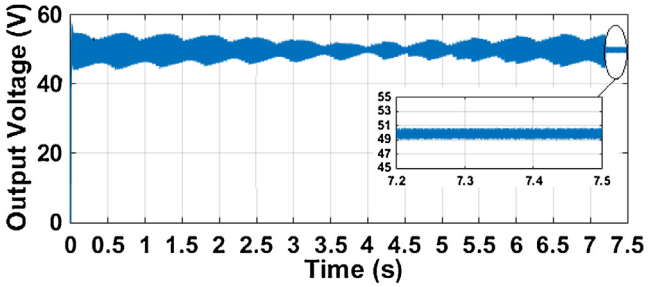

Fig. 15. DC-bus voltage during and after using PSCA.

analog to digital converters with direct memory access make it possible to acquire analog feedback signals with a fast sampling rate while operating at fast switching frequencies. The STM32f407vgt6 32 Bit ARM cortex M4 processor running at 160 MHz was used for the embedded implementation of the low level control layer. The main purposes of the LC are to guarantee PWM carrier synchronization process based on DC-bus voltage measurements and step angle control for each controller based on advanced PSCA.

5.1.2. High level control design (MGEMC)

The high level control layer based on the dSPACE 1104 is used also in this work as a MGEMC. The first objective of this layer is to send the power reference of each DG and then its controller. In this work, the reference power for converter 2 and converter 3 obtained by MGEMC are equal to 165W and 185W respectively. The data exchange between local controllers and MGEMC is made through the dSPACE RS-485 serial interface.

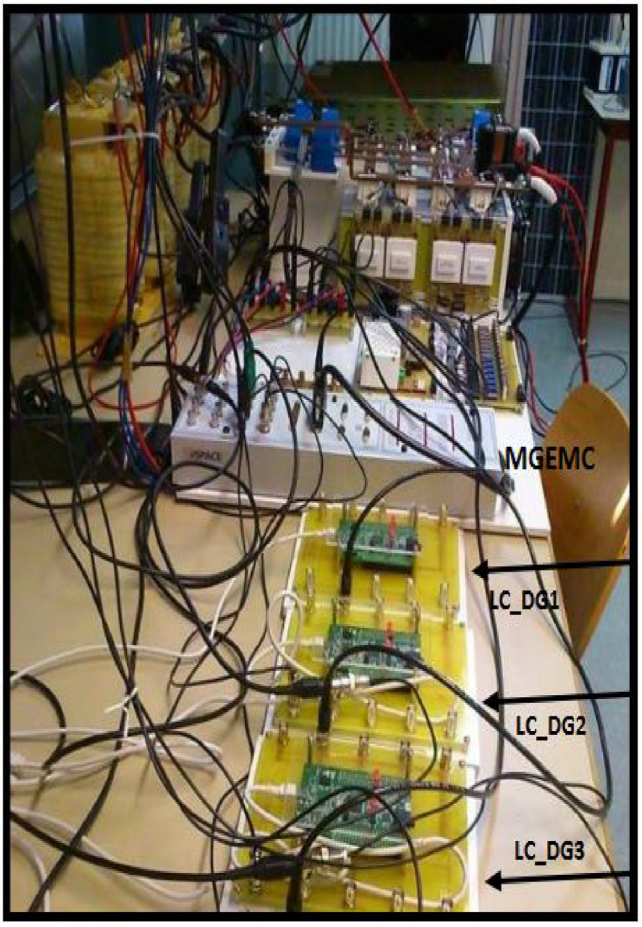

Fig. 17. Low and high level control layer.

5.2. Experimental results

This section presents the experimental results which are obtained based on the proposed algorithm (PSCA). Fig. 18 shows the DC-bus voltage which is regulated at 50 V by using the voltage and current control design of the master controller. The DC-bus's carrier frequency and phase angle are measured based on DC-bus voltage. Following to the initialization step, the perturbation process for converter two and three will be started as shown in Fig. 19.

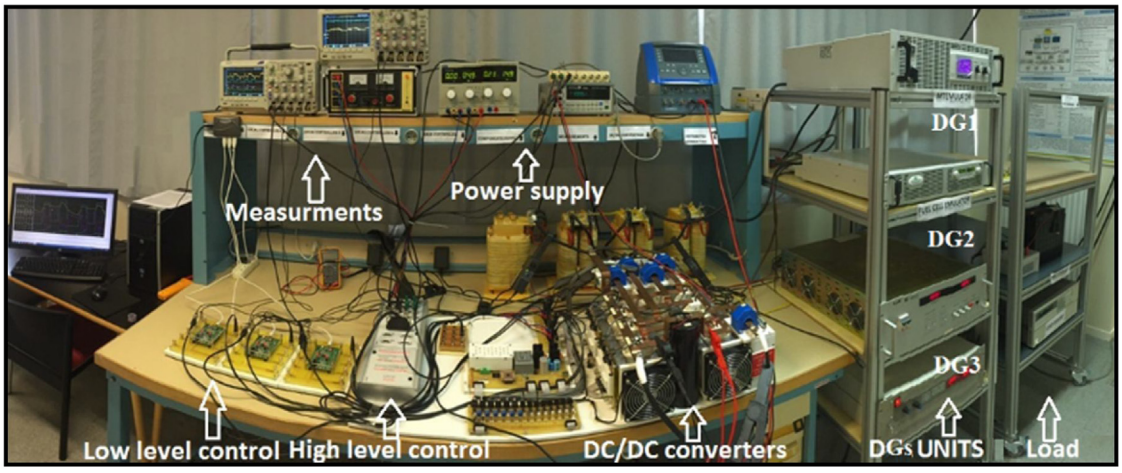

Fig. 16. DCMG testbed.

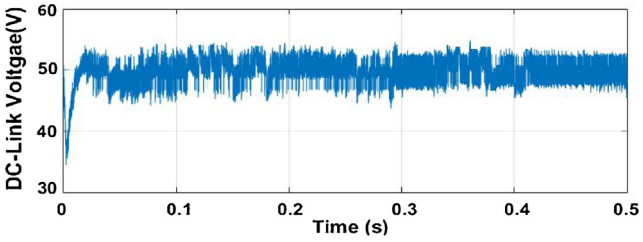

Fig. 18. DC-bus voltage without using PSCA.

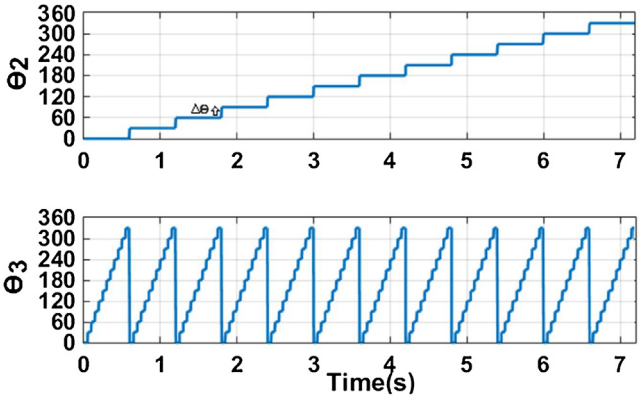

Fig. 19. Assumed θ_i for converter two and converter three.

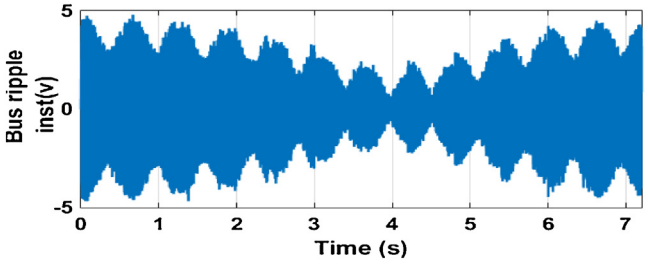

Fig. 20. Variation of DC-bus ripple according to θ_i variation.

As the simulation work, the θ_i is chosen to be varied from 0 until 360 with $\Delta\theta$ equal to 30°, and its sampling time is assumed to be 0.6 s for converter 2 and 0.05 s for converter 3. According to this perturbation, the ripple magnitude of DC-bus is recorded during test period (7.2 s) as shown in Fig. 20. The online PSCA will start to monitor the variation of DC-bus ripple magnitude in order to globally detect the lowest ripple magnitude during test period. The lowest ripple magnitude and the optimum phase angles are detected in the time interval between 3.95 s and 4s. The corresponding optimum phase shift θ_{i_opt} is indexed as 180° degree for converter 2 and 210° for converter 3.

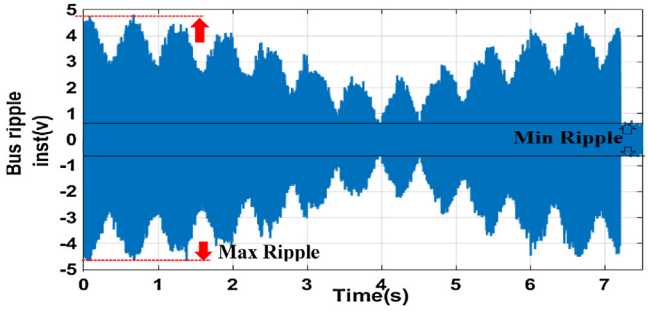

Fig. 22. DC-bus ripple during and after using PSCA.

Fig. 21 shows v_{cr_lc} for each converter. These carriers will be considered by each controller after the end of the test period which set to be 7.2 s. It is clear from the figure that all PWM carriers are synchronized to the PWM carrier of the master converter. The difference in the DC-bus ripple contents during and after using PSCA can be clearly viewed in Fig. 22 in the time interval between 7.2 s and 7.5 s. It worthy to note that DC-bus ripple (ΔV) is decreased from its initial value 9 V to 0.8 V, which reflect the efficient performance of the proposed method.

6. Conclusion

In this paper, a new PWM carrier extraction based synchronization scheme for distributed DC–DC converters in DC-Microgrids is presented. Then, a phase shift control algorithm for synchronized PWM carrier is implemented to minimize the DC bus voltage ripple magnitude. A DC microgrid model encompassing three DGs with their DC–DC converters is used as a prototype to test the proposed synchronization method and DC-bus ripple minimization algorithm based on Matlab\Simulink. The simulation results show that proposed methods have the ability to generate adapted PWM carriers in order to decrease the DC-bus voltage ripple by more than

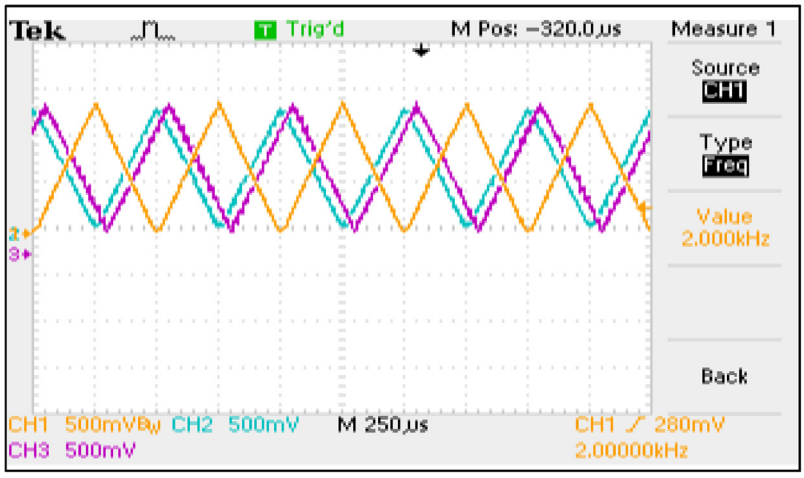

Fig. 21. PWM carrier for each LC.
(Orange: converter1; Cyan: converter 2; Magenta: converter 3). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

70%. In addition, a small power scale experimental test-bed has been built in order to test the proposed methods and validate the simulation results. Experimental results have also demonstrated that the proposed method is very promising to minimize ripple contents of DC–DC converters that are interfaced to the DCMG's DC-bus.

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