New Fundamental Multilevel Inverter with Reduced Number of Switching Elements

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***Abstract*—This research presents an optimum asymmetric fundamental inverter for cascaded multilevel inverters. This circuit can produce total voltage levels without any extra circuit. Then, cascaded structures were used in order to determine the magnitudes of DC links which have been suggested. The advantage of the suggested cascaded connection is the increasing of the output voltage levels in the same number of switching elements, in comparison with other cascaded structures. PSCAD/EMTDC simulation outcome are demonstrated to confirm the suggested structure has an excellent operation.**

Keywords—fundamental inverter; optimum; symmetric and asymmetric; cascaded structure

I. INTRODUCTION

In recent years, high-power medium-voltage multilevel inverters applications have been increased due to producing good output voltage harmonic spectrum and easy control. Multilevel inverters structures are used in some applications, including FACTS devices, HVDC transmissions, AC motors drives and active filters to overcome the voltage and current limitation on semiconductors switch [1]–[3].

Multilevel inverters are suitable for high-power applications due to good characteristic such as high-power generation, low voltage common-mod, better output harmonic waveforms and lower dv/dt. Other important advantages of multilevel inverters are reducing THD, losses; electromagnetic interference and the stress of power electronic switches [4,5].

Different structures have been presented for multilevel inverters. The neutral point diode clamped multilevel inverters, flying capacitors multilevel inverters and H-bridge cascaded multilevel inverters are part of the basic structures [6,7].

Cascaded H-bridge multilevel inverter is one of the most popular structures compared to other classical structures due to the use of lower number of power electronics devices for producing high number of voltage levels. The biggest advantages of the cascade H-bridge multilevel inverters are: [8,9]

1. Regular circuit structure due to the same structure of each cell.
2. No additional clamping diodes compared to the diode-clamped multilevel inverters.
3. No need to flying capacitors compared to flying capacitors multilevel inverters.
4. To produce the specified voltage levels need to lower number of power electronic devices in compared to classical multilevel inverters.

However despite all the advantages mentioned, the cascaded H-bridge multilevel inverter have disadvantages such as: voltage generation is independent to DC links in each cell, non-flexibility in increasing the output voltage range and high number of DC links and power switches for generating high number of voltage levels [10]–[12].

Recently, new cascaded multilevel inverters structure has been a topic of investigation by many researchers [13]–[17]. Although, researchers have made great efforts on multilevel inverter, it seems further research on multilevel inverter structures can still be done in order to define an optimal structure for increasing number of output voltage levels.

Therefore, in this research, firstly a new fundamental inverter for cascaded multilevel inverters is introduced, which reduces the number of switching elements and independent power supplies. Secondly, a cascaded inverter is suggested linked to *z* number series of fundamental inverter. Subsequently, three methods to define values of DC links are presented. To check the advantage and disadvantages of the suggested cascaded structure a comparison is made with traditional structures aspects of the number of switching elements and DC links. Lastly, to verify the performance of the inverter a single-phase 15-levels fundamental inverter is simulated in PSCAD/EMTDC environments.

II. SUGGESTED FUNDAMENTAL INVERTER

The suggested fundamental inverter is shown in Fig. 1. This circuit produces 15-levels (14 positive and negative and zero level) without none circuit in the output. This circuit has 8 switches and four DC links. The all of used switches are unidirectional. The used DC are (V_1, V_2, V_3 and V_4), the DC link V_4 has the same values with V_3 but all the remaining DC links have different values. The unidirectional switches are comprised of one IGBT and one reverse diode and can block voltage in one polarity and conduct current in both path.

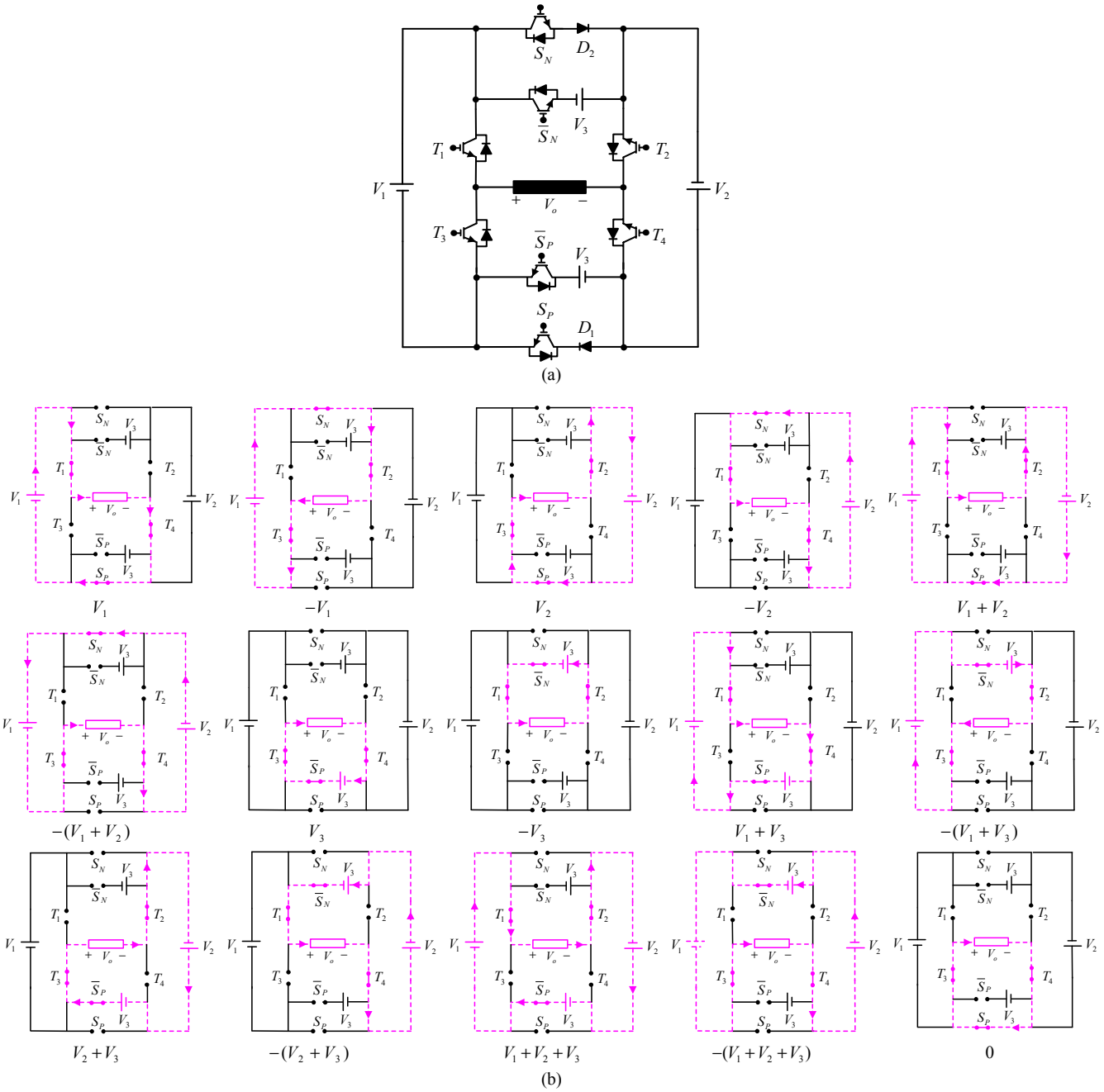


Fig. 1. (a) The suggested fundamental inverter; (b) different switching states

The switching pattern and produced output levels of the fundamental inverter are displayed in Table I. As shown in Table I, the switches of (S_P, $\overline{S}_P$), (S_N, $\overline{S}_N$) utilized to create of positive and negative levels, respectively. Also, the switches of (T_1, T_4) and (T_2, T_3) must turn on in a complementary mode to avoid the short circuit of respective DC links.

III. SUGGESTED CASCADED DESIGN

If the values of the DC links are equally considered, the fundamental inverter can create seven levels at its end. Therefore, to get maximum levels at the output, the values of DC links must be choosing differently. Hence, by connecting the *Z* number of the fundamental circuit inverter it creates a new cascaded structure. Fig. 3 shows the cascaded structure. The number of elements such as switches, IGBTs, driver circuits and DC link for cascaded structure are calculated as follows, respectively:

$$N_{switch} = N_{driver} = N_{IGBT} = 8z \quad (1)$$

$$N_{DC\,link} = 4z \quad (2)$$

In a cascaded structure, the number and the maximum amplitude of the generated output levels rely directly on the values of DC links.

TABLE I. THE OUTPUT LEVELS OF 15-LEVEL INVERTER

No.	T_1	T_2	T_3	T_4	S_P	S_N	V_o
1	on	off	off	on	on	off	V_1
2	off	on	on	off	off	on	$-V_1$
3	off	on	on	off	on	off	V_2
4	on	off	off	on	off	on	$-V_2$
5	on	on	off	off	on	off	V_1+V_2
6	off	off	on	on	off	off	$-(V_1+V_2)$
7	off	off	on	on	off	off	V_3
8	on	on	off	off	off	off	$-V_3$
9	on	off	off	on	off	off	V_1+V_3
10	off	on	on	off	off	off	$-(V_1+V_3)$
11	off	on	on	off	off	off	V_2+V_3
12	on	off	off	on	off	off	$-(V_2+V_3)$
13	on	on	off	off	off	off	$V_1+V_2+V_3$
14	off	off	on	on	off	off	$-(V_1+V_2+V_3)$
15	off	off	on	on	on	off	0
	on	on	off	off	off	on	

Therefore, three methods to determine the value of the DC links are suggested in order to generate total voltage levels

A. First method

In first method, the values of total DC links are considered equally. As seen as follows:

$$V_{1,j} = V_{2,j} = V_{dc} \qquad j = 1, 2, \cdots, z \tag{3}$$

In this condition, the maximum magnitude of output dc voltage ($V_{o,max}$), the number of generated output levels (N_{level}) and the variety of the value of DC links ($N_{variety}$) are obtained as follows:

$$V_{o,max} = \sum_{j=1}^{z} (V_{1,j} + V_{2,j} + V_{3,j}) = 3zV_{dc} \tag{4}$$

$$N_{level} = 6z + 1 \tag{5}$$

$$N_{variety} = 1 \tag{6}$$

B. Second Method

In the second method, the magnitudes of DC links in each fundamental suggested inverter are no equal. In other word the DC links of each fundamental inverter have three different values which are considered as follows:

First Fundamental Multilevel Inverter:

$$V_{1,1} = V_{dc} \tag{7}$$

$$V_{2,1} = 2V_{1,1} = 2V_{dc} \tag{8}$$

$$V_{3,1} = 3V_{1,1} = 3V_{dc} \tag{9}$$

Second Fundamental Multilevel Inverter:

$$V_{1,2} = 13\ V_{1,1} = 13\ V_{dc} \tag{10}$$

$$V_{2,2} = 13\ V_{2,1} = 26\ V_{dc} \tag{11}$$

$$V_{3,2} = 13\ V_{3,1} = 39\ V_{dc} \tag{12}$$

$\vdots$

j^{th} Fundamental Multilevel Inverter:

$$V_{1,j} = (13^{j-1})V_{1,1} \qquad j = 2, 3, \cdots, z \tag{13}$$

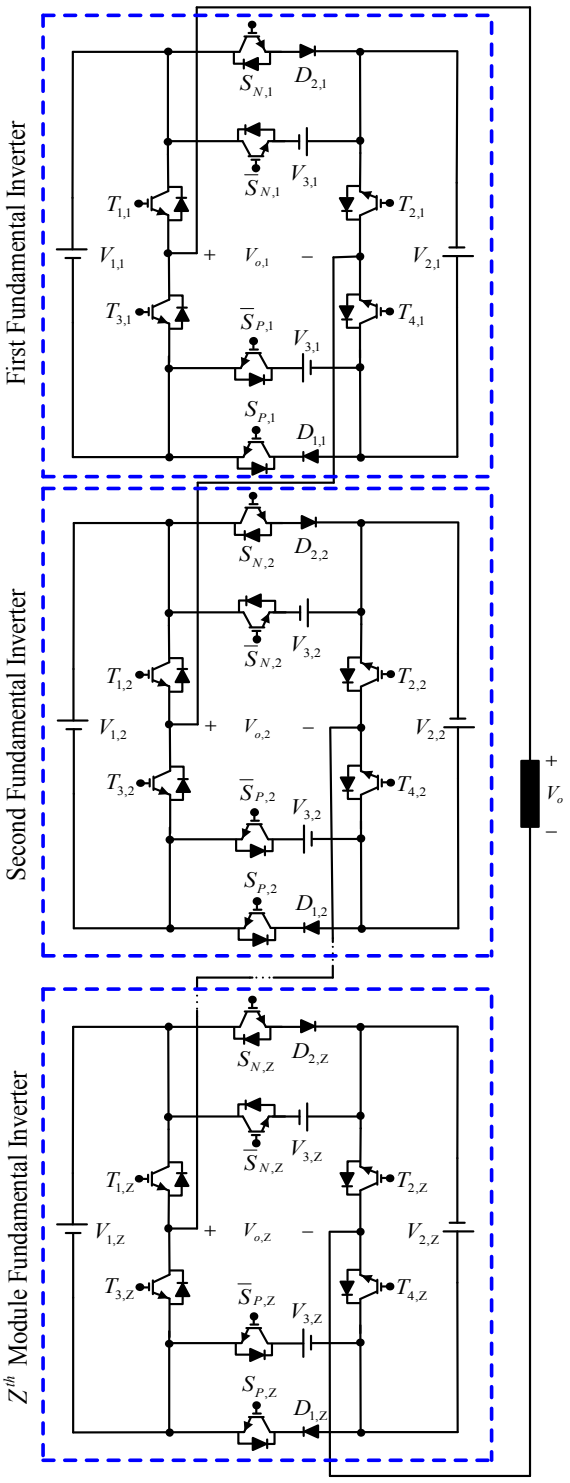


Fig. 2. The cascade arrangement based on fundamental inverter

$$V_{2,j} = (13^{j-1})V_{2,1} \qquad j = 2, 3, \cdots, z \tag{14}$$

$$V_{3,j} = (13^{j-1})V_{3,1} \qquad j = 2, 3, \cdots, z \tag{15}$$

For this method, the maximum magnitude of output voltage, the number of levels, and the variety of the value of DC links are obtained as follows:

$$V_{o,max} = \sum_{j=1}^{z} (V_{1,j} + V_{2,j} + V_{3,j}) V_{dc} = \frac{1}{2}(13^z - 1) V_{dc} \quad (16)$$

$$N_{level} = 13^z \quad (17)$$

$$N_{variety} = 3z \quad (18)$$

C. Third Method

In the second method, the magnitudes of the used DC links in the suggested cascaded structure are selected as follows:

First Fundamental Multilevel Inverter:

$$V_{1,1} = V_{dc} \quad (19)$$

$$V_{2,1} = 2\,V_{1,1} = 2V_{dc} \quad (20)$$

$$V_{3,1} = 4\,V_{1,1} = 4V_{dc} \quad (21)$$

Second Fundamental Multilevel Inverter:

$$V_{1,2} = 15\ V_{1,1} = 15\ V_{dc} \quad (22)$$

$$V_{2,2} = 15\ V_{2,1} = 30\ V_{dc} \quad (23)$$

$$V_{3,2} = 15\ V_{3,1} = 60\ V_{dc} \quad (24)$$

$\vdots$

j^{th} **Fundamental Multilevel Inverter:**

$$V_{1,j} = (15^{j-1})\,V_{1,1} \qquad j = 2,3,\cdots,z \quad (25)$$

$$V_{2,j} = (15^{j-1})\,V_{2,1} \qquad j = 2,3,\cdots,z \quad (26)$$

$$V_{3,j} = (15^{j-1})\,V_{3,1} \qquad j = 2,3,\cdots,z \quad (27)$$

For this method, the maximum magnitude of output voltage, the number of levels, and the variety of the value of DC links are obtained as follows:

$$V_{o,max} = \sum_{j=1}^{z} (V_{1,j} + V_{2,j} + V_{3,j}) V_{dc} = \frac{1}{2}(15^z - 1) V_{dc} \quad (16)$$

$$N_{level} = 15^z \quad (17)$$

$$N_{variety} = 3z \quad (18)$$

It is clear that the suggested asymmetric cascaded multilevel of this inverter with respect to the DC links have different magnitudes. It is also obvious that the number of generated output levels in the asymmetric states is higher than symmetric ones. However, the number of used power switches, IGBTs, diodes, driver circuits and DC links are the same as in the symmetric state.

IV. COMPARING THE SUGGESTED STRUCTURE WITH CONVENTIONAL STRUCTURES

To show the benefits of the suggested structure three algorithms is compared with other structures in [8], [15]–[17]. For this comparison, a classical CHB [8] and presented structure (FBMLI) [15], two methods of determined of magnitudes of DC links for symmetric and asymmetric states are selected. For the presented structure (DCHB) [16], three methods and for E-TYPE structure [17] an asymmetric state for magnitude of DC links is considered. Table II and Table III shows the number of switching elements and DC links based on their methods for all cascaded structures.

Fig. 3(a) compares the number of switches in four structures and the suggested structure. This figure proves that the suggested structure based on the third method can generate higher number of voltage levels with the same number of switches compared to the four structures. As mentioned in section I, the number of drivers and IGBTs have the same number of switches; however theses terms have other advantages than the suggested structures. Considering the E-type structure [17], this structure only uses bidirectional switches and requires two IGBT for each power switches due to this reason, the results of the comparison shows that the number of IGBT structures is highly similar to the number of switches.

Fig. 3(b) shows the results of the comparison between the number of DC links and its suggested structure and four other structures. According to this figure, the suggested cascaded structure creates high number of voltage levels compared to other cascaded structures, excepting R4. Likewise, these structures create less number of voltage levels than the suggested structure using the same number of DC links.

The variety of magnitudes of the DC links is another important factor in this comparison because when this factor rises the cost of the inverter will increase. The comparison of this factor and the number of levels in the suggested structure and other structures is shown in Fig.3 (c).

According to this figure, in the symmetric case, this factor is the same in all of the structures and all of the other four cascaded structures.

In the asymmetric case, the suggested structure creates high number of output voltage levels along with decreasing the variety of DC links compared to the four other cascaded structures expecting the structures in R6, R7. However, these structures generate less number of voltage levels than the four other structures exposed with the same number of switches, IGBT and DC links.

This research presented fundamental multilevel inverter in three states extension among them second method is more practical for industrial. Although presented fundamental multilevel inverter with third method, CHB with binary method and extend H-bridge [16] are satisfied mathematically and complexity in practical applications

TABLE II. PRESENTED METHODS FOR OTHER STRUCTURES

Structures	Methods	Magnitudes of DC links for j=1,2,…,n
CHB [8]	R_1	$V_1=V_2=\cdots=V_j=V_{dc}$
	R_2	$V_j = 2^{j-1}\ V_{dc}$
(FBMLI) [15]	R_3	$V_{1,j}=V_{2,j}=V_{3,j}=V_{dc}$
	R_4	$V_{1,1}=V_{2,1}=V_{dc}$, $V_{1,j}=V_{2,j}= 2V_{dc}$
(DCHB) [16]	R_5	$V_{R,j}=V_{L,j}=V_{dc}$
	R_6	$V_{R,1}=V_{L,1}=V_{dc}$, $V_{R,j}=V_{L,j}= 3^{j-1}\ V_{dc}$
	R_7	$V_{R,j}=V_{L,j}=V_{dc}$, $V_{R,j}=0.5V_{L,j}= 2^{j-1}\ V_{dc}$
(E-TYPE) [17]	R_8	$V_{1,j}=V_{dc}$, $V_{2,j}= 2V_{dc}$

TABLE III. ELEMENTS REQUIREMENTS FOR SUGGESTED STRUCTURE AND OTHER STRUCTURES BASED ON THEIR MAGNITUDES OF DC LINKS

Structures	CHB [8]		(FBMLI) [15]		(DCHB) [16]		(E-TYPE) [17]
Methods	**R_1**	**R_2**	**R_3**	**R_4**	**R_6**	**R_7**	**R_8**
N_{switch}	$2(N_{level}-1)$	$4[(\ln(N_{level}+1)/\ln 2)-1]$	$3(N_{level}-1)/2$	$3[\ln(N_{level}+1)/\ln 2]-3$	$6[(\ln(N_{level}+1/2)/\ln 3]$	$6[(\ln(N_{level}+7/3)/\ln 2]-6$	$3(N_{level}-1)/2$
N_{IGBT}	$2(N_{level}-1)$	$4[(\ln(N_{level}+1)/\ln 2)-1]$	$3(N_{level}-1)/2$	$3[\ln(N_{level}+1)/\ln 2]-3$	$6[(\ln(N_{level}+1/2)/\ln 3]$	$6[(\ln(N_{level}+7/3)/\ln 2]-6$	$(N_{level}-1)/2$
$N_{DC\text{-}link}$	$(N_{level}-1)/2$	$[\ln(N_{level}+1)/\ln 2]-1$	$(N_{level}-1)/2$	$[\ln(N_{level}+1)/\ln 2]-1$	$2[(\ln(N_{level}+1/2)/\ln 3]$	$2[(\ln(N_{level}+7/3)/\ln 2]-2$	$(N_{level}-1)/3$
$N_{variety}$	1	$[\ln(N_{level}+1)/\ln 2]-1$	1	$[\ln(N_{level}+1)/\ln 2]-1$	$[(\ln(N_{level}+1/2)/\ln 3]$	$[(\ln(N_{level}+7/3)/\ln 2]-1$	$(N_{level}-1)/6$

*The method of R_5 for [16] is equal to R_3.

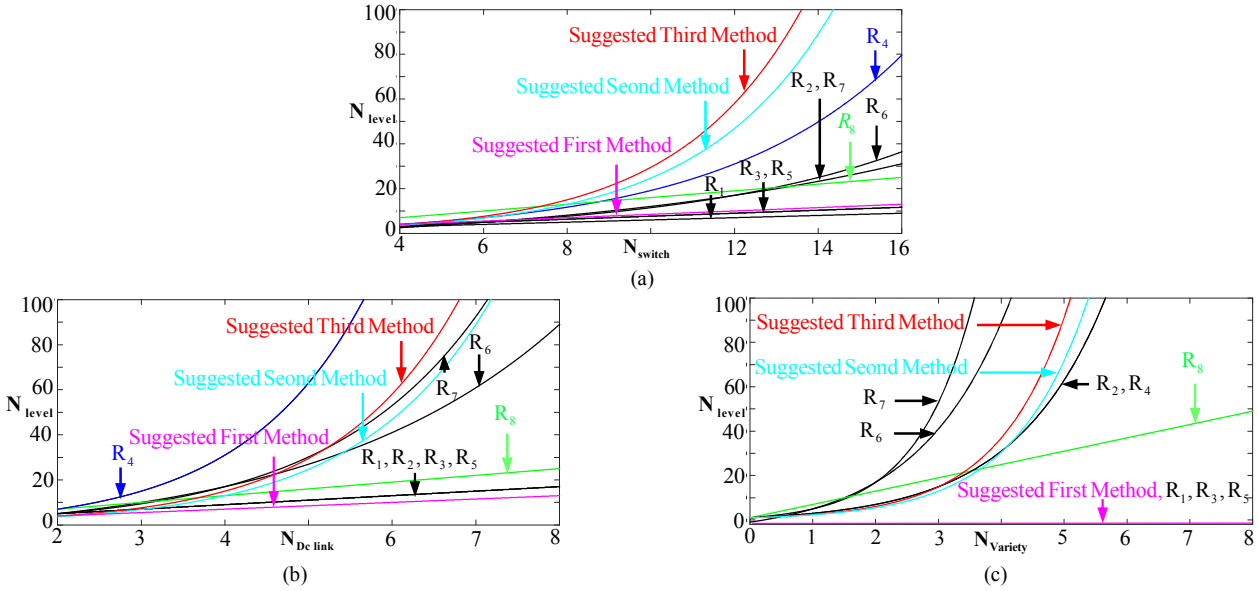


Fig. 3. (a) Curve of N_{switch} against N_{level}; (b) variation of N_{DC} links against N_{level}; (c) variation of $N_{variety}$ against N_{level}.

V. SIMULATION RESULTS

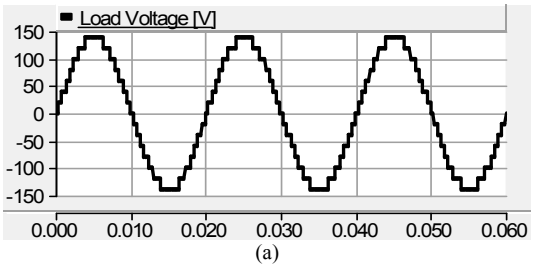
To verify the performance of the fundamental suggested inverter, a single phase 15-levels inverter has been simulated by PSCAD/EMTDC software for R-L load with R=90Ω, L=20mH. In this simulation, all of the power switches and diodes are assumed ideal. The fundamental frequency of output voltage is 50Hz. Fundamental frequency switching control method to generate gate switching pulses have been used. In this method the referenced sinusoidal waveform is compared to the DC levels. This method reduced switching losses since it used low switching frequency [18]–[19].

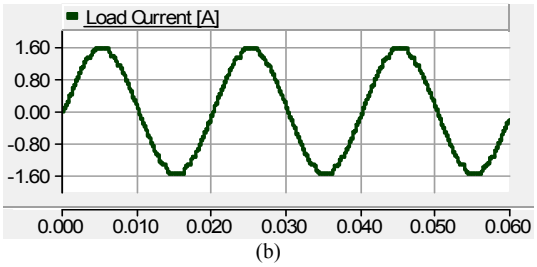
To achieve maximum output voltage of 140V, the values of DC links are determined based on the third method. With respect to Table II, the value of DC links are V1=20V, V2=40V and V3=80V.

The voltage and current output waveforms are shown Figs. 4(a) and (b) show, respectively. Fig. 4(a) shows that the suggested structure is able to produce fifteen level with the values of 0, ±20, ±40, ±60 ±80 ±100 ±120 and ±140V at its final stage. The maximum amplitude of current is 1.6 A.

Figs. 4(a) and (b) make evident that the output voltage and current is highly close to sinusoidal waveforms. By comparing Figs 4(a) and (b) it is clear that, there is a phase shift between them that is due to the inductive characteristic of the output load. Figs. 4(c) and (d) show harmonic spectra of output voltage and THD amplitude of output voltage.

The value of THD voltage is 3.67%. Figs. 4(e) and (f) show harmonic spectra of output current and THD amplitude of output current. The value of THD current is 2.50%.





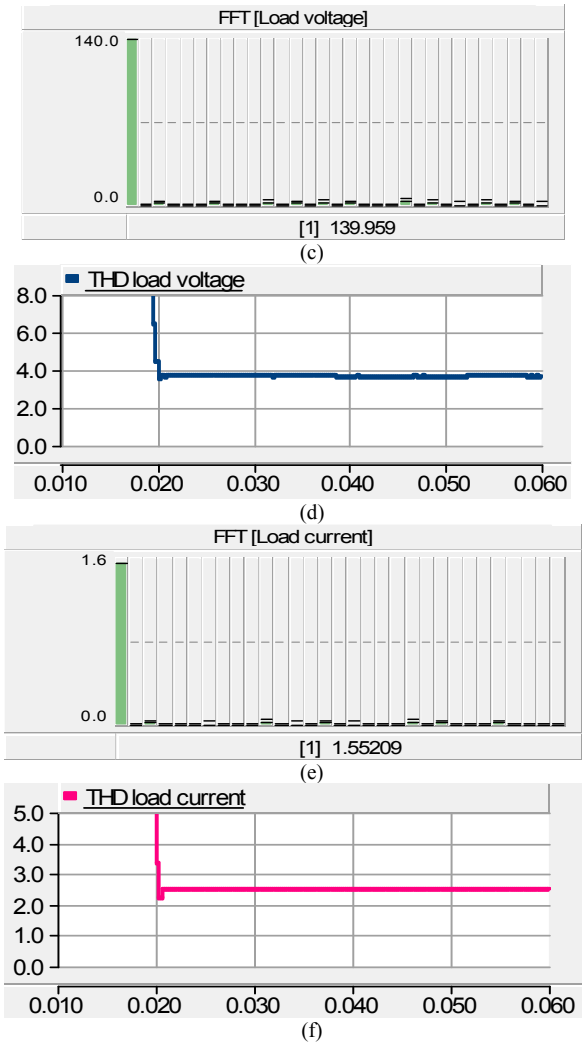


Fig.4. (a) output voltage waveform; (b); output current waveform;(c) harmonic spectra of output voltage;(d) load voltage total harmonic distortion (THD= %3.67); (e) harmonic spectra of output current; (f) load current total harmonic distortion (THD= %2.5)

VI. CONCLUSION

The fundamental 15-levels inverter is a new inverter structure for the cascaded multilevel inverters. The main advantage of this structure was the generating of maximum levels by using minimum number of elements such as switch, drivers and IGBTs. In order to achieve maximum voltage level which leads to lower THD in the output voltage, three methods to determine the magnitude of DC links have been suggested. The suggested cascaded inverter has compared with other cascaded structure in term of switching elements and DC links. In conclusion, to verify and approve of representation fundamental inverter, the results of simulation have been carrying out on a single phase 15- levels inverter.

ACKNOWLEDGMENTS

The authors would like to thank the financial support of FONDECYT Regular 1160690 Research Project, FONDECYT Postdoctoral 3170014 Research Project and Newton Picarte Project EPSRC: EP/N004043/1: New Configurations of Power Converters for Grid Interconnection Systems/CONICYT DPI20140007.

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