# Modeling, Analysis and Implementation of High Voltage Low Power Flyback Converter Feeding Resistive Loads

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***Abstract*—In High Voltage Flyback converters, the dominant factor that influences a converter operation is the parasitic capacitance. A significant portion of input energy is utilised in charging the parasitic capacitances of the circuit, which is circulated back to the source at the end of every switching cycle. The circulating energy is a function of output voltage, load power and parasitic capacitances and remain significant in High Voltage Low Power (HVLP) applications. This energy transfer phenomena involving parasitic capacitances results in reduced fraction of input energy reaching the load in every cycle, thereby resulting in an apparent deviation in converter operating point compared to ideal flyback in case of resistive loads. An analytical energy based model is derived including the effect of parasitic capacitances, valid for steady state and dynamics of High Voltage Low Power (HVLP) flyback converters feeding resistive loads. The influence of parasitic capacitances on switch voltage of the converter is exploited to achieve Zero Voltage Switching (ZVS) thereby minimising the turn on loss. The proposed analytical model is verified through simulation and experimental results on 1.5 kV / 5 W and 1.5 kV / 200 mW resistive load.**

***Index Terms*—High Voltage, Flyback, Voltage Gain, Resonance, Transformer Parasitics, Resistive Loads, Zero Voltage Switching (ZVS)**

## I. Introduction

High Voltage Power Supply encompass a broad application spectra such as analytical instruments for spectroscopy and electrophoresis, ion mass analyzers, smart material based actuators etc [1]–[4]. Analytical instruments like ion mass analyzer perform study and characterization of ions for space instrumentation systems. Such instruments comprise of electrostatic ion detector and deflector plates. The ion detector requires voltage in the range of 1.5 - 3 kV to scan and focus ions of specific energy level and is electrically modeled as a resistive load of 20 - 50 MΩ [2]. Analytical instrument employed in ozone generation require voltage in the range of 1 - 3 kV and is electrically modeled as resistive load (375 - 700 kΩ) [3]. Such devices are battery fed, operates with low power (typically in the range of 200 mW - 5 W) and need light weight high power density intermediate processing systems. A constant regulated output voltage with lower steady state ripple is required for effective operation of instruments modeled as resistive loads.

To cater such requirements, numerous topologies each with distinct advantages and disadvantages are proposed in literature [5]. Flyback converters have been widely used because of their relative simplicity and their performance for power rating less than 100 W [6]. Some constructive features of the flyback converter include: isolation between the source and load side, requires a capacitive filter on the HV side, compact with low component count.

Transfer of energy from source to load in a flyback converter occurs by energy storage in an intermediate flyback transformer. In HVLP flyback converters for the above applications feeding resistive loads, flyback transformers are designed with larger secondary turns and hence leads to higher self capacitance of transformer winding [7]–[9].

In general, the presence of parasitics impose a deviating behaviour in converter's operation, in comparison with the ideal characteristic. In a flyback converter specific to HVLP applications, the primary requirement of achieving the desired steady state gain is itself restricted by the parasitic capacitances [10]. A significant energy exchange occurs between parasitic capacitance ($C_{eff}$) and magnetising inductance ($L_m$) resulting in notable transition intervals apart from the typical intervals of an ideal flyback converter [11].

Converter's operation is categorized as Continuous (CCM) or Discontinuous (DCM) based on the variations of the load. CCM operation is also known as incomplete energy transfer mode since a part of the energy drawn from the source is retained by the flyback transformer. CCM for flyback converters specific to HVLP applications poses semiconductors with higher voltage stress and results in an inefficient hard switching process. The presence of a high turns ratio transformer results in high effective capacitance ($C_{eff}$) across drain to source of the primary active switch; this results in a significant amount of energy loss at the turn on instant of the active switch. Therefore the switching loss of the converter dominate the conduction loss.

DCM operation is known as complete energy transfer mode since no energy is retained by the transformer. In DCM operation, the parasitic capacitance present in the circuit resonates with magnetizing inductance and results in low frequency resonant intervals in addition to the MOSFET

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and diode conduction interval of an ideal flyback converter. Also, DCM with fixed frequency operation results in low and high gain oscillating instants of turn on in DCM idle period until the energy in the magnetising inductance ($L_m$) completely decays to zero; consequently, the converter turns on at unpredicted instants of oscillation leading to dramatic variations in the converter steady state gain [12].

Such a phenomena gained research attention and further works on modeling & control strategies of flyback converter for HVLP applications feeding resistive loads considering the parasitic capacitances is evolving in literature. Circuit based mode equations of HV flyback converter operating in discontinuous and critical conduction mode including the parasitic capacitance effect is presented in [13]–[15].

Research on efficiency optimisation for HVLP applications reveal that the major loss in converter operation is the switch node capacitance loss [16]- [17] and is addressed by variable frequency Quasi-Resonant (QR) mode of operation which exploits the converter behaviour and turns the active switch on with Zero Voltage Switching (ZVS turn-on) [18]. A look up table based online efficiency optimisation approach of a 65 W flyback converter prototype is presented in [17].

Implementing ideal steady state model of flyback converter ignores the effect of parasitic capacitances and hence inaccurately predicts the HVLP flyback converter operating point. Ideal steady state converter model provides an underestimate of input energy required to attain a desired output voltage ignoring the parasitic capacitance effect. Interpreting the input energy requirement, hence $I_{pk}$ from circuit mode equations involves mathematically intensive procedure and is not straightforward.

In this work, an expression for steady state voltage gain of a HVLP flyback converter with the parasitic capacitances included, driving a low power resistive load is presented [19]. An energy based steady state model along with the dynamic model which offers an expression for output voltage ($\hat{v_o}$) to control current ($\hat{i_c}$) transfer function is derived to implement a compensator based control scheme for achieving steady state voltage regulation targeting resistive loads.

A two loop control scheme with peak current defined by the outer loop, ZVS turn-on instant & Peak Current Mode Control (PCMC) turn-off instant decided by the inner loop is incorporated to ensure constant energy modulation considering low power resistive loads. The proposed energy based model is verified on a experimental prototype of HVLP flyback converter feeding 1500 V / 5 W and 1500 V / 200 mW resistive loads.

The paper is organised as below. Following the introduction, section II presents the circuit based analysis of HVLP flyback converter, section III outlines the energy transfer phenomena in HVLP flyback converter, section IV presents the design and implementation of HVLP flyback converter. Section V verifies the model through analytical, simulation and experimental tests. Section VI summarises and concludes the paper.

## II. Modeling of High Voltage Low Power (HVLP) Flyback Converter - Circuit Based Analysis

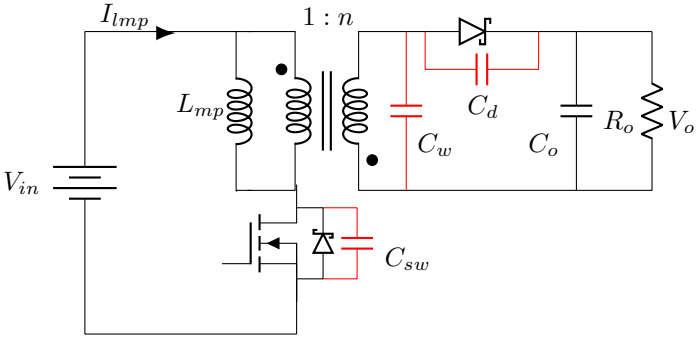


Fig. 1: Circuit diagram of HVLP flyback converter with parasitic capacitances included

Circuit model of HVLP flyback converter with parasitic capacitances namely the capacitance of the flyback transformer winding ($C_w$), MOSFET switch capacitance ($C_{sw}$), flyback diode capacitance ($C_d$) is shown in Fig. 1. The sinusoidal energy exchange between the magnetising inductance ($L_m$) and the net parasitic capacitance ($C_{eff}$) results in additional resonant intervals of resonant frequency $\omega$ apart from the typical intervals of an ideal flyback. The net parasitic capacitance referred to secondary of flyback transformer ($C_{seff}$) is the parallel equivalent of transformer winding capacitance ($C_w$), flyback diode capacitance ($C_d$), MOSFET capacitance ($C_{sw}$) and is defined by Eq.(1).

$$C_{seff} = C_{sw}/n^2 + C_w + C_d \tag{1}$$

$$\omega = \frac{1}{\sqrt{L_{ms} C_{seff}}} \tag{2}$$

The intervals of flyback converter operation with Quasi Resonant (QR) switching is explained in [15, 19]. A two loop control scheme where the MOSFET turn on with Zero Voltage Switching (ZVS turn-on) and turn off with peak current mode control (PCMC turn-off) decided by the inner loop is briefed in the following subsection. Equivalent circuit governing the individual modes and key waveforms of converter with two loop control scheme is presented in Fig. 2 and Fig. 3. Following are the assumptions considered in deriving the analytical model of HVLP Flyback converter.

1) In HVLP applications, the current flowing through the leakage inductance is lower, hence energy stored in magnetic field ($L_{lk}$) is lesser compared to energy stored in electric field ($C_{eff}$) [11, 20]. Thus, the dominant transformer parasitic that influences a HVLP converter operation is the winding capacitance which is included in analysis while the other transformer parasitics are neglected.
2) The semiconductor voltage drops and on state resistances are ignored while the switch and diode capacitances are retained.
3) The filter capacitor $C_o$ is choosen such that the series combination of $C_d$ and $C_o$, ($C_{S,eq}$) is approximately

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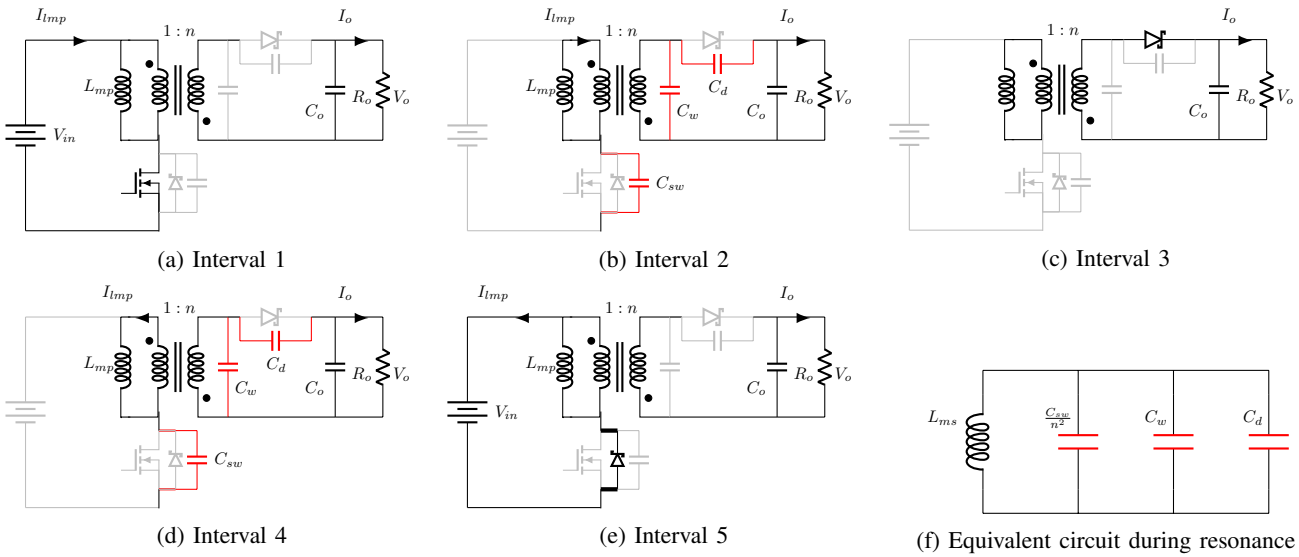


(a) Interval 1 (b) Interval 2 (c) Interval 3

(d) Interval 4 (e) Interval 5 (f) Equivalent circuit during resonance

Fig. 2: Equivalent circuit of HVLP flyback converter in various time intervals considering two loop control scheme.

TABLE I: Governing equations of HVLP flyback converter considering two loop control scheme

| Mode | Time Interval | Voltage across Mag.Inductance (Py.) | Current through Mag.Inductance (Py.) | Current through Filter Capacitor |
|---|---|---|---|---|
| Mode-1<br>(MOSFET Turn On) | $t_0 - t_1$<br>$T_{on} = \frac{L_{mp} I_{pk}}{V_{in}} + \frac{V_o}{nV_{in}} \frac{sin(\omega T_{res2})}{\omega}$ - $T_z$ | $V_{lmp}(t) = V_{in}$ | $I_{lmp}(t) = I_{init} + \frac{V_{in}}{L_{mp}} t$ | $I_c(t) = -I_o$ |
| Mode-2<br>(First Resonance Interval) | $t_1 - t_2$<br>$T_{res1} = \frac{1}{\omega}(cos^{-1}(\frac{-V_o}{nV_{in}} cos\phi) - \phi)$ | $V_{lmp}(t) = V_{max} cos(\omega(t-t_1)+\phi)$<br>$V_{max} = I_{max} Z_c$<br>$Z_c = \omega\ L_{mp}$ | $I_{lmp}(t) = I_{max} sin(\omega(t-t_1)+\phi)$<br>$\phi = tan^{-1}(\frac{I_{pk} Z_c}{V_{in}})$ | $I_c(t) = I_{max} \frac{C_d}{nC_{seff}}$<br>$sin(w(t-t_1)+\phi)$<br>$-I_o$ |
| Mode-3<br>(Diode-Conduction Interval) | $t_2 - t_3$<br>$T_d = \sqrt{\frac{2L_{ms}}{RF_s}}$ | $V_{lmp}(t) = \frac{-V_o}{n}$ | $I_{lmp} = \frac{I_{lmpTres1}}{n} \frac{(T_d - t)}{T_d}$ | $I_c(t) = \frac{I_{lmpTres1}}{n}$<br>$\frac{(T_d - t)}{T_d} - I_o$ |
| Mode-4<br>(Second Resonance Interval) | $t_3 - t_4$<br>$T_{res2} = \frac{1}{\omega}(\pi - cos^{-1}(\frac{nV_{in}}{V_o}))$ | $V_{lmp}(t) = \frac{-V_o cos(\omega(t-t_3))}{n}$ | $I_{lmp}(t) = \frac{-V_o sin(\omega(t-t_3))}{n\omega L_{mp}}$ | $I_c(t) = \frac{-V_o}{n^2 Z_c} \frac{C_d}{C_{seff}}$<br>$sin(w(t-t_3)) - I_o$ |
| Mode-5<br>(Body Diode Conduction) | $t_4 - t_5$<br>$T_z = cos^{-1}(\frac{nV_{in}}{V_o})$ | $V_{lmp}(t) = V_{in}$ | $I_{lmp}(t) = I_{lmpTres2} + \frac{V_{in}(t-t_4)}{L_{mp}}$ | $I_c(t) = -I_o$ |

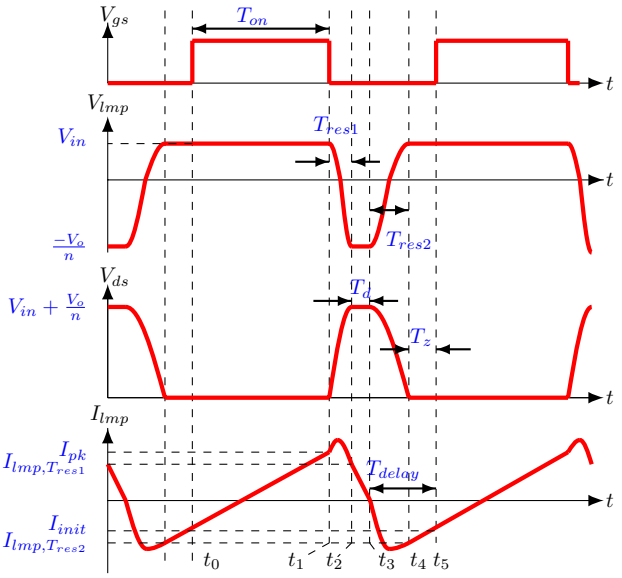


Fig. 3: Key waveforms of HVLP flyback converter including the effect of parasitic capacitances considering two loop control scheme

equals to $C_d$ while the parallel combination of $C_w$ and $C_o$, ($C_{P,eq}$) approximately results in $C_o$.

$$C_{S,eq} = \frac{C_d C_o}{C_d + C_o} \approx C_d \tag{3}$$

$$C_{P,eq} = C_o + C_w \approx C_o \tag{4}$$

This ensures the filter capacitance and load do not affect the resonating intervals.

4) Converter is in steady state with the output voltage $V_o >$ n $V_{in}$.

### A. Operating Principle

HVLP flyback converter operation features the typical MOSFET and flyback diode conduction interval along with two additional resonant intervals. The analytical equations governing each interval is presented in Table.(I).

**Interval 1** ($t_0$ - $t_1$) MOSFET conduction interval ($T_{on}$)

**Initial conditions**: $V_{lmp}(t_0)$ = $V_{in}$ ; $I_{lmp}(t_0)$ = $I_{init}$

MOSFET switch is turned on at t = $t_0$, with ZVS. The magnetising current $I_{lmp}$ linearly ramps up with a slope given by $\frac{V_{in}}{L_{mp}}$. There exists a negative initial current ($I_{init}$) as observed from Fig. 3. This results in additional on time $T_{on}$ of the MOSFET unlike the ideal flyback. The

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controller detecting $I_{lmp}$ = $I_{pk}$ where $I_{pk}$ is the reference peak current, turns off the MOSFET.

**Interval 2 ($t_1$ - $t_2$)** First resonance interval ($T_{res1}$)

**Initial conditions**: $V_{lmp}(t_1)$ = $V_{in}$ ; $I_{lmp}(t_1)$ = $I_{pk}$

During this interval, some portion of magnetising energy stored in the flyback inductor during interval 1 is utilised in charging the equivalent parasitic capacitance ($C_{seff}$) from -$nV_{in}$ to $V_o$. This forms the portion of parasitic circulating energy ($E_{par}$) and reduces the energy available to the load during diode conduction. A small portion of magnetising current $i_c(t)$ flows through the diode capacitance ($C_d$) and charges the filter capacitance ($C_o$).

**Interval 3 ($t_2$ - $t_3$)** Diode conduction interval ($T_d$)

**Initial conditions**: $V_{lmp}(t_2)$ = $\frac{-V_o}{n}$ ; $I_{lmp}(t_2)$ = $\frac{I_{lmp,Tres1}}{n}$

Voltage across the parasitic capacitance ($C_{seff}$) is clamped to $V_o$. This mode is similar to the discharging mode in an ideal flyback converter except that the initial current for the mode is not $\frac{I_{lmp}}{n}$ but $I_{lms,Tres1} = \frac{I_{max}sin(wT_{res1}+\phi)}{n}$.

**Interval 4** ($t_3$ - $t_4$) Second resonance interval ($T_{res2}$)

**Initial conditions**: $V_{lmp}(t_3)$ = $\frac{-V_o}{n}$ ; $I_{lmp}(t_3)$ = 0

The voltage across the parasitic capacitance ($C_{seff}$) discharges from $V_o$ to $-nV_{in}$, thereby transferring the circulating energy (utilised by the parasitic capacitances during the first resonance interval) to the magnetising inductance ($L_{mp}$). At the end of interval 4, voltage across the magnetising inductance ($L_{mp}$) is clamped to $V_{in}$ and initiates the body diode of MOSFET to conduct.

**Interval 5 ($t_4$ - $t_5$)** Body diode conduction interval ($T_z$)

**Initial conditions**: $V_{lmp}(t_4)$ = $V_{in}$ ; $I_{lmp}(t_4)$ = $I_{lmp,Tres2}$

During this interval, the circulating energy stored in the magnetising inductance ($L_{mp}$) is delivered to the source through body diode conduction.

A constant programmed delay of $T_{delay}$ = $\frac{\pi}{\omega}$ post the diode conduction interval marks the end of a switching cycle, defines the turn-on instant (ZVS turn-on) of MOSFET for subsequent cycle.

### *B. Analysis and Observation*

The instruments that require high voltage in the range of 1-3 kV is presented along with their equivalent electrical model in Table.II. Analysis and operating principles of HVLP flyback converter are tested on low power resistive loads namely Ozoniser (1.5 kV / 5 W) and Ion detector (1.5 kV / 200 mW).

TABLE II: Equivalent electrical model and parameters of applications fed from the HVLP flyback converter

| Test Cases | Applications | Equivalent Model under testing |
|---|---|---|
| Case 1 | **Ozonisers** [3]<br>Electrostatic precipitators<br>Mass spectroscopy [1] | Resistive Load<br>$R_o$ : 546 kΩ |
| Case 2 | **Ion detectors** [2]<br>Image intensifiers<br>Piezo devices [4] | Resistive Load<br>$R_o$ : 20 MΩ |

A typical design of HV flyback transformer shown in Table.III is considered to study the influence of parasitic capacitance in HVLP application.

TABLE III: Flyback converter specifications considered for analysis

| Parameter | Value |
|---|---|
| Magnetising inductance referred to Primary/Secondary ($L_{mp}/L_{ms}$) | 25.52 $\mu$H / 7.37 mH |
| Turns ratio ($n$) | 17 |
| Self capacitance of HV winding ($C_w$) | 19 pF |
| Net parasitic capacitance referred to secondary ($C_{seff}$) | 26 pF |
| Input voltage ($V_{in}$) | 12 V |
| Reference peak current ($I_{pk}$) | 1 A |

Table.IV compares the key parameters of ideal and HVLP flyback considering $R_o$ : 546 kΩ and $R_o$ : 20 MΩ. Comparison of such parameters is worth investigating which leads to better understanding on the converter steady state and dynamic performances.

TABLE IV: Key parameters of ideal and HVLP flyback converter subjected to a input peak current $I_{pk}$ = 1 A feeding $R_o$ : 546 kΩ

| Parameters | Ideal Flyback | HVLP Flyback (Analytical) | HVLP Flyback (Simulation) |
|---|---|---|---|
| **Time Intervals** | | | |
| $T_{on}$ | 2.13 $\mu$s | 3.13 $\mu$s | 3.01 $\mu$s |
| $T_{res1}$ | 0 $\mu$s | 0.47 $\mu$s | 0.43$\mu$s |
| $T_d$ | 0.38 $\mu$s | 0.38 $\mu$s | 0.39$\mu$s |
| $T_{res2}$ | 0 $\mu$s | 0.82 $\mu$s | 0.82 $\mu$s |
| $T_z$ | 0 $\mu$s | 0.57 $\mu$s | 0.58 $\mu$s |
| **Magnetising Current** | | | |
| $I_{init}$ | 0 A | -0.47 A | -0.47 A |
| $I_{lmp,Tres1}$ ($I_{dp,pk}$) | 1 A | 0.66 A | 0.68 A |
| $I_{lmp,Tres2}$ | 0 A | -0.74 A | -0.72 A |
| **Output Voltage** | | | |
| $V_o$ | 1136.9 V | 756.7 V | 758.6 V |
| **Load Current** | | | |
| $I_o$ | 2.08 mA | 1.38 mA | 1.39 mA |

TABLE V: Key parameters of ideal and HVLP flyback converter subjected to a input peak current $I_{pk}$ = 1 A feeding $R_o$ : 20 MΩ.

| Parameters | Ideal Flyback | HVLP Flyback (Analytical) | HVLP Flyback (Simulation) |
|---|---|---|---|
| **Time Intervals** | | | |
| $T_{on}$ | 2.13 $\mu$s | 3.49 $\mu$s | 3.63 $\mu$s |
| $T_{res1}$ | 0 $\mu$s | 0.71 $\mu$s | 0.73 $\mu$s |
| $T_d$ | 0.065 $\mu$s | 0.064 $\mu$s | 0.064 $\mu$s |
| $T_{res2}$ | 0 $\mu$s | 0.79 $\mu$s | 0.79 $\mu$s |
| $T_z$ | 0 $\mu$s | 0.65 $\mu$s | 0.61 $\mu$s |
| **Magnetising Current** | | | |
| $I_{init}$ | 0 A | - 0.64 A | -0.70 A |
| $I_{lmp,Tres1}$ ($I_{dp,pk}$) | 1 A | 0.13 A | 0.14 A |
| $I_{lmp,Tres2}$ | 0 A | -0.96 A | -0.98 A |
| **Output Voltage** | | | |
| $V_o$ | 6.6 kV | 986 V | 986 V |
| **Load Current** | | | |
| $I_o$ | 0.33 mA | 0.05 mA | 0.05 mA |

Fig. 4, 5 presents the gate pulse ($V_{gs}$) and magnetising inductance current ($I_{lmp}$) profile of an ideal and HVLP flyback converter with $R_o$ : 546 kΩ and $R_o$ : 20 MΩ, subjected to input voltage $V_{in}$ = 12 V and $I_{pk}$ = 1 A.

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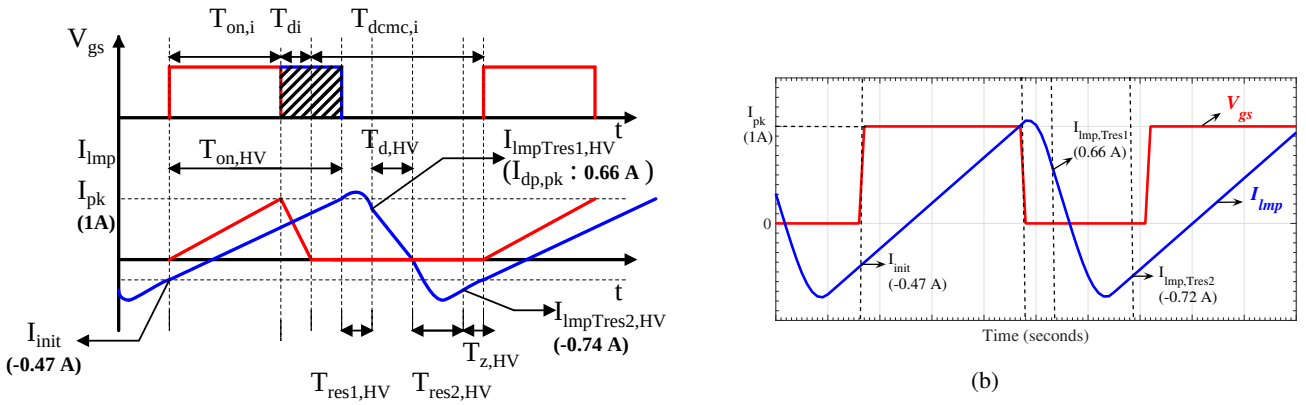


Fig. 4: a) Analytical waveform of magnetising inductance current ($I_{lmp}$) referred to primary side of ideal and HVLP flyback converter subjected to $I_{pk}$ = 1 A, considering $R_o$ : 546 kΩ b) Simulation waveform of magnetising inductance current ($I_{lmp}$) referred to primary side of HVLP flyback converter subjected to $I_{pk}$ = 1 A, considering $R_o$ : 546 kΩ

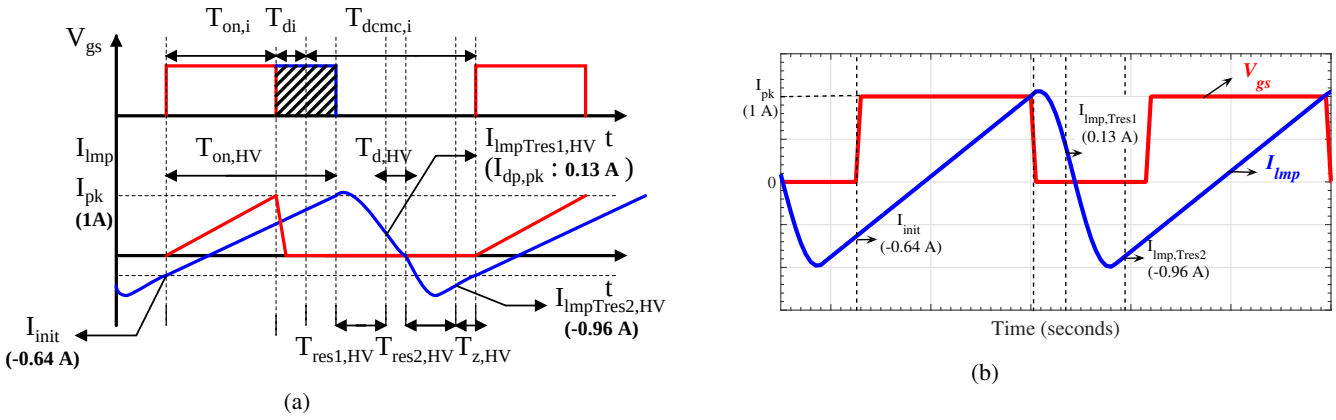


Fig. 5: a) Analytical waveform of magnetising inductance current ($I_{lmp}$) referred to primary side of ideal and HVLP flyback converter subjected to $I_{pk}$ = 1 A, considering $R_o$ : 20 MΩ b) Simulation waveform of magnetising inductance current ($I_{lmp}$) referred to primary side of HVLP flyback converter subjected to $I_{pk}$ = 1 A, considering $R_o$ : 20 MΩ

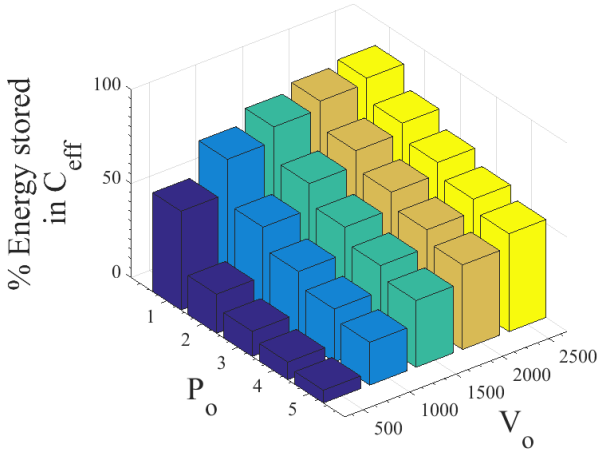


Fig. 6: % of energy stored in net parasitic capacitance $C_{eff}$ to the total energy as a function of output voltage ($V_o$) and output power ($P_o$)

1) A non-zero initial current ($I_{init}$) is carried by the magnetising inductance ($L_{mp}$) at the instant of turn on, which is a function of load voltage ($V_o$) and parasitic capacitance ($C_{eff}$), independent of loading condition ($R_o$). Such initial current observed is a characteristic of circulating energy (utilised in charging the parasitic capacitance during resonant intervals) and being fed back to the source through body diode conduction. Hence an increased $T_{on}$ is required to reach same $I_{pk}$ compared to ideal flyback.
2) In other words, considering on time predicted by ideal model results in reduced input energy drawn from the source, thereby resulting in reduced voltage in HVLP flyback converter operated with ZVS constant $T_{on}$ control.
3) A reduction in peak current carried by the diode ($I_{dp,pk}$ = $I_{lmp,Tres1}$) in comparison with the ideal, is observed which relates to the reduced average load current ($I_o$). The current carried by the diode capacitance ($C_d$) during resonance intervals is a fraction of circulating energy utilised in charging the parasitics.

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4) Fig. 6 presents the percentage of energy stored in $C_{eff}$, (circulating energy) as a function of output voltage ($V_o$) and output power ($P_o$). Steady state output voltage is swept between 500 - 2500 V and output power between 1-5 W. The portion of input energy is utilised in charging the parasitics increases as the output voltage increases and output power decreases. This affirms the dominant influence of parasitic capacitances in HVLP application.

Applying steady state voltage gain expression of ideal flyback which ignores the parasitic capacitances is inappropriate. A modified expression of steady state voltage gain with parasitic capacitance effect included is derived in the following subsection.

### C. Steady state voltage gain of HVLP flyback

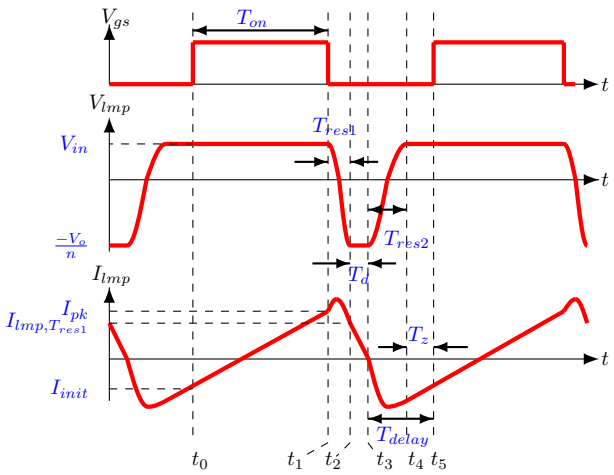


Fig. 7: Voltage across the primary magnetising inductance ($V_{lmp}$) and current carried by the primary magnetising inductance ($I_{lmp}$) in a HVLP flyback converter feeding resistive load

Fig. 7 presents the voltage across the primary magnetising inductance ($V_{lmp}$) and current carried by the primary magnetising inductance ($I_{lmp}$) in a HVLP flyback converter. The governing equations presented in Table.I are extended to steady state and applying volt-sec principle across the primary magnetising inductance gives,

$$V_{in}T_{on} + V_{max}\frac{sin(\omega T_{res1}+\phi)}{\omega} - V_{max}\frac{sin\phi}{\omega} - \frac{V_o}{n}T_d - \frac{V_o sin(\omega T_{res2})}{n\omega} = 0 \quad (5)$$

$$V_o = n\frac{V_{in}T_{on} + V_{in}T_z + V_{max}\frac{sin(\omega T_{res1}+\phi)}{\omega} - V_{max}\frac{sin\phi}{\omega}}{T_d + \frac{sin(\omega T_{res2})}{\omega}} \quad (6)$$

Eq. (6) can be rewritten as,

$$\frac{V_o}{V_{in}} = n\frac{D + D_z + \frac{sin(2\pi K D_{res1}+\phi)}{2\pi K cos\phi} - \frac{tan\phi}{2\pi K}}{D_2 + \frac{sin(2\pi K D_{res2})}{2\pi K}} \quad (7)$$

where, D = $\frac{T_{on}}{T_s}$; $D_z$ = $\frac{T_z}{T_s}$; $D_{res1}$ = $\frac{T_{res1}}{T_s}$; $D_{res2}$ = $\frac{T_{res2}}{T_s}$; $D_2$ = $\frac{T_d}{T_s}$; K = $\frac{\omega}{\omega_s}$. The time intervals $T_{on}$ - $Tz$ is computed by substituting initial & final values of current and voltage in mode equations presented in Table I. The expression for $T_{on}$ - $T_z$ in terms of circuit parameters namely $L_{mp}$, R, $\omega$, $V_{in}$, $F_s$, $V_o$ is defined in Table I.

The time intervals are function of output voltage which makes the voltage gain equation non-linear. Solution to these equations needs an iterative procedure and is solved using numerical analysis.

Substituting $D_{res1}$, $D_{res2}$, $D_z$ = 0 in Eq.(7) gives the steady state gain of the ideal flyback converter in DCM.

$$\frac{V_o}{V_{in}} = n\frac{D}{D_2} \quad (8)$$

A constant input peak current of 1 A is fed to ideal & HVLP flyback converter model and the steady state gain ($\frac{V_o}{V_{in}}$) & time taken to reach steady state is compared in Table.VI. A significant deviation is perceived in both the steady state gain & time taken to reach steady state in a HVLP flyback converter in comparison to ideal converter.

| **Load** | **Steady state gain** ($\frac{V_o}{V_{in}}$) | | **Time taken to reach steady state** | |
|---|---|---|---|---|
| | **Ideal** | **HVLP** | **Ideal** | **HVLP** |
| 546 kΩ | 94.9 | 63.3 | 34 ms | 13.06 ms |
| 20 MΩ | 552 | 82 | 1.25 s | 26.5 ms |

TABLE VI: Comparison of Ideal and HVLP steady state gain & time taken to reach steady state considering $I_{pk}$ = 1 A.

Though the analytical steady state expression derived based on the circuit mode equations is accurate, the circuit based model fails to provide physical insight on circulating energy involved in HVLP flyback converter. Interpreting the input energy requirement, hence $I_{pk}$ from circuit based equations involves mathematically intensive procedure and is not straightforward. An energy based model provides better insight on energy components of various passive elements of the converter and is more appropriate to predict the input peak current required to reach a desired output voltage ($V_o$).

## III. Energy Based Analysis

In an ideal flyback converter (without considering the parasitic capacitances), only energy intervals $E_1$ and $E_2$ exist.

**Energy storage phase** $E_1$ (MOSFET conduction interval $T_{on}$): Energy ($\Delta E_{mag}$) is drawn from the source and stored in $L_m$ in the form of electromagnetic energy.

**Energy delivery phase** $E_2$ (Diode conduction interval $T_d$): The stored electromagnetic energy ($\Delta E_{mag}$) charges the load capacitor ($\Delta E_{load}$).

Applying energy balance in an ideal flyback,

$$\Delta E_{mag} = \Delta E_{load}$$

$$E_{load} = E_{mag} = \frac{L_{mp}I_{pk}^2}{2} \quad (9)$$

However, it does not hold true in a HVLP flyback converter with the presence of parasitic capacitances.

Fig. 8 presents the HVLP flyback converter with energy

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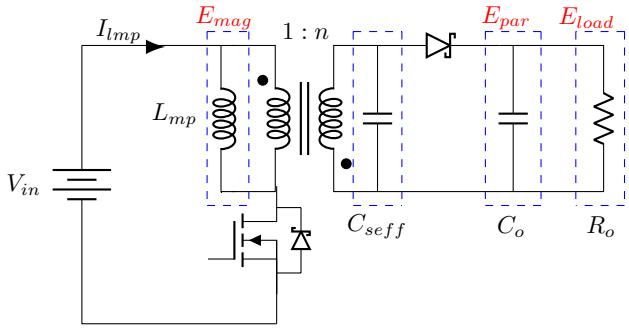


Fig. 8: Energy components associated with magnetising inductance ($L_{mp}$), parasitic capacitance ($C_{eff}$) and load ($R_o$) in a HVLP flyback converter

components of magnetising inductance ($L_m$), parasitic capacitance ($C_{eff}$), filter capacitor ($C_o$) and load resistance ($R_o$) defined.

A HVLP flyback converter operation consist of three energy intervals $E_1$, $E_2$, $E_3$ and two resonating intervals $R_1$ and $R_2$.

**Energy storage phase** $E_1$(MOSFET conduction interval $T_{on}$): Energy ($\Delta E_{mag}$) is drawn from the source and stored in $L_m$ in the form of electromagnetic energy.

**Resonating interval** $R_1$ (First resonance interval $T_{res1}$): A portion of input energy defined by $\Delta E_{par}$ is used in charging the parasitic capacitance $C_{seff}$ from -$nV_{in}$ to $V_o$. This reduces the energy stored in $L_m$ and is related to the fall in magnetising current ($I_{lmp,Tres1}$) as shown in Fig. 4-5.

**Energy delivery phase** $E_2$ (Diode conduction interval $T_d$): The remaining electromagnetic energy defined by ($\Delta E_{load}$) charges the filter capacitor ($C_o$) and the load resistor ($R_o$).

**Resonating interval** $R_2$ (Second resonance interval $T_{res2}$): The energy stored in the parasitic capacitances ($\Delta E_{par}$) is discharged to the magnetising inductance ($L_m$).

**Energy transfer phase** $E_3$ (Body diode conduction interval $T_z$): The energy stored in the magnetising inductance ($\Delta E_{par}$) is supplied back to the source through body diode conduction.

Applying energy balance in HVLP flyback converter,

$$\Delta E_{load} = \Delta E_{mag} - \Delta E_{par}$$

$$E_{load} = \frac{L_{mp} I_{pk}^2}{2} - \frac{C_{seff}(V_o^2 - n^2 V_{in}^2)}{2} \qquad (10)$$

Ideal flyback converter model (Eq.9) does not include the circulating energy component, hence provides a lower estimate of input energy ($E_{mag}$) required to reach a desired voltage.

A reference peak current of ($I_{pk}$ = 1A) corresponding to input energy ($E_1$) =12.76 $\mu$J is fed to a HVLP flyback converter with specifications presented in Table.III. The amount of energy delivered to the load resistances $R_o$ : 546 kΩ and 20 MΩ along with the circulating energy required to charge the parasitic capacitances is computed using Eq.(9, 10) and presented in Table.VII. Hence, implementing ideal flyback model (Eq.9) for a HVLP flyback converter results

TABLE VII: Energy delivered to the load resistance ($E_{load}$) and stoed in parasitic capacitances ($E_{par}$) in an ideal and HVLP flyback converter feeding resistive loads ($R_o$ : 546 kΩ and 20 MΩ)

| Load | Parameter | Ideal flyback | HVLP flyback |
|---|---|---|---|
| 546 kΩ | $E_{mag}$ | 12.76 $\mu$J | 12.76 $\mu$J |
| | $E_{par}$ | 0 | 7.02$\mu$J |
| | $E_{load}$ | 12.76 $\mu$J | 5.74 $\mu$J |
| | $V_o$ | 1136 V | 763 V |
| 20 MΩ | $E_{mag}$ | 12.76 $\mu$J | 12.76 $\mu$J |
| | $E_{par}$ | 0 | 12.73$\mu$J |
| | $E_{load}$ | 12.76 $\mu$J | 0.278$\mu$J |
| | $V_o$ | 6.62 kV | 979 V |

in incorrect prediction of $I_{pk}$ to attain desired output voltage ($V_o$).

Fig. 9,10 presents the analytical response of ideal and HVLP flyback converter considering ($R_o$ : 546 kΩ and 20 MΩ) subjected to $I_{pk}$ = 1A.

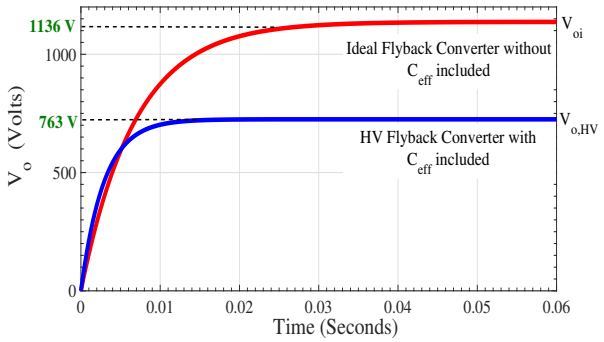


Fig. 9: Analytical output voltage of ideal and HVLP flyback converter feeding resistive load $R_o$: 546 kΩ subjected to $I_{pk}$ = 1 A

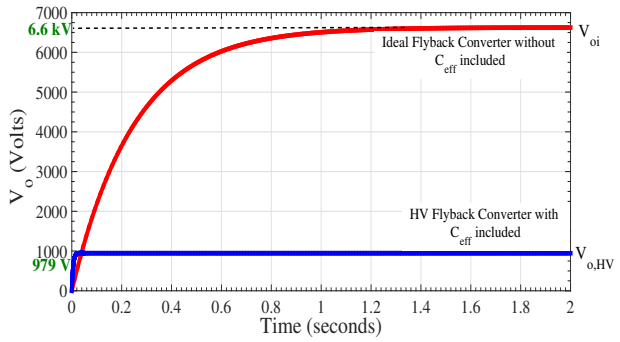


Fig. 10: Analytical output voltage of ideal and HVLP flyback converter feeding resistive load $R_o$: 20 MΩ subjected to $I_{pk}$ = 1 A

Considering a 546 kΩ resistive load, Eq.(9) predicts an output voltage $V_o$ = 1136 V ($E_{load}$ = 12.76$\mu$J) while the output voltage $V_o$ of HVLP flyback converter is limited to 763 V.

A significant difference in output voltage is observed in case of a 20 MΩ resistive load. 20 MΩ loading condition almost resembles a capacitive load. In an ideal flyback converter without parasitic capacitances, the voltage across the capacitive load charges to near infinity and the charging

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is limited only by the parasitic resistances of the converter. Hence 12.76 $\mu$J delivered to light load of 20 M$\Omega$ with filter capacitor value of 20 nF attains 6.6 kV. However the output voltage considering the parasitic capacitances is limited to 925 V owing to the restriction in charging the parasitic capacitances (-$nV_{in}$ to $V_o$) by the reference peak current (1 A). A major fraction of input energy ($E_{mag}$) circulates between the magnetising inductance ($L_m$) and parasitic capacitance ($C_{eff}$) without reaching the load.

### *A. Steady state peak current prediction in a HVLP flyback converter*

Eq.(10) is rewritten to compute the accurate steady state peak current requirement from the source to achieve $V_{ref}$.

$$I_{pri,pk} = \sqrt{\frac{C_{seff}}{L_{mp}}(V_{ref}^2 - n^2 {V_{in}}^2) + \frac{2V_{ref}^2}{RF_sL_{mp}}} \quad (11)$$

where $V_{ref}$ is the desired steady state output voltage.
In Eq.(11), the second term represents the fraction of input energy (in terms of peak current) demanded by the load in steady state while first term represents the circulating energy required in charging the parasitic capacitances from $-nV_{in}$ to $V_{ref}$.

$$I_{pri,pk} = \sqrt{I_{pk,par}^2 + I_{pk,load}^2} \quad (12)$$

From Eq.(11) & (12),

$$I_{pk,par} = \gamma I_{pk,load} \quad (13)$$

where,

$$\gamma = \sqrt{\frac{C_{seff}F_s(V_{ref}^2 - n^2V_{in}^2)}{2P_{load}}} \quad (14)$$

Eq.(14) defines the increment in the input peak current required to achieve the desired output voltage $V_{ref}$. The incremental factor ($\gamma$) defined is a function of parasitic capacitance ($C_{eff}$), switching frequency ($F_s$), load power ($P_o$). The individual components of peak current ($I_{pk,par}$ & $I_{pk,load}$) along with the net peak current $I_{pri,pk}$ required to achieve 1500 V considering 5 W and 200 mW resistive load is presented in Table.VIII.

TABLE VIII: Peak current $I_{pk}$ demanded by load $R_o$ and parasitic capacitances $C_{eff}$ in steady state considering 1500 V / 5 W and 1500 V / 200 mW resistive load

| Load | $I_{pk,par}$ | $I_{pk,load}$ | $I_{pri,pk}$ | $\gamma$ |
|---|---|---|---|---|
| 5 W | 1.499 A | 1.797 A | 2.340 A | 0.834 |
| 200 mW | 1.499 A | 0.2655 A | 1.522 A | 5.645 |

### *B. Small Signal Model of HV Flyback converter*

The small signal model of an ideal flyback converter in DCM with peak current mode control is implemented using average switch modeling approach [6]. The average transistor voltage and current follows a power sink characteristic while the average diode voltage and current follows the power source characteristic. The power sink and source characteristic is explained in terms of inductor energy arguments. However the model do not include the circulating energy component of the converter, consequently results in incorrect prediction of DC Gain and dominant pole location of the converter. A modified small signal model including the circulating energy component ($E_{par}$) is derived to understand the impact of parasitic capacitance on converter dynamics.

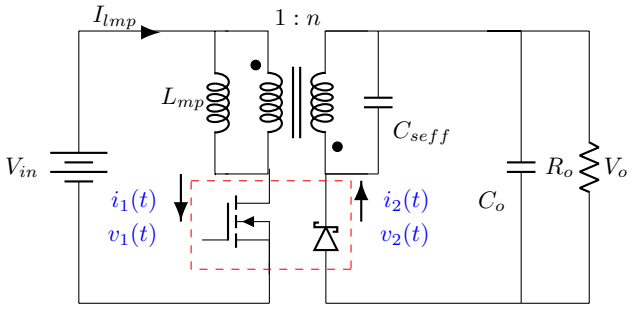


Fig. 11: Input and output port representation of HVLP flyback converter with parasitic capacitances included

MOSFET terminals forms the input port of the switch network, with the terminal waveforms of the input port defined by $v_1$(t) and $i_1$(t). HV diode terminals forms the output port of the switch network, with the terminal waveforms of the output port referred to primary side is defined by $v_2$(t) and $i_2$(t).
The HVLP flyback converter model shown in Fig. 11 is represented by reflecting the secondary side components to primary side, presented in Fig. 12.

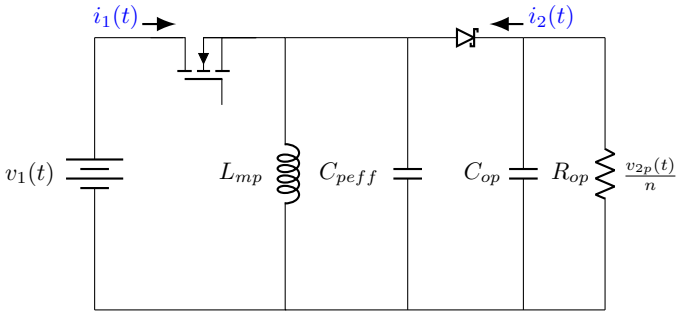


Fig. 12: Equivalent circuit model of HVLP flyback converter with secondary side components reflected to the primary

Considering an ideal flyback converter, average current carried by input and output port is defined by,
**Input port - ideal flyback**

$$< i_1 >_{Ts} = \frac{L_{mp}{i_c}^2 f_s}{2 < v_1 >_{Ts}} \quad (15)$$

**Output port - ideal flyback**

$$< i_2 >_{Ts} = \frac{L_{mp}{i_c}^2 f_s}{2 < v_{2p} >_{Ts}} \quad (16)$$

where $i_c$ is the reference control current required to reach $v_{2p}$.
In an HVLP flyback converter with circulating energy component included, the average terminal currents are modified

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as,

**Input port - HVLP flyback**

$$< i_1 >_{Ts} = \frac{L_{mp} {i_c}^2 f_s - C_{peff}({v_{2p}}^2 - {v_1}^2) f_s}{2 < v_1 >_{Ts}} \quad (17)$$

**Output port - HVLP flyback**

$$< i_2 >_{Ts} = \frac{L_{mp} {i_c}^2 f_s - C_{peff}({v_{2p}}^2 - {v_1}^2) f_s}{2 < v_{2p} >_{Ts}} \quad (18)$$

where, $v_{2p}$ is the average voltage of the output port referred to primary and $i_c$ is the reference control current.
Perturbation and linearisation of converter input and output port equations around the steady state operating point yields the small signal model of the converter.

$$< i_2 >_{Ts} = f(i_c, v_1, v_{2p}) \quad (19)$$

$$\hat{i_2} = \frac{\partial i_2}{\partial i_c}\hat{i_c} + \frac{\partial i_2}{\partial v_1}\hat{v_1} + \frac{\partial i_2}{\partial v_{2p}}\hat{v_{2p}} \quad (20)$$

$$\frac{\partial i_2}{\partial i_c} = f_2 \quad (21)$$

$$\frac{\partial i_2}{\partial v_1} = g_i \quad (22)$$

$$\frac{\partial i_2}{\partial v_{2p}} = g_o = \frac{1}{r_o} \quad (23)$$

Differentiating eq.(18) with respect to $i_c$, $v_{2p}$

$$f_2 = \frac{L_{mp} I_c F_s}{V_{op}} \quad (24)$$

$$g_o = \frac{1}{r_o} = \frac{1 + R_{op} C_{peff} F_s}{R_{op}} \quad (25)$$

where $R_{op}$ is the load resistance referred to primary of flyback transformer.
The control to output transfer function is given by,

$$\hat{v_o} = f_2 \hat{i_c} \frac{r_o || \frac{1}{sC_{op}}}{R_{op} + r_o || \frac{1}{sC_{op}}} \quad (26)$$

$$\frac{\hat{v_o}}{\hat{i_c}} = \frac{L_{mp} R_{op} I_c F_s}{2V_{op}(1 + \frac{R_{op} C_{peff} F_s}{2} + \frac{S R_{op} C_{op}}{2})} \quad (27)$$

Eq.(27) gives the control to ouput transfer function of HVLP flyback converter including the circulating energy component. Substituting $C_{peff}$ = 0 in Eq.(27) gives the small signal model of ideal flyback converter in DCM.
Fig. (13) & (14) shows the frequency response of control to output transfer function of an ideal and HVLP flyback converter feeding 546 kΩ and 20 MΩ respectively. A significant deviation in DC gain is observed compared to ideal conditions. The low frequency pole of the converter is shifted by 1+ $\frac{R_{op} C_{peff} F_s}{2}$ times away from the origin compared to ideal converter pole. Fig. 14 presents a larger deviation compared to Fig. 13 indicating the extremely light loaded condition (200 mW resistive load) where the circulating energy component due to parasitic capacitance dominates the load energy. Ideal model provides an underestimate of input energy ignoring the dominant parasitic capacitance effect, thus demands several trials to attain an

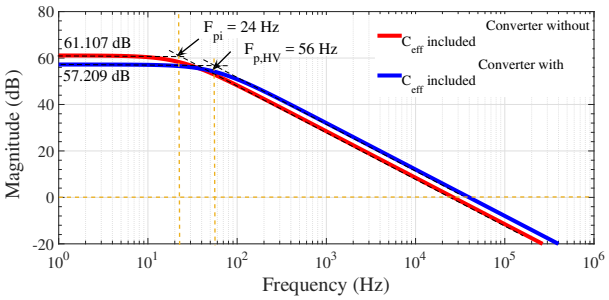


Fig. 13: Frequency response of ideal flyback (without parasitic capacitances) and HVLP flyback converter (with parasitic capacitances included) considering $R_o$ : 546 kΩ

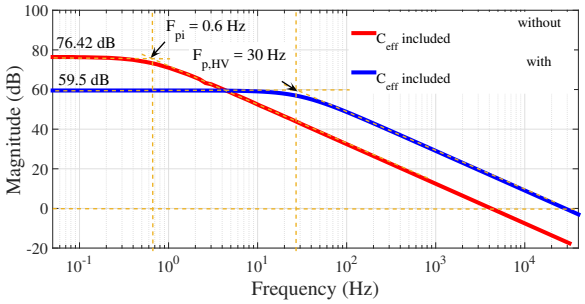


Fig. 14: Frequency response of ideal flyback (without parasitic capacitances) and HVLP flyback converter (with parasitic capacitances included) considering $R_o$ : 20 MΩ

appropriate design. Hence, an estimate of input magnetising energy ($E_{mag}$) including the circulating energy component is critical in HVLP application to achieve a desired voltage. The derived analytical energy based model aids in design of power stage (semiconductor selection & HV transformer design) and controller design.

## IV. Design and Implementation

Following the energy based analysis presented in section III, a HV flyback transformer is designed.

- Choosing an optimum turns ratio of HV transformer and semiconductor device selection are interrelated. The minimum and maximum turns ratio is calculated considering reduced voltage stress on the primary MOSFET and the HV diode respectively [18].
- Determination of HV transformer parameters including the magnetising inductance ($L_m$) and peak current selection ($I_{pk}$) is a function of circulating energy ($E_{par}$) which is dominantly governed by winding capacitance under light loaded conditions. A comprehensive study on winding capacitance of HV transformers is presented in [7]–[9], [21]. The winding capacitance is a function of geometrical parameters i.e. diameter & dimensions of the conductor, material properties such as the dielectric constant of insulating material and the winding strategy. Hence estimation of winding capacitance prior to the design phase is complex considering significant analytical error margins caused in practical implementation. Neglecting the winding capacitance

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($C_w$) in computing the input energy $E_{in}$ (thus $L_m$ & $I_{pk}$) leads to a trial and error based approach in achieving an appropriate design.

Several transformer winding architectures for HVLP applications is investigated in [8]. It is observed the winding capacitance (referred to secondary) of an interleaved non sectioned HV flyback transformer is in the range of 15 - 25 pF. A worst case winding capacitance of 25 pF referred to the secondary is considered to initiate the design. Steady state switching frequency ($F_s$) of 100 kHz and an optimum turns ratio ($n$) of 17 is selected considering 5 W load. Steady state efficiency ($\eta$) of 80% is assumed in design.

Following the energy balance equation in steady state, (Eq.10)

$$E_{in} = \eta \frac{L_{mp} I_{pk}^2}{2} = \frac{C_{seff}(V_o^2 - n^2 V_{in}^2)}{2} + \frac{V_o^2}{RF_s} \quad (28)$$

the input energy ($E_{in}$) required to reach the desired voltage ($V_o$) is computed. Maximum limit on the primary magnetising current ($I_{pk,max}$) defines the minimum primary magnetising inductance ($L_{mp,min}$).

Resonant frequency of the converter is designed to be atleast three times greater than the converter's steady state switching frequency. Eq. (30) defines the maximum value of primary magnetising inductance ($L_{mp,max}$).

$$\frac{\omega}{\omega_s} > 3 \quad (29)$$

where, $\omega_s$ is the steady state converter's switching frequency.

$$\sqrt{L_{mp,max} C_{peff}} < \frac{1}{3(2\pi F_s)} \quad (30)$$

Computation of $L_{mp}$ and $I_{pk}$ leads to selection of suitable transformer core and wire guage [6].

The designed transformer is characterised using AP300 frequency response analyser and the winding capacitance of the transformer referred to secondary is computed to be 19 pF. The experimental prototype of HVLP flyback converter is presented in Fig. 15. Table. IX presents the power stage parameters and HVLP flyback transformer parameters.

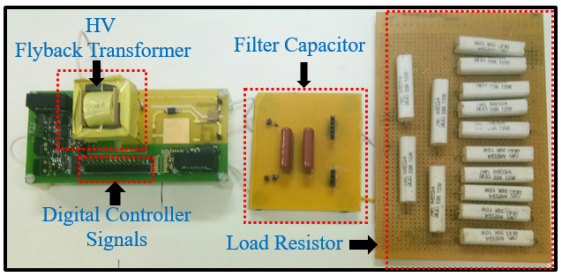


Fig. 15: Hardware prototype of HVLP flyback converter.

The control scheme shown in Fig. 16 presents a two loop control logic. Inner loop defines the Zero voltage switching instant (ZVS turn-on) and peak current mode control turn off instant (PCMC turn-off). Inner loop includes two high speed comparator (TLV3501) where comparator 1 compares the switch voltage ($V_{ds}$) & input voltage ($V_{in}$) and generates a trigger corresponding to $V_{ds} < V_{in}$ [18]. The generated trigger is delayed by a constant programmed delay of $\frac{\pi}{\omega}$ post the diode conduction interval to initiate the primary MOSFET switch turn on (ZVS turn-on instant). Comparator 2 compares the reference peak current ($I_{pk}$) computed from the outer loop with the magnetising inductance current ($I_{lmp}$) to ensure PCMC turn-off.

TABLE IX: Power stage and flyback transformer specifications

| Specifications | Values |
|---|---|
| **Power stage specifications** | |
| $V_{in}$ | 12 V |
| $V_{out}$ | 1500 V |
| Primary side Low Voltage MOSFET | 200 V/ 3.9 A (FDS2672CT - ND) |
| Secondary side High Voltage Diode | 3300 V/0.3 A (GAP3SLT33-214) |
| MOSFET Switch Node Capacitance ($C_{sw}$) | 135 pF |
| Diode Capacitance ($C_d$) | 7 pF |
| **Flyback transformer Specifications** | |
| Core Material used | Ferrite (N87) E30/15/7 |
| $N_p$ | 6 |
| $N_s$ | 102 |
| $L_{mp}$ | 25.52$\mu$H |
| $L_{ms}$ | 7.37mH |
| Winding Capacitance referred to Sy. | 19 pF |
| DC resistance of Py./ Sy. winding | 46.2 m$\Omega$ / 9.4 $\Omega$ |
| Leakage Inductance referred to Py. | 0.52 $\mu$H |
| Diameter of Py./Sy. Winding | 0.711 mm / 0.345 mm |
| Number of Layers of Transformer Py. / Sy. | 1 / 4 |

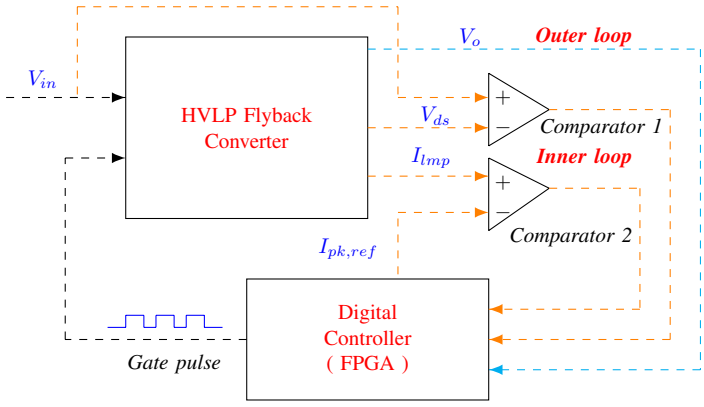


Fig. 16: Two loop control scheme implemented in HVLP flyback converter

Outer loop includes a 1000:1 RC divider sensing circuit, 12 bit analog to digital converter (ADS7886), a compensator implemented using MAX-10 FPGA which computes the primary peak current ($I_{pk,ref}$) required to achieve $V_o$.

## V. Results and Discussion

### A. Steady State Performance

The peak current demanded by the HVLP Flyback converter to reach 1.5 kV in the presence of parasitic

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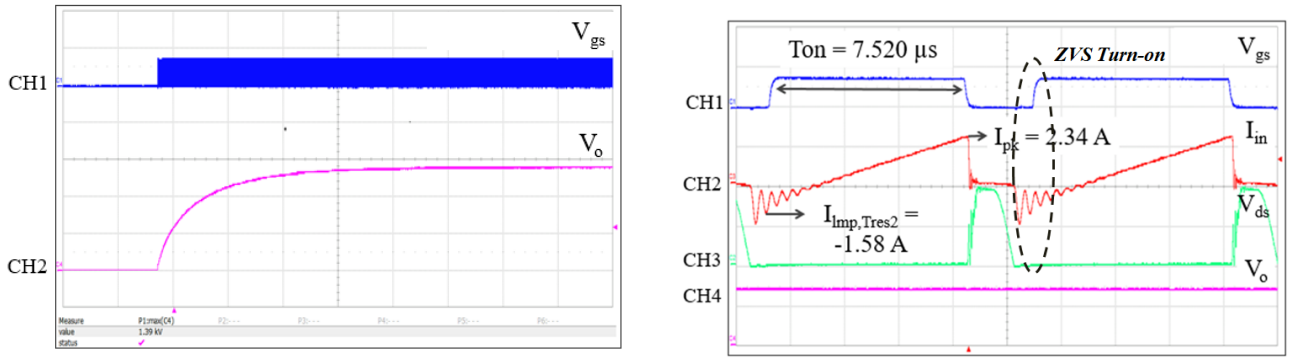


Fig. 17: Experimental results considering case 1 : $R_o$ - 546 kΩ a) gate pulse ($V_{gs}$) and output voltage ($V_o$) ; CH1: 20 V/div gate pulse; CH2: 500 V/div output voltage; Time scale: 2 ms/div. b) Key waveforms of the HVLP flyback converter CH1: 20 V/div gate pulse; CH2: 2 A/div input source current; CH3: 50 V/div voltage across the primary MOSFET; CH4: 500 V/div output Voltage; Time scale: 2 $\mu$s/div

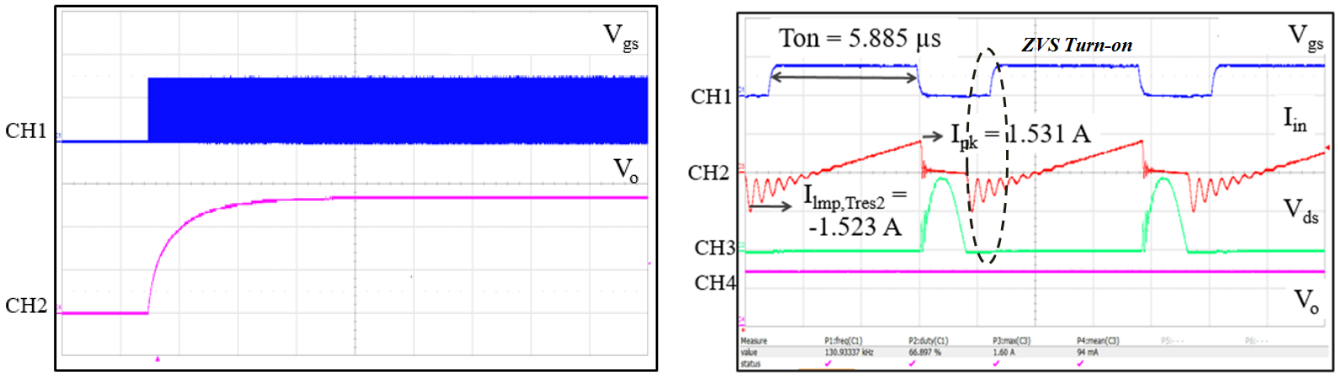


Fig. 18: Experimental results considering case 2 : $R_o$ - 20 MΩ a) gate pulse ($V_{gs}$) and output voltage ($V_o$); CH1: 20 V/div gate pulse; CH2: 500 V/div output voltage; Time scale: 5 ms/div b) Key waveforms of the HVLP flyback converter CH1: 20 V/div gate pulse; CH2: 2 A/div input source current; CH3: 50 V/div voltage across the primary MOSFET; CH4: 500 V/div output Voltage; Time scale: 2 $\mu$s/div

capacitances is computed using the energy based model considering the test loading conditions and is provided externally to the converter. The key waveforms of the converter are validated both through simulation and experimental prototype on two different loading conditions presented in Table.II.

Fig. 17 presents the key waveforms of HVLP flyback converter considering a resistive load of 546 kΩ. A input peak current of $I_{pri,pk}$ = 2.34 A is demanded by the converter to reach 1.5 kV. The steady state switching frequency is 101 kHz and the negative peak current which is the characteristic of the converter is found as $I_{lmp,Tres2}$ = -1.5 A. Fig. 18 presents the key waveforms of HVLP flyback converter considering a resistive load of 20 MΩ. A input peak current of $I_{pri,pk}$ = 1.53 A is demanded by the converter to reach 1.5 kV. The steady state switching frequency is 125 kHz. ZVS characteristic is observed from the switch voltage waveforms presented in Fig. 17 and 18. A initial negative current is carried by the MOSFET switch (Body diode of MOSFET in conduction) at the instant of turn on which ensures (ZVS) zero turn on loss in the converter under steady state.

High frequency ringing oscillations is observed in the converter's input current and switch voltage waveforms owing to the energy exchange between the leakage inductance and parasitic capacitance. The frequency of oscillation observed in the current waveforms is given by $\frac{1}{2\pi\sqrt{L_{lkp}C_{p,eff}}}$ (corresponds to 2.504 MHz).

The various losses in steady state and prototype efficiency considering 5 W resistive load is presented in Table. X. The steady state efficiency of the prototype feeding 5 W load is 81.6 %. 200 mW resistive load almost resembles a capacitive load with the converter losses dominating the output power in steady state. Table.VII & VIII reveals the major fraction of steady state input energy is the circulating energy in case of 200 mW resistive load. Hence, defining charging efficiency rather than steady state efficiency is more appropriate under such light loaded condition. Table.XI presents the individual loss components and charging efficiency to reach 1500 V. The charging efficiency of converter prototype feeding 200 mW load is 77.6 % [16, 17].

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TABLE X: Loss distribution & steady state efficiency considering 5 W resistive load

| Specifications | Values |
|---|---|
| **Transformer Loss** | |
| Primary winding conduction loss | 0.5349 $\mu$J |
| Secondary winding conduction loss | 0.08576 $\mu$J |
| Transformer core loss | 0.011 $\mu$J |
| **Leakage inductance Loss** | |
| Leakage loss | 1.447 $\mu$J |
| **Semiconductor conduction Loss** | |
| MOSFET conduction loss | 0.6357 $\mu$J |
| Body diode conduction loss | 1.7244 $\mu$J |
| High Voltage diode conduction loss | 0.0458 $\mu$J |
| **Semiconductor switching Loss** | |
| MOSFET Turn on loss | 0 |
| MOSFET Turn off loss | 4.62 $\mu$J |
| **Net energy loss** | 9.104 $\mu$J |
| **Load energy** | 40.559$\mu$J |
| **Efficiency** | 81.7 % |

TABLE XI: Loss distribution & charging efficiency considering 200 mW resistive load

| Specifications | Values |
|---|---|
| **Transformer Loss** | |
| Primary winding conduction loss | 0.2762 mJ |
| Secondary winding conduction loss | 0.0852 mJ |
| Transformer core loss | 0.0016 mJ |
| **Leakage inductance Loss** | |
| Leakage loss | 0.2764 mJ |
| **Semiconductor conduction Loss** | |
| MOSFET conduction loss | 0.9625 mJ |
| Body diode conduction loss | 1.6 mJ |
| High Voltage diode conduction loss | 0.045 mJ |
| **Semiconductor switching Loss** | |
| MOSFET Turn on loss | 0.420 $\mu$J |
| MOSFET Turn off loss | 3.1 mJ |
| **Net energy loss** | 0.0064 J |
| **Load energy** | 0.0221 J |
| **Efficiency** | 77.6 % |

### *B. Dynamic Response of HV Flyback Converter*

The transfer functions involved with the compensator are designed based on the small signal model derived in section III-B. To validate the derived mathematical expression of output voltage to control current transfer function ($\frac{\hat{v_o}}{\hat{i_c}}$), AP300 frequency response analyser is used which injects a small signal to the input peak current through a 1:1 injection transformer. A small signal is injected to the computed peak current under test loading conditions namely 1500 V / 546 kΩ and 1500 V / 20 MΩ. The analyser measures the ratio of injected signal to the output voltage and plots the magnitude gain as shown in Fig. 19 and Fig. 20. The experimental bode plots are in good agreement with the analytical plots. A compensator is designed to obtain a desired regulation accuracy along with better transient response. Phase margin of the plant is maintained at 75° while the cross over frequency is kept at less than $1/10^{th}$ of the minimum switching frequency of the converter.
Fig. 21,23 presents the converter tracking a reference input of 1V to deliver a regulated output voltage of 1000 V on 546 kΩ and 20 MΩ resistive loads. Fig. 22,24 shows the 1- 1.25 V step reference transient in the reference voltage which corresponds to change in output from 1000 - 1250 V considering 546 kΩ and 20 MΩ.

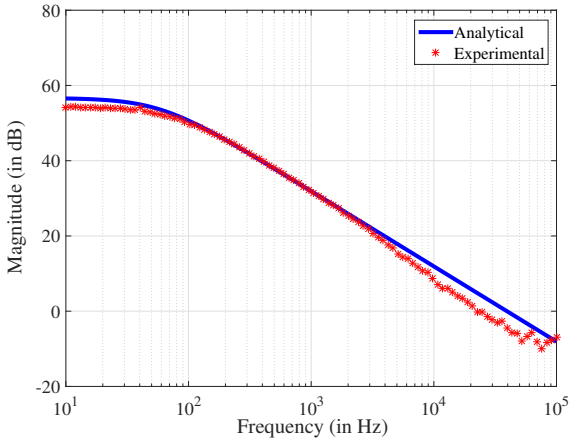


Fig. 19: Analytical and experimental magnitude bode plots of output voltage to control current transfer function ($\frac{\hat{v_o}}{\hat{i_c}}$) considering test loading conditions: 1500 V / 546 kΩ

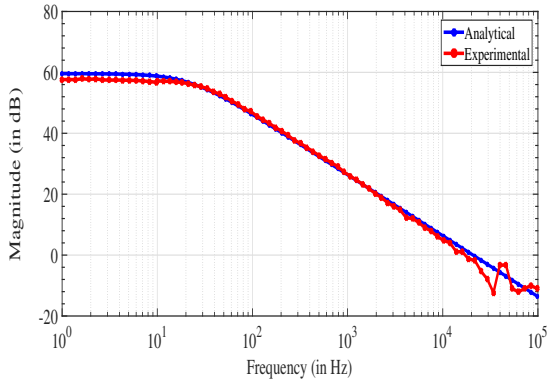


Fig. 20: Analytical and experimental magnitude bode plots of output voltage to control current transfer function ($\frac{\hat{v_o}}{\hat{i_c}}$) considering test loading conditions: 1500 V / 20 MΩ

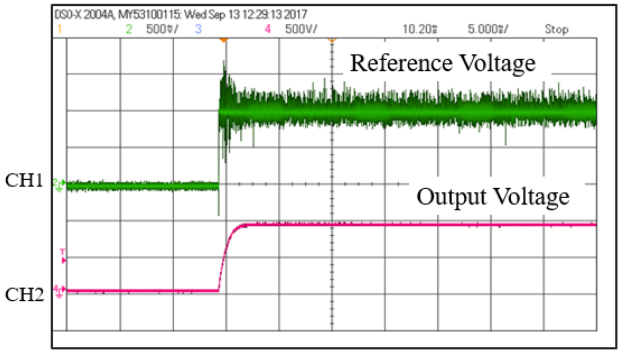


Fig. 21: Experimental results considering case 1 : $R_o$ - 546 kΩ : regulated output voltage of 1000 V CH1: 500 mV/div reference voltage CH2: 500 V/div output voltage; Time scale: 5 ms/div

Experimental results shows that the controller undergoes smooth transition from one operating point to other following the reference step change under different loading conditions.

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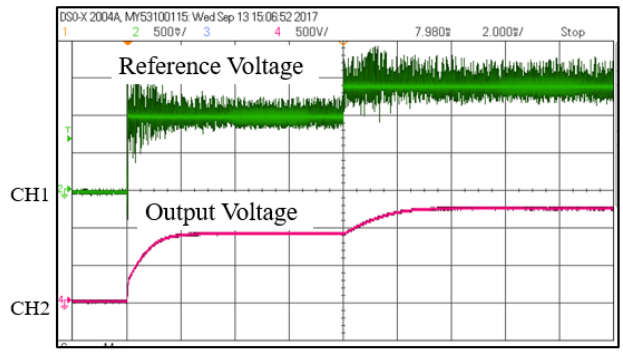


Fig. 22: Experimental results considering case 1 : $R_o$ - 546 kΩ : b) Converter subjected to a step change of 250 V at 8ms a) CH1: 500 mV/div reference voltage CH2: 500V/div output voltage; Time scale: 2 ms/div

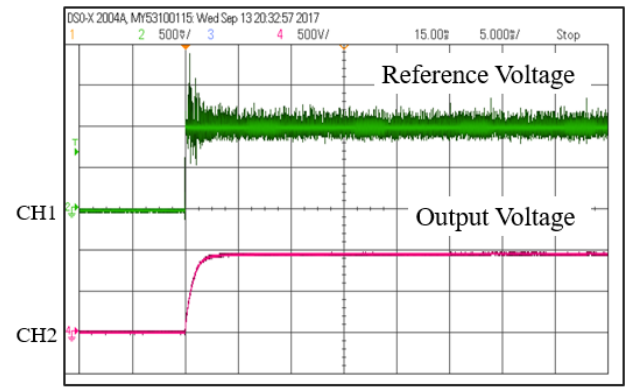


Fig. 23: Experimental results considering case 2 : $R_o$ - 20 MΩ : regulated output voltage of 1000 V CH1: 500 mV/div reference voltage CH2: 500 V/div output voltage; Time scale: 5 ms/div

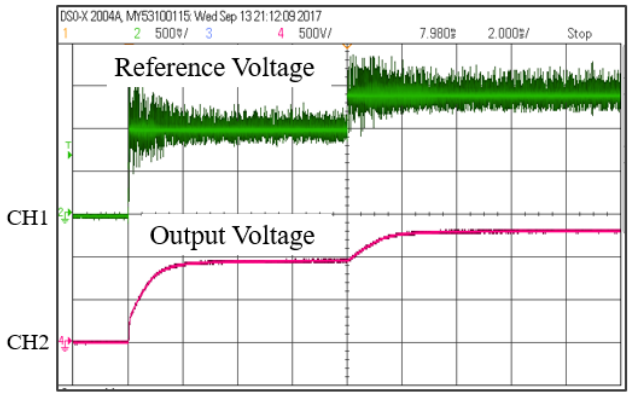


Fig. 24: Experimental results considering case 2 : $R_o$ - 20 MΩ : b) Converter subjected to a step change of 250 V at 8ms a) CH1: 500 mV/div reference voltage CH2: 500V/div output voltage; Time scale: 2 ms/div

## VI. Conclusion

A dominant impact of parasitic capacitance is observed in a HVLP flyback converter. Implementing ideal flyback converter model ignores the parasitic capacitance effect hence underestimates the amount of input energy required to reach a desired output voltage. The circuit based mode equations of converter including the parasitic capacitance effect is presented and extended to steady state to derive the steady state voltage gain of a HVLP flyback converter feeding resistive loads. Circuit based equations demand a mathematically intensive procedure to determine the converter operating point. Hence, a simplified energy based model which provides better insight on the parasitic energy is proposed and an expression for steady state peak current required to achieve desired output voltage is derived. A modified dynamic model including the parasitic capacitances of the converter is derived to implement a compensator based control scheme for achieving steady state voltage regulation targeting low power resistive loads. The proposed analytical model is validated through simulation and experimental results. The simulation and experimental results obtained are in good agreement with analytical results.

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## References

[1] Z. Xu, X. Wang, R. J. Weber, R. Kumar, and L. Dong, "Microfluidic eletrophoretic ion nutrient sensor," in *2016 IEEE SENSORS*, Oct 2016, pp. 1–3.

[2] D.McCann, S.Barabash, H.Nilsson, and A.Bhardwaj, "Miniature ion mass analyser," in *Planetary and Space Sciences*, June 2007, pp. 1190–1196.

[3] J. M. Alonso, C. Ordiz, M. A. D. Costa, J. Ribas, and J. Cardesin, "High-voltage power supply for ozone generation based on piezoelectric transformer," *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1513–1523, July 2009.

[4] R. J. Wood, "Driving high voltage piezoelectric actuators in microrobotic applications," 2012.

[5] S. D. Johnson, A. F. Witulski, and R. W. Erickson, "Comparison of resonant topologies in high-voltage dc applications," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 24, no. 3, pp. 263–274, May 1988.

[6] R. W. Erickson and D.Maksimovic, "Fundamentals of power electronics," *Springer*, 2001.

[7] L. Dalessandro, F. da Silveira Cavalcante, and J. W. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 2081–2092, Sept 2007.

[8] P. Thummala, H. Schneider, Z. Zhang, and M. A. E. Andersen, "Investigation of transformer winding architectures for high-voltage (2.5 kv) capacitor charging and discharging applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5786–5796, Aug 2016.

[9] P. Thummala, H. Schneider, Z. Zhang, Z. Ouyang, A. Knott, and M. A. E. Andersen, "Efficiency optimization by considering the high-voltage flyback transformer parasitics using an automatic winding layout technique," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5755–5768, Oct 2015.

[10] H. Kewei, L. Jie, H. Xiaolin, and F. Ningjun, "Analysis and simulation of the influence of transformer parasitics to low power high voltage output flyback converter," in *2008 IEEE International Symposium on Industrial Electronics*, June 2008, pp. 305–310.

[11] M. J. Prieto, A. Fernandez, J. M. Diaz, J. M. Lopera, and J. Sebastian, "Influence of transformer parasitics in low-power applications," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol. 2, Mar 1999, pp. 1175–1180 vol.2.

[12] J. Mcardle, T. G. Wilson, and R. C. S. Wong, "Effects of power-train parasitic capacitance on the dynamic performance of dc-to-dc converters operating in the discontinuous mmf mode," *IEEE Transactions on Power Electronics*, vol. PE-2, no. 1, pp. 2–19, Jan 1987.

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[13] S. K. Chung, "Transient characteristics of high-voltage flyback transformer operating in discontinuous conduction mode," *IEE Proceedings - Electric Power Applications*, vol. 151, no. 5, pp. 628–634, Sept 2004.
[14] S.-S. Hong, S.-K. Ji, Y.-J. Jung, and C.-W. Roh, "Analysis and design of a high voltage flyback converter with resonant elements," *Journal of Power Electronics*, vol. 10, no. 2, Sept March 2010.
[15] L. Huang, Z. Zhang, and M. A. E. Andersen, "Analytical switching cycle modeling of bidirectional high-voltage flyback converter for capacitive load considering core loss effect," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 470–487, Jan 2016.
[16] P. Thummala, H. Schneider, Z. Ouyang, Z. Zhang, and M. A. E. Andersen, "Estimation of transformer parameters and loss analysis for high voltage capacitor charging application," in *2013 IEEE ECCE Asia Downunder*, June 2013, pp. 704–710.
[17] S. H. Kang, D. Maksimovi, and I. Cohen, "Efficiency optimization in digitally controlled flyback dc dc converters over wide ranges of operating conditions," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3734–3748, Aug 2012.
[18] P. Thummala, D. Maksimovic, Z. Zhang, and M. A. E. Andersen, "Digital control of a high-voltage (2.5 kv) bidirectional dc–dc flyback converter for driving a capacitive incremental actuator," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8500–8516, Dec 2016.
[19] V. Ravi and N. Lakshminarasamma, "Steady state voltage gain of flyback converter for high voltage low power applications," *International Conference PEDES 2016*, Sept 2016.
[20] S. Gunewardena, W. E. Archer, and R. O. Sanchez, "High voltage miniature transformer design," in *Proceedings: Electrical Insulation Conference and Electrical Manufacturing and Coil Winding Conference (Cat. No.01CH37264)*, 2001, pp. 141–147.
[21] P. Thummala, H. Schneider, Z. Zhang, A. Knott, and M. A. E. Andersen, "Optimization of bi-directional flyback converter for a high voltage capacitor charging application," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, March 2014, pp. 2556–2563.

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