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Optimum structure of a generalized three-phase reduced switch multilevel inverter

Ravi Raushan*, Saikat Majumdar, Kartick Chandra Jana

Department of Electrical Engineering, Indian Institute of Technology (Indian School of Mines), Dhanbad, India

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ABSTRACT

This study presents a new generalized three-phase multilevel converter based on the combinations of half-bridge modules along with a three-phase T-Type multilevel inverter. The proposed topology reduces the number of switches and associated gate-driver circuits that attains much higher number of output voltage levels. The optimized structure of the proposed three-phase inverter topology has been developed to obtain the maximum number of output voltage levels of the inverter with a minimum number of power electronic switches and the DC voltage sources. The operation, control and performance analysis of the proposed generalized multilevel inverter have been considered here. A nearest level control (NLC) technique is adopted to generate the gating signal for the proposed three-phase hybrid inverter. A laboratory prototype of a specimen three-phase low power fifteen-level inverter have been designed using twenty four switches and nine voltage sources. The conduction losses of the proposed fifteen level inverter is around 14.71 watt/phase compared to 23.26 watt/phase in an asymmetrical cascaded inverter. The exhaustive simulations of the proposed three-phase inverter are performed using MATLAB/SIMULINK and the results are verified experimentally and presented for the different modulation index.

1. Introduction

In power electronics, multilevel power conversion technology is evolving in a rapid manner with good potential and wide future scope. The multilevel inverter (MLI) topology using small voltage magnitude to achieve the required voltage magnitude was introduced in 1975 [1]. In the conventional two-level inverter, the quality of the output power (THD) can be improved to a certain bound with the increase of inverter switching frequency on the cost of high switching loss. Benefits of multilevel inverters using medium power semiconductor over the conventional two-level inverter with high-power semiconductors include low switching stress, better electro-magnetic compatibility, low switching losses, high voltage capability, reduced losses, shrinks the filter size, possibility of fault tolerance and improved performance [2–4]. The extensive applications of inverter can be used to a variable frequency drives, un-interrupted power supply (UPS), conveyors, ID and FD fans, medium voltage traction drive, blowers, pumps, compressors, EV/HEV, HVDC system, Static VAR compensators, FACTs, PV system, smart grids and renewable energy [4–6].

The most common multilevel inverter topologies including neutral-point clamped MLI (NPC-MLI) [7], flying capacitor based MLI (FC-MLI) [8], and cascaded H-bridge MLI (CHB-MLI) [9] are well established and commercially available with various control techniques specific to the applications. The power quality of the MLI improves with the step resolution of voltage. Which in turn increases the number of device count, driver circuit, protection circuit and its size as well as cost and control complexity with reduced efficiency as well as the reliability of the inverters. Hence, the number of voltage levels restrict to the tradeoff between the number of voltage levels and the costs as well as the complexity of the inverter circuit. Symmetrical multilevel inverters come up with the benefits in terms of modular structure, homogeneous control, and the easy availability of equal DC sources. Asymmetry and hybridization in multilevel inverter configuration have high conversion efficiency and further reduces the size and cost [10,11] of the MLI. DC voltage sources with unequal magnitudes and/or capacitors with balanced voltages reduces the number of DC sources. Though, the different multilevel topologies lose its modularity, switching redundancies and DC source of voltage magnitude depending on the number of levels that limits its industrial applications [12]. However, multilevel inverter with reduced component [2,3,10–22] for further improvement in total harmonic distortion (THD) has been reported as a challenge to perforate economic and density constrains to a

* Corresponding author.
E-mail addresses: ravi.roshan.b15@nitp.ac.in (R. Raushan), sm.16dr000205@ee.ism.ac.in (S. Majumdar).

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greater extent. Hence, considered provocative in research along with industry for further improvement in power quality and control.

On the other hand, three-phase inverters have been developed as T-type inverter [17] and pin mid-point (PMP) MLI [18]. However, these three-phase inverters require a large number of switching devices and symmetrical DC sources. For designing a three-phase reduced switch inverters using the single-phase MLI, all component counts, including DC sources become three times [11,22]. The hybrid MLI has been designed combining basic three-phase two-level inverter and several symmetrical H-bridges that require a large number of switches [12,20]. A three-phase hybrid inverter combining three-phase two-level inverter with several two-level auxiliary modules has been proposed to reduce the number of switches [15]. However, this three-phase inverter unable to generate the negative voltage levels in their phase and hence the configuration cannot be applied for its single-phase applications. Some of the hybrid MLI configurations having a T-type/modified-T type with half-bridge [16] and full-bridge [19] converter modules respectively for required voltage polarity. However, the most of the proposed topologies used a large number of components including voltage sources also. In this paper a generalized three-phase inverter topology has been proposed combining a three-phase generalized T-type MLI to minimize the number of voltage sources and several half-bridges to increase the voltage levels including negative voltage levels. The benchmark for the comparison of these unaccustomed configurations are the ratio of the number of phase voltage levels to switch ratio (LSR) per phase, the number of phase voltage levels to the diode ratio (LDR) per phase as well as the number of DC sources or capacitive sources used per phase have been analyzed [15].

2. The proposed three-phase generalized hybrid multilevel inverter

In this paper a generalized three-phase multilevel inverter configuration is proposed and the detailed operation of a specimen fifteen-level inverter is analyzed. The schematic diagram of the generalized three-phase inverter is shown in Fig. 1(a). The entire three-phase inverter configuration is the series combinations of three converter sections consists of a generalized T-type inverter (inverter section-I), cascading of half-bridge inverters for increasing the voltage levels (inverter section-II) and one half-bridge inverter for reversing the polarity of the inverter voltage levels (inverter section-III).

The generalized T-type inverter (section-I) may consist of m number of unary voltage sources $\{E_{I,1} = E_{I,2} = E_{I,3} = ,\ldots, = E_{I,m} = E\}$, six unidirectional switches ($T_{I,a1}$, $T_{I,a2}$), ($T_{I,b1}$, $T_{I,b2}$), ($T_{I,c1}$, $T_{I,c2}$) along with m-1 number of bi-directional switches $T_{B,aj}$, $T_{B,bj}$, $T_{B,cj}$, {j = 1, 2, 3,. . ., (m-1)} for the inverter phase a, b and c respectively as shown in Fig. 1(a). In this inverter section, only one switch (either a bi-directional switch or a unidirectional switch) from each phase of the inverter should be remain ON in any mode of operation, which can be able to generate m numbers of positive voltage levels along with a zero voltage level (0, E, 2E, 3E,. . ., mE). For a three-phase inverter operation, though the number of devices becomes three times, however the DC link voltages are equally shared among the phases. By increasing the number of voltage sources, the number of phase voltage levels can be increased proportionally.

On the other hand, both of the above inverter section-II and -III (as of Fig. 1(a)) contains the half bridge inverters. Similar to the section-I, the section-II can also be designed to increase the inverter voltage levels using several half-bridge modules (n) that normally generate two voltage levels (0 & $E_{II,n}$). To increase the number of voltage levels of the inverter further, the half-bridges can be made asymmetric. Therefore, the combination of inverter section-I & II can be extended up to any desired number of voltage levels. The magnitude of DC voltage sources ($E_{II,n}$) for n number of half-bridge modules in section-II can be derived in a geometric progression to achieve maximum number of voltage levels as:

$$E_{II,n} = (1/2)^n \mathrm{E}, \text{ for} n = 1, 2, 3, \ldots, n. \quad (1)$$

However, the above two inverter section (I & II) can only generate positive voltage levels. Therefore, the design of inverter section-III is essential to generate all the negative voltage levels with the help of section-I & II. The inverter section-III have only one half-bridge module having two switches per phase (for phase-a) $T_{III,a}$ & $T'_{III,a}$ and one voltage source E_{III} with a maximum voltage rating (sum of the voltages in section-I & II) for obtaining the negative voltage levels. Thus, with the help of the section-III, the proposed inverter generates all the negative voltage levels and hence, doubled the number of inverter voltage levels. The magnitude of the voltage source of section-III is the algebraic sum of all the DC sources connected in section-I and section-II. Therefore, the magnitude of the E_{III} can be derived as:

$$E_{III} = (E_{I,1} + E_{I,2} + E_{I,3} + \ldots + E_{I,m}) + (E_{II,1} + E_{II,2} + E_{II,3} + \ldots + E_{II,n}) = mE + \sum_{n=1}^{n} (1/2)^n E \quad (2)$$

Hence, the proposed MLI can generate phase voltages of magnitude $-E_{III}$, $-(E_{III} - E_{II,n})$, $-(E_{III} - E_{II,n-1})$, $-(E_{III} - E_{II,n} - E_{II,n-1})$,. . .,$-E_{II,n}$, 0, $E_{II,n}$ . . . . ., $(E_{III} - E_{II,n} - E_{II,n-1})$, $(E_{III} - E_{II,n})$, E_{III}. A suitable delay must be incorporated between the switches belonging to each section of any phase to avoid the short circuit of the voltage sources. The switching status of all the switches of 'phase-a' with the corresponding voltage levels of the proposed inverter are given in Table 1. The switching table for the other two phases are identical, however, their switching signals are 120° and 240° apart from phase-a respectively.

A detailed per phase operation of the proposed multilevel inverter have been further explained for a specimen three-phase fifteen-level inverter as depicted in Fig. 1(b). For a three-phase fifteen-level inverter, the inverter section-I have three equal DC voltage sources (m = 3) of magnitude E can generate four voltage levels (0, E, 2E and 3E).

The inverter section-II consists of one half-bridge inverter module (n = 1) with a voltage source of magnitude 0.5E, that can generate two voltage levels (0 and 0.5E). The inverter section-III consists of one half-bridge inverter module having the magnitude of the voltage source is the summation of voltages in section-I and section-II as $E_{III} = 3.5E$ $\{E_{III} = E_{I,1} + E_{I,2} + E_{I,3} + E_{II,1}\}$, that can generate two voltage levels (0, −3.5E). Thus, the entire inverter is the cascading of the inverter section-I, II & III that can generate the fifteen voltage levels $\{2^2(3+1)-1\}$, as given by 3.5E, 3E, 2.5E, 2E, 1.5E, E, 0.5E, 0E, −0.5E, −E, −1.5E, −2E, −2.5E, −3E and −3.5E. The switching states, the corresponding switching status and the voltage generated by the different sections of the proposed fifteen-level inverter is given in Table 2.

3. Mathematical formulation of the parameters of the proposed multilevel inverter

For a high level inverter, to determine the optimum values of the number of switches and voltage sources for generating the maximum number of voltage levels, a generalized methodology has been developed. To implement this generalized technique, the expressions of inverter output phase voltage levels (L), the total number of switches (N_{SW}) and the DC voltage sources (N_V) for the proposed three-phase MLI have been derived as a function of

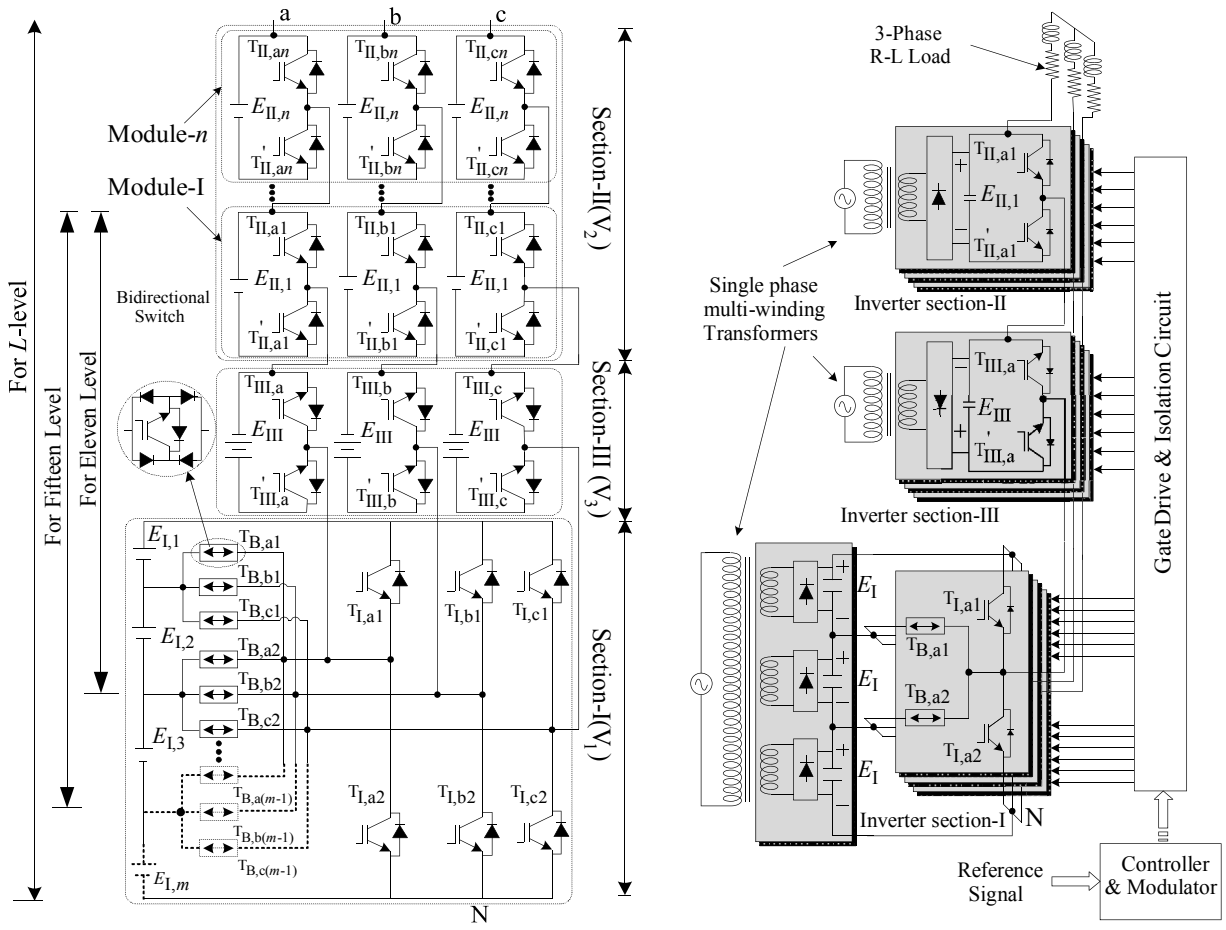

Fig. 1. Proposed three-phase MLI. (a) Generalized configuration (b) fifteen-level configuration.

Table 1
Switching states, status of the switches and the corresponding phase voltage (V_{ph}) of the proposed generalized three-phase inverter 'phase-a'.

State $(S_x)_{x=phase}$	Status of switches (1 = ON, 0 = OFF)													V_{ph}
	$T_{I,a1}$	$T_{B,a1}$	$T_{B,a2}$	...	$T_{B,a(m-1)}$	$T_{I,a2}$	$T_{II,a1}$	$T_{II,a2}$	...	$T_{II,a(n-2)}$	$T_{II,a(n-1)}$	$T_{II,an}$	$T_{III,a}$	
1	1	0	0	...	0	0	0	0	...	0	0	0	0	0
	0	0	0	...	0	1	1	1	...	1	1	1	1	
2	0	0	0	...	0	1	1	1	...	1	1	0	1	$E_{II,n}$
3	1	0	0	...	0	0	0	0	...	0	0	1	0	$-E_{II,n}$
4	0	0	0	...	0	1	1	1	...	1	0	1	1	$E_{II,n-1}$
5	1	0	0	...	0	0	0	0	...	0	1	0	0	$-E_{II,n-1}$
6	0	0	0	...	0	1	1	1	...	1	0	0	1	$E_{II,n}+E_{II,n-1}$
7	1	0	0	...	0	0	0	0	...	0	1	1	0	$-E_{II,n}-E_{II,n-1}$
8	0	0	0	...	0	1	1	1	...	0	1	1	1	$E_{II,n-2}$
9	1	0	0	...	0	0	0	0	...	1	0	0	0	$-E_{II,n-2}$
...	...	...	...	...	...		...	...	...	...	...	...	...	...
...	...	...	...	...	...		...	...	...	...	...	...	...	...
$2^{n+1}\cdot(m+1)-2$	1	0	0	...	0	0	0	0	...	0	0	0	1	E_{III}
$2^{n+1}\cdot(m+1)-1$	0	0	0	...	0	1	1	1	...	1	1	1	0	$-E_{III}$

the number of DC voltage sources (m) of inverter section-I and number of half-bridge inverter modules (n) of inverter section-II as depicted in Fig. 1(a). The number of voltage levels of the proposed inverter can be increased by increasing the number of DC voltage sources (extending the section-I of the inverter) in section-I and/or by increasing the number of half-bridge modules in inverter section-II. Therefore the generalized expression (given in the last row of Table 3) of the above parameters can be derived in terms of (n, m) based on Table 3.

The number of output voltage levels (L) contributed by the proposed MLI depends on the number of DC sources (m) in section-I and number of inverter modules (n) in section-III and can be expressed as:

$$L = 2^{n+1}\cdot(m+1)-1. \tag{3}$$

Further, for a desired possible value of inverter voltage levels (L), the total number of the components (such as sources (N_{SW}), switches (N_V), and diode (N_D)) is the aggregate sum of respective components of each invert section-I, II and III can be derived as:

$$N_{SW} = 3m+6n+9 = 12+6n+3\left(\frac{L-2^{n+2}+1}{2^{n+1}}\right). \tag{4}$$

Table 2
Switching states, status of the switches and the corresponding phase voltage (V_{ph}) of the proposed three-phase fifteen-level inverter with E_{II}:E_I:E_{III} = 1: 2: 7.

Switching state (S_x)	Status of switches (1 = ON, 0 = OFF)									V_{ph}
	$T_{I,a1}$	$T_{B,a1}$	$T_{B,a2}$	$T_{I,a2}$	$T_{II,a1}$	$T_{III,a1}$	V_1	V_2	V_3	
1	1	0	0	0	0	0	3E	0.5E	−3.5E	0
	0	0	0	1	1	1	0	0	0	
2	0	0	0	1	0	1	0	0.5E	0	+0.5E
3	1	0	0	0	1	0	3E	0	−3.5E	−0.5E
4	0	0	1	0	1	1	E	0	0	+E
5	0	1	0	0	0	0	2E	0.5E	−3.5E	−E
6	0	0	1	0	0	1	E	0.5E	0	+1.5E
7	0	1	0	0	1	0	2E	0	−3.5E	−1.5E
8	0	1	0	0	1	1	2E	0	0	+2E
9	0	0	1	0	0	0	E	0.5E	−3.5E	−2E
10	0	1	0	0	0	1	2E	0.5E	0	+2.5E
11	0	0	1	0	1	0	E	0	−3.5E	−2.5E
12	1	0	0	0	1	1	3E	0	0	+3E
13	0	0	0	1	0	0	0	0.5E	−3.5E	−3E
14	1	0	0	0	0	1	3E	0.5E	0	+3.5E
15	0	0	0	1	1	0	0	0	−3.5E	−3.5E

Table 3
Number of voltage levels (L), switches (N_{SW}) and the voltage sources (N_V) obtained by the proposed three-phase generalized MLI for various combinations of (n, m).

m	n									-			
	n = 1			n = 2			n = 3			-	n		
	L	N_{SW}	N_V	L	N_{SW}	N_V	L	N_{SW}	N_V	=	L	N_{SW}	N_V
m = 2	11	21	8	23	27	11	47	33	14	=	$3.2^{n+1}-1$	3(5 + 2n)	5 + 3n
m = 3	15	24	9	31	30	12	63	36	15	=	$4.2^{n+1}-1$	3(6 + 2n)	6 + 3n
m = 4	19	27	10	39	33	13	79	39	16	=	$5.2^{n+1}-1$	3(7 + 2n)	7 + 3n
m = 5	23	30	11	47	36	14	95	42	17	=	$6.2^{n+1}-1$	3(8 + 2n)	8 + 3n
--	--	--	--	--	--	--	--	--	--	-	--	--	--
m	4m + 3	15 + 3m	6 + m	8m + 7	21 + 3m	9 + m	16m + 15	27 + 3m	12 + m	-	$[(m+1).2^{n+1}-1]$	3(m + 3 + 2n)	(m + 3) + 3n

$$N_V = 3(n+1) + m = 3(n+1) + \left(\frac{L - 2^{n+1} + 1}{2^{n+1}}\right). \quad (5)$$

$$N_D = 6(2m+n) \quad (6)$$

Moreover, the mathematical expression of any output phase voltage ($V_{ph,x}$) for the proposed multilevel inverter can be derived as a product of the switching states (S) of switches and the associated voltage (E) of that switch in section-I, section-II and section-III. The switching function of IGBT switches ($T_{I,x1}$, $T_{I,x2}$) and bi-directional switches ($T_{B,xj}$) of section-I can be assumed ($S_{TI,x1}$, $S_{TI,x2}$) and $S_{TB,xj}$ respectively. Whereas, the switching function of the half-bridges in inverter section-II & III can be assumed as $S_{TII,xn}$ and $S_{TIII,x}$ respectively. Thus the expression of inverter phase voltage for any phase-x ($V_{ph,x}(t) = V_{1x}(t) + V_{2x}(t) + V_{3x}(t)$) can be expressed as the sum of the voltages of inverter section-I, II and III in terms of the respective switching functions as:

$$V_{ph,x}(t) = [S_{T1,x1}\sum_{i=1}^{m} E_{I,i} + \sum_{j=1}^{m-1}\left(\sum_{i=j+1}^{m} E_{I,i}\right) S_{T_{B,xj}} + S_{TI,x2}E_0]$$
$$+[\sum_{1}^{n} E_{II,n}\, S'_{T_{II,xn}}] + [-E_{III}\, S'_{T_{III,x1}}] \quad (7)$$

where, E_I, E_{II} and E_{III} are the voltage source across the inverter section-I, II & III respectively. While, the parameter E_0 is the zero voltage appeared across the lower switches of the inverter section-I considered as no voltage source is active.

4. Methodology to determine the optimum design of the proposed generalized three-phase inverter

The purpose of this study is to find out the optimum inverter design having maximum number of voltage levels by using a minimum number of switches and the voltage sources. The number of voltage levels can be further increased by increasing the number of switches (N_{SW}) and the number of voltage sources (N_V). Thus the generalized expression of inverter voltage levels (L) can be derived to find the most optimum inverter configuration that generates the maximum number of voltage levels with a given number of switches or a given number of DC sources. This is also helpful for comparison of the inverter cost and complexity with the other inverter configuration.

4.1. Maximizing the number of voltage levels for a specific number of switches

The number of voltage levels (L) for the proposed inverter configuration can be derived with a given number of switches using Eqs. (3) and (4) as:

$$L = (m+1)2^{[N_{sw}-3(m+1)]/6} - 1 = A \times 2^{N_{sw}/6} - 1 \quad (8)$$

where, $A = (m+1)/2^{(m+1)/2}$ is an intermediate variable depends on the number of DC sources (m) in inverter section-I. The variations of $A = (m+1)/2^{(m+1)/2}$ with different values of m have been plotted for finding optimum value of 'm' where the parameter 'A' is maximum as shown in Fig. 2(a). It is observed from Fig. 2(a) that, the value of the parameter 'A' and hence the number of output voltage level (L) becomes maximum towards the lowest possible value of m = 2.

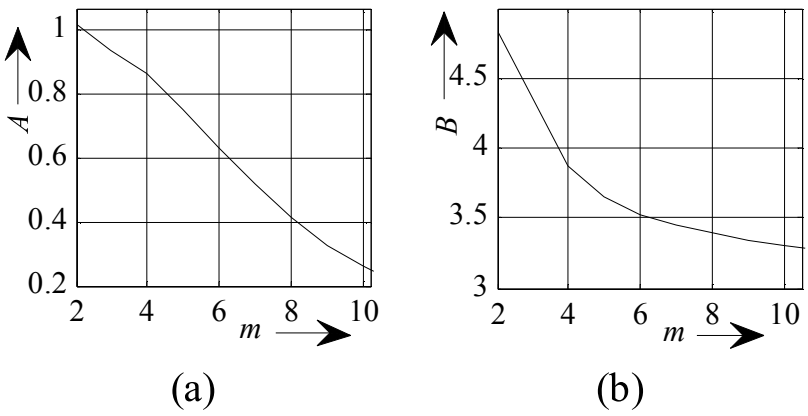

Fig. 2. Variations of the parameters (a) A with m and (b) B with m.

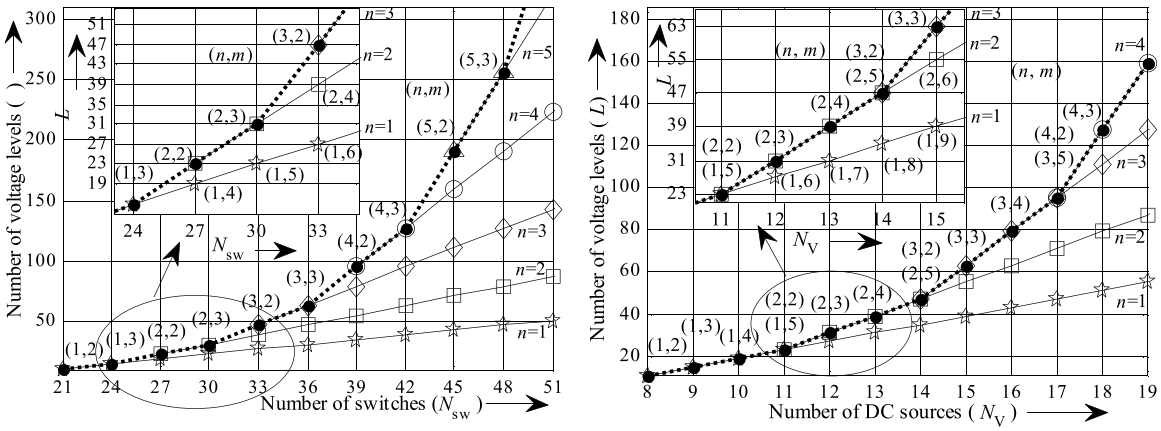

Fig. 3. Plots of inverter parameters for various value of (n, m) (a) voltage levels (L) versus number of switches (N_{SW}) and (b) voltage levels (L) versus number of voltage sources (N_V).

4.2. Maximizing the number of voltage levels with a given number of voltage sources

When the number of voltage sources (N_V) are given (or fixed), the design of the proposed MLI should be in such way that, the inverter can generate the maximum number of voltage levels (L). Thus, for a fixed number of DC voltage sources, the number of inverter voltage levels (L) can be expressed from Eqs. (3) and (4) as:

$$L = [(m+1)2^{(N_V-m)/3} - 1] = B \times 2^{N_V/3} - 1 \quad (9)$$

where, the parameter $B = (m+1)/2^{m/3}$ is an another intermediate variable depends on the value of m. Similar to the previous case the variation of parameter 'B' is plotted for different m as shown in Fig. 2(b) and it is observed that, the value of 'B' becomes maximum at $m = 2$.

4.3. Generalized configuration of the proposed MLI with a given voltage sources and switches

The number of voltage levels (L) of the proposed MLI configuration depends upon the values of m (ranging between 2 to m) and n (ranging between 1 to n) as per Eq. (3). However, from Fig. 2, it is observed that the maximum number of voltage levels (L) for a given number of switches (N_{SW}) and the voltage sources (N_V) depends on only and becomes maximum at $m = 2$. Hence, for increasing the number of voltage levels (L), the value of 'n' should be increased while the 'm' should be kept closer to 2. Moreover, from Fig. 2 and from Table 3, it is also observed that, the optimal design of the proposed MLI configuration for extensive utilization of all the given possible number of switches (N_{SW}) to generate the maximum number of output voltage levels (L) exist for $m \in \{2, 3\}$ and $n \in \{1,2,\ldots n\}$.

Moreover, it is observed from Table 3 that, the optimal design of the proposed MLI configuration for the extensive use of all the given possible number of voltage sources (N_V) to generate the maximum number of output levels (L) exists for $m \in \{2,3, 4\}$ and $n \in \{1,2,\ldots\}$. For further explanation of the above optimum combinations of (n, m), the L versus N_{SW} and L versus N_V have been plotted for all possible values of (n, m) as shown in Fig. 3. The number of switches (N_{SW}) can be increased by the various combinations of (n, m) as indicated by different markers for the all possible values of inverter voltage levels (L). While the dashed parabolic curves joining the dotted markers in Fig. 3(a) shows the locus of optimal values of (n, m) for several numbers of switches for the maximum values of L. Similarly, when the number of voltage sources (N_V) is increased, the various combinations of (n, m) can be obtained as shown by different markers for the all possible values of L as shown in Fig. 3(b). The locus of the dotted markers as directed by a dashed parabolic line indicate the most optimum combinations of (n, m) that synthesizes the maximum number of inverter voltage levels with various voltage sources. Thus, from Fig. 3, it's effortless to find the most optimum combinations of (n, m) and hence the most optimum combination of (N_{sw}, N_v) for an economical inverter design that produces the maximum inverter voltage levels.

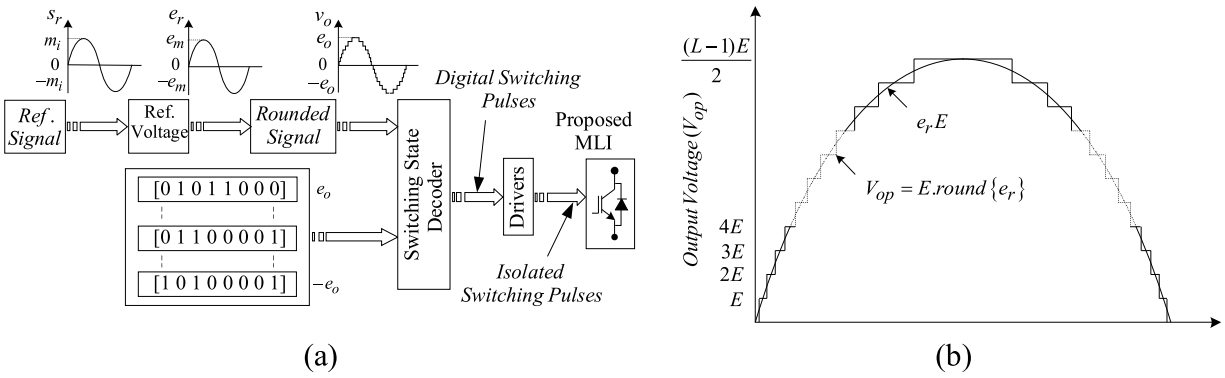

Fig. 4. Nearest level control technique (a) different stages of per phase implementation (b) corresponding output voltage (V_{op}) waveform of the inverter.

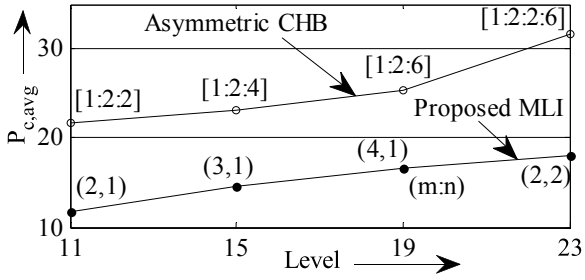

Fig. 5. Comparison of conduction loss of the proposed MLI with asymmetric CHB MLI with NLC at $m_i = 1$.

5. Modulation and control of the proposed three-phase multilevel inverter

A wide variety of modulation and control methods have been used for a multilevel converter such as sinusoidal pulse width modulation (SPWM) [23], single-carrier PWM [24], selective harmonic elimination PWM (SHE-PWM) [25,26], active harmonic elimination (AHE) [27], space vector modulation (SVM) [28,29] etc.

As a low frequency modulation technique, the nearest level control (NLC) [21,30] algorithms may generate the relatively less amount of switching losses as compared to any PWM technique. The NLC technique facilitates the synthesizing of a very high number of voltage levels by approximating the amplified voltage reference to the closest possible voltage level to be generated by the converter. The block diagram based NLC algorithm for the proposed fifteen-level inverter of any one phase is depicted in Fig. 4.

The corresponding mathematical equations of a reference signal (s_r), scaled up signal (e_r) and the corresponding rounded voltage signal (v_o) of the NLC for a fifteen-level inverter are given by:

$$s_r = m_i \sin(\omega t) \tag{10}$$

$$e_r = mi\frac{(L-1)}{2} \sin(\omega t) = e_m \sin(\omega t) \tag{11}$$

$$v_o = round\{e_r\} \tag{12}$$

$$V_{op} = E.round\{e_r\} \tag{13}$$

$$m_i = \frac{2\,e_m}{E(L-1)} \tag{14}$$

For the proposed three-phase fifteen-level inverter, the three-phase reference signals (s_r, 0 to 1) are first scaled to get (e_r) and then rounded to obtain the nearest level signal (v_o) using the round function (e.g. *round* {5.4} = 5, but *round* {5.6} = 6). Depending on the number of levels of the rounded voltage signal, the gate pulses of the inverter switches can be generated to produce the corresponding output voltage level. The reference signal (s_r), the switching signal (v_o) and the corresponding gate pulses are obtained using the NLC method is depicted as shown in Fig. 4.

To study the effectiveness of the proposed NLC technique (low switching frequency modulation technique) for the proposed MLI, the inverter losses, especially the conduction loss (negligible switching loss) is required to be calculated. The conduction losses of the inverter switches can be determined by the switching signal (v_o) generated by NLC (as shown in Fig. 4(a)) and the decoded pulse pattern of the switching state (as given in Table 2). The instantaneous conduction losses (losses due to conduction of a switch/diode) of an IGBT switch ($P_{c,T}(t)$) and its antiparallel diode ($P_{c,D}(t)$) can be expressed as follows [11]:

$$p_{c,T}(t) = [V_t + R_t I^{\beta}(t)]I(t) \tag{15}$$

$$P_{c,d}(t) = [V_d + R_d I(t)]I(t) \tag{16}$$

While, instantaneous conduction losses of a bidirectional switch ($p_{c,B}(t)$), as depicted in Fig. 1(a), is the sum of the power dissipation of two diodes and an IGBT as:

$$p_{c,B}(t) = [V_t + R_t I^{\beta}(t)]I(t) + 2.[V_D + R_D I(t)]I(t) = (V_t + 2V_D)I(t) + R_t I^{\beta+1}(t) + 2R_D I^2(t). \tag{17}$$

where, V_t, V_d and V_D are the threshold voltages of the IGBT, antiparallel diode and diode for the bidirectional switch while R_t, R_d and R_D are their corresponding on-state resistances. The parameter β is a constant directed by the IGBT characteristics. Considering $x(t)$, $y(t)$ and $z(t)$ are the number of conducting bidirectional switch, unidirectional switch and antiparallel diodes at any instant that depends on the inverter output voltage levels or switching signal, decoded pulse pattern, direction of current and the power factor of the load connected. The average value of the conduction loss for all the switches of each phase with a load current of $I(t) = I_L \sin(\omega t)$ can be expressed as:

$$P_{c,avg} = \frac{1}{\pi}\left(\int_0^{\pi} x(t).p_{c,B}(t)\,d(\omega t) + \int_0^{\pi} y(t).p_{c,T}(t)\,d(\omega t) + \int_0^{\pi} z(t).p_{c,t}(t)\,d(\omega t)\right) \tag{18}$$

MATLAB/Simulink based model of the proposed inverter has been developed to evaluate the conduction loss. The proposed inverter is considered to deliver output power of 1.9 kW. A three-phase star connection R-L load (45 Ω–55 mH/Phase) is used for the experimentation and analysis. The NLC technique at $m_i = 1$ is implemented to generate the appropriate gate signals. The on-state resistance of IGBT, antiparallel diode and diode for bidirectional switches are calculated from their data sheet values as $R_t = .0125\ \Omega$, $R_d = 0.019\ \Omega$ and $R_D = 0.07\ \Omega$ respectively. The voltage drop of IGBT,

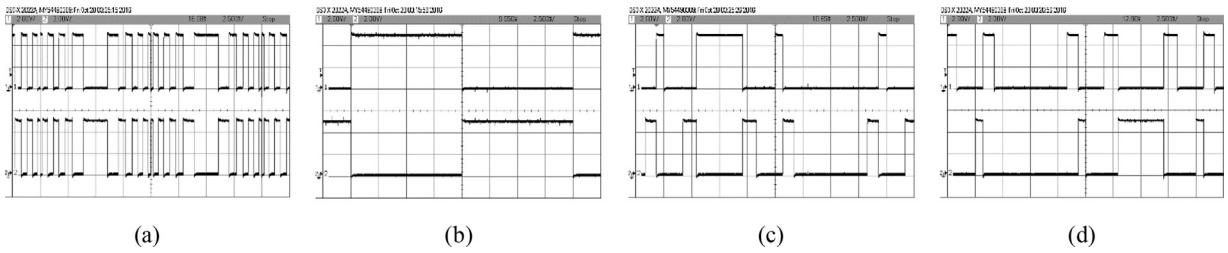

Fig. 6. Gate pulses of inverter switches for inverter (a) section-II ($T_{II,a1}$& $T'_{II,a1}$), (b) section-III ($T_{III,a}$& $T'_{III,a}$), (c) & (d) section-I ($T_{I,a1}$ & $T_{B,a1}$) and ($T_{B,a2}$ & $T_{I,a2}$).

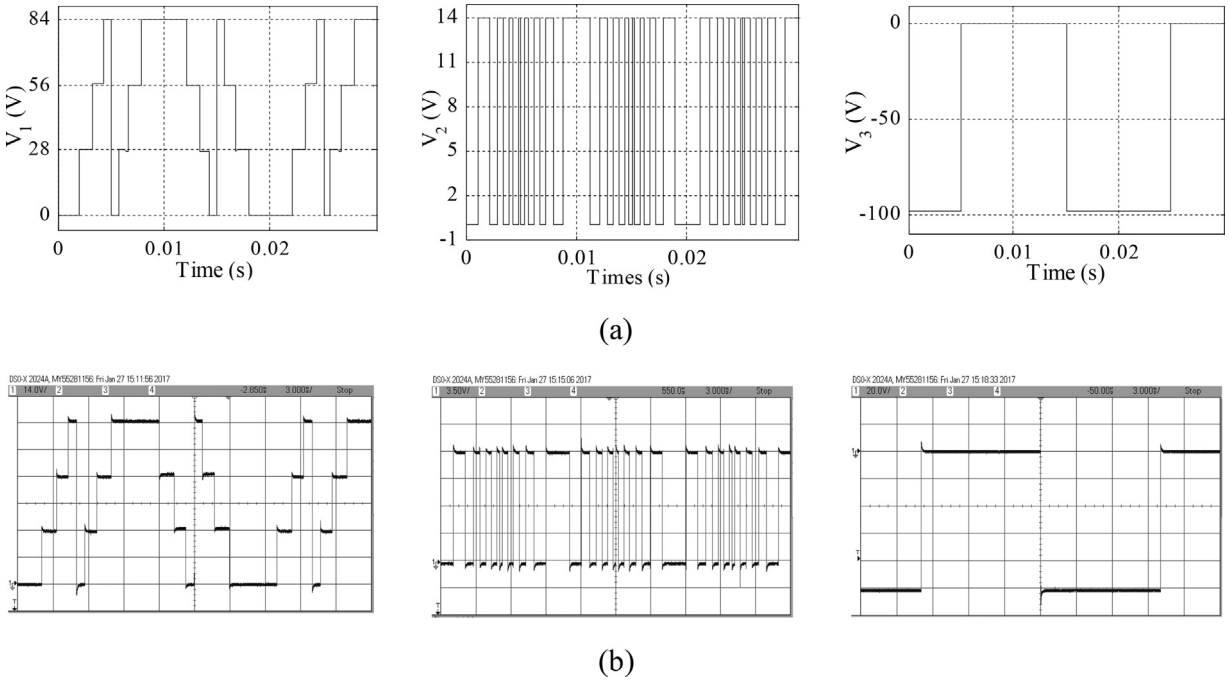

Fig. 7. The waveforms of voltage across the inverter section-I (V_1), section-II (V_2) and section-III (V_3) (a) simulation results and (b) experimental results.

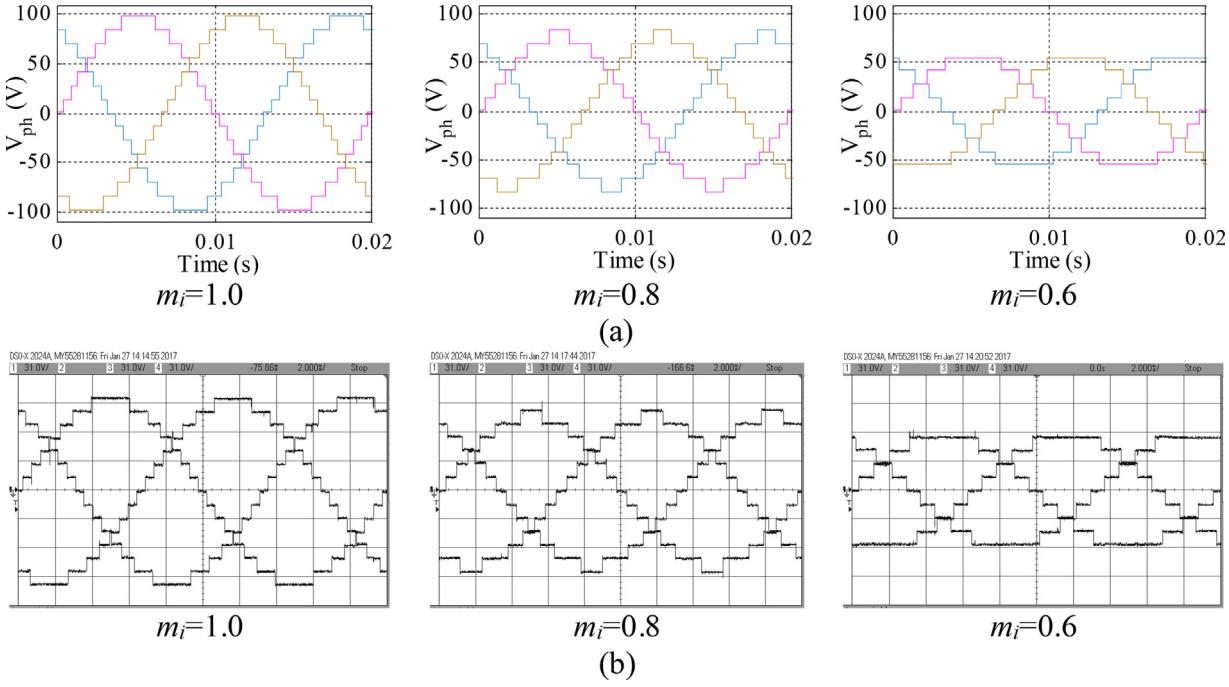

Fig. 8. The output phase voltages of the proposed three-phase fifteen-level inverter at different m_i (a) simulation results and (b) experimental results.

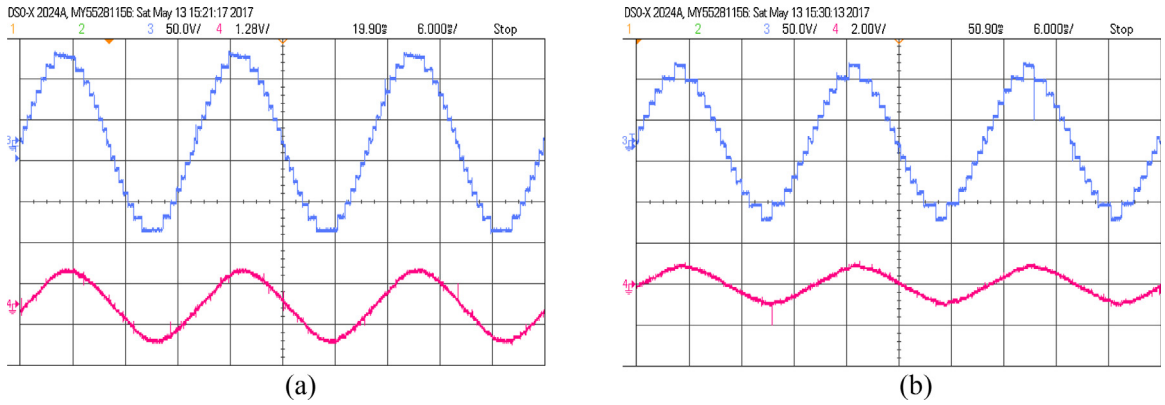

Fig. 9. The phase voltages and current of the proposed three-phase fifteen-level inverter at (a) $m_i = 1$ and (b) $m_i = .8$.

Table 4
Rating of the switches of proposed and the existing topology for *L*-level.

	Proposed inverter				NPC	FC	CHB
	Section-I		Section-II	Section-III			
	$T_{I,x1}$–$T_{I,x2}$	$T_{B,x1}$–$T_{B,x(m-1)}$	$T_{II,x(j+1)}$	$T_{III,X}$			
Voltage rating of switches of phase *x*. *x* = (a,b,c)	$\frac{m(L+1)V_{DC}}{2(m+1)}$	$\frac{(m-j)(L+1)V_{DC}}{2(m+1)}$ $j = 1,\ldots(m\text{-}1)/2$ for m is odd. $j = 1,\ldots, m/2$ for even m.	$2^j V_{DC}$ For $j = 0,\ldots$ $\ldots \frac{(L+1)}{4(m+1)}$	$\frac{(L-1)V_{DC}}{2}$	V_{DC}	V_{DC}	V_{DC}

antiparallel diode and diode for the bidirectional switches are assumed as $V_t = 1.25$ V, $V_d = 2.2$ V and $V_D = 1.5$ V respectively. Fig. 5 depicts the comparison of the conduction loss per phase of the proposed inverter with the asymmetrical CHB of suitable voltage ratios to obtain different possible voltage levels (*L*) with the implementation of the proposed NLC technique. It is observed from Fig. 5 that, the conduction loss of the proposed inverter is always lesser than the asymmetric CHB.

Further, to demonstrate the cost of the proposed MLI, the device rating is being calculated in this proposed work for *L*-level inverter considering a step voltage of the V_{DC}. The Table 4 demonstrates the rating of the switches for the proposed generalized inverter as well as the rating of the switches used in some of the classical MLI topologies such as CHB, FC and NPC. It's observed from Table 4 that, the proposed inverter employs few switching devices with a comparatively higher voltage rating resulting high-cost per-switch. Since the topology needs a considerably reduced number of switches, driver-circuits, isolated power sources and the diodes, the semiconductor device expenses are substantially recovered.

6. Simulation and experimental results

The exhaustive simulation and experimental results for the proposed fifteen-level MLI have been presented under different modulation index (m_i) using the nearest level control technique. A MATLAB/Simulink based modelling of the proposed three-phase inverter is carried out for the analysis and corresponding laboratory prototype for a specimen fifteen-level inverter is developed. Many other techniques in different fields [31–36] have been successfully applied in performing simulations to justify the choice of MATLAB environment. The NLC based control algorithm has been implemented in real-time using DS1103 due to its availability in the laboratory. The experimental results of the gate pulses of the inverter switches for 'phase-a' is shown in Fig. 6.

For simulation as well as for experimental verification of the proposed MLI, the values of DC link voltages for the specimen three-phase fifteen-level inverter are considered as $E_I = 28$ V, $E_{II} = 14$ V, and $E_{III} = 98$ V. The above isolated voltages are realised from the AC source with multi-winding transformer rectifier and filter capacitors. The simulation and experimental voltage response of section I, II and III (V_1, V_2 and V_3) of inverter 'phase-a' is shown in Fig. 7. From Figs. 6 and 7, it is observed that, the switching frequency of switches of inverter section-II ($T_{II,a1}$ & $T'_{II,a1}$) is relatively high with lesser voltage stress (as observed in Fig. 7). Whereas, the switching frequency of switches of inverter section-III ($T_{III,a}$ & $T'_{III,a}$) have a fundamental frequency with higher voltage stress and the switching frequency of switches of inverter section-I ($T_{I,a1}$ & $T_{B,a1}$, $T_{B,a2}$ & $T_{1,a2}$) have a comparatively lower switching frequency with low switching stress.

The simulation as well as the experimental results of the phase voltages for the proposed three-phase fifteen-level inverter are conducted at different modulation indexes (1.0, 0.8 and 0.6) as depicted in Fig. 8. It is observed from Fig. 8 that, the phase voltages are balanced in nature, having fifteen voltage levels at $m_i = 1$.

The experimental results of inverter phase voltage and phase current at different modulation index ($m_i = 1$ and 0.8) corresponding to the three-phase star connected R-L load ($R = 100\,\Omega$ and $L = 50$ mH/phase) is depicted in Fig. 9.

For the analysis purpose, the performances of the proposed three-phase inverter is compared with the exiting MLI topologies referred here in terms of number of switches, voltage sources and level of inverter as presented in Table 5. For further analysis, the number of phase voltage levels to switch ratio (LSR) and number of phase voltage levels to diode ratio (LDR) for a specimen twenty-three level inverter have been presented in Fig. 10(a). It is observed from Fig. 10(a) that, the value of LSR as well as LDR of the proposed MLI is better than that of the other MLI configurations. The dc source required to obtain a twenty-three voltage level is calculated from Table 5 and represented in Fig. 10(b) which is found noticeably lesser than the other popular topologies.

7. Conclusion

The paper demonstrated a new generalized three-phase hybrid multilevel inverter configuration with reduced number of switches and the DC sources. The optimal design of the proposed gen-

Table 5
Comparison of proposed three-phase MLI with existing multilevel inverters.

Existing topologies	Number of switches (N_{SW})	Number of separate DC supply/capacitors	Remarks
Babaei and Hosseini [2]	$3(L+3)$[b] $[6(\log_2(L+1)+1)]$[c]	$[3(L-1)/2]$[b] $[3\log_2(L+1)-1]$[c]	1. Separate dc source is required. 2. Asymmetrical (binary) MLI is possible.
Babaei et al. [3]	$3(L+1)$[b]	$[3(L-1)/2]$[b]	1. Required only bi-directional switches. 2. Asymmetrical MLI loses few voltage levels.
Nabae et al. [7]	$6(L-1)$	$[1+(I-1)$[a]$]$	1. Balancing of capacitor is required. 2. Unequal utilization of switches.
Meynard and Foch [8]	$6(L-1)$	$[1+(L-1)$[a]$]$	1. High switching frequency applications. 2. Requires large number of capacitors.
Marchesoni et al. [9]	$6(L-1)$[b] $4[\log_2(L+1)-1]$[c]	$[1.5(L-1)]$[b] $[\log_2(L+1)-1]$[c]	1. Extremely modular. 2. Required isolated source.
Masaoud et al. [10]	$[2L+8]$[b] $[2\log_2(L-1)+12]$[c]	$(L-1)$[b] $[1+\log_2(L-1)]$[c]	1. Most of the switches are of high rated.
Ebrahimi at al. [11]	$12+1.5(L-1)$	$1.5(L-1)$	1. Bidirectional switches are also required. 2. Only symmetrical configuration is possible.
Chattopadhyay and Chakraborty [12]	$3(L+1)$	$0.25(3L+1)$	1. All odd voltage levels can't be synthesized. 2. Applicable for medium voltage motor drive.
Hinago and Koizumi [13]	$[1.5(3L-1)]$[b] $[9\log_2(L+1)-6]$[c]	$1.5(L-1)$[b] $3[\log_2(L+1)-1]$[c]	1. Asymmetrical (binary) MLI is also possible. 2. Medium- and high-power applications.
Babaei et al. [14]	$1.5(L+9)$[b]	$1.5(L-1)$[b]	1. Non isolated course is required. 2. Considered asymmetrical cascaded MLI
Mekhilef et al. [15]	$3(\sqrt{4L-7}+1)$	$1.5\{\sqrt{(4L-7)}-1\}+1$	1. Isolated source is required. 2. Generate only even number of levels.
Raushan et al. [16]	$12+1.5(L-3)$	$[0.5(L-1)+3]$	1. One additional switch can create two extra voltage levels per phase. 2. Bidirectional switch is also required.
Choi et al. [17]	$3(L+1)$	$(L-1)$	1. Asymmetry is not possible. 2. Bidirectional switch is also required.
Vahedi et al. [18]	$3(2L-3)$	$(L-1)$	1. Asymmetrical MLI is not possible. 2. Bidirectional switch is also required.
Najafi et al. [19]	$3(L+3)$	$0.5(L-1)$	1. Asymmetrical MLI is not possible. 2. Required high rated switches for H-bridge.
Haiwen et al. [20]	$6(L-2)$	$1+[0.5(3L-5)]$[a]	1. Asymmetrical (binary) MLI is also possible. 2. Required large number of capacitors.
Gupta and Jain [22]	$6(L-1)$	$1.5(L-1)$	1. Asymmetrical MLI is also possible. 2. Bidirectional switches are also required.
Proposed topology	$3(m+3+2n)$	$[(+3)+3n]$	1 Bidirectional switches are also required. 2. Optimized m & n for reduced components

[a] DC sources realized by the capacitors.
[b] Symmetrical source configuration.
[c] Asymmetrical source configuration.

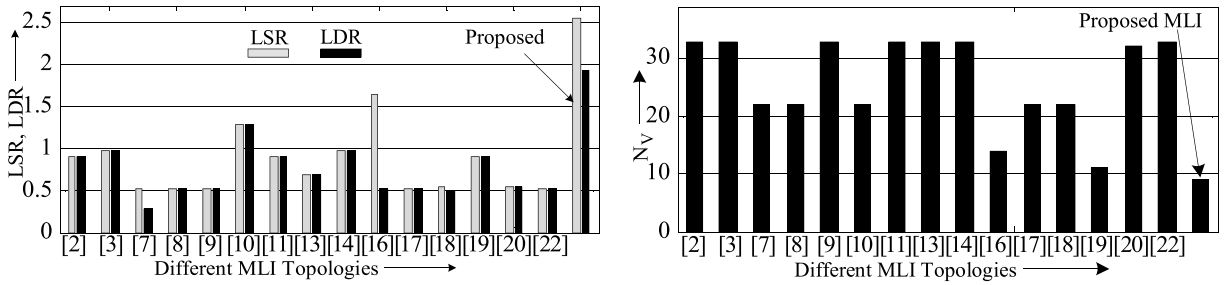

Fig. 10. Comparison of proposed MLI with different MLI configurations for $L=23$ in terms of (a) LSR and LDR and (b) number of DC source (N_V).

eralized MLI has been developed for any given number of switches and DC voltage sources using the generalized expressions developed. The optimum value of switches and voltage sources required to design the proposed three-phase inverter that generates maximum inverter voltage levels have been studied and plotted for various combinations of the above inverter components. The NLC based modulation technique have been developed for any voltage level and simulated for the three-phase fifteen-level inverter using MATLAB/Simulink platform and implemented in real-time using DS1103. Experiments have been conducted on a laboratory prototype of the proposed fifteen-level inverter for the R–L load. The experimental results corresponding to the different modulation index are also presented that verified the respective simulation results. The effectiveness of the proposed reduced switch three-phase MLI configuration have been studied by comparing the LSR, LDR and number of voltage source (N_V) of the proposed MLI with the other MLI configuration and it is found better than the existing MLIs presented here.

Appendix A.

The detail specification of the components for the proposed specimen three-phase fifteen- level inverter is given in Table A1.

Table A1
Specifications of the components.

Name of the components	IC number/specification	Qty.
Single-phase rectifier	KBPC2510	09
DC link filter capacitor	Alcon Electrolytic, 1600MFD, 200VDC	09
MOSFETs	IRFP460	24
Snubber circuit	10 Ω,10 W and 0.01 μF, 1000 V	24
Ultrafast diode	MUR1560	12
Common cathode dual diode	MUR1660CT	06
Opto-isolators	TLP250	24
Zenor diodes	1N4746, 18 V	24
DC link voltages, E_I, E_{II}, E_{III}	14 V, 28 V and 98 V	03

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