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Investigation of Single-Phase Multilevel Inverter Based on Series/Parallel-Connected H-Bridges

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***Abstract*—This paper investigates a multilevel inverter composed of series/parallel-connected H-bridges. The presented structure can be used for applications in which the use of semiconductor switches with low voltage and low current ratings is intended. A comprehensive system model, an overall control strategy to adjust the output voltage with constant magnitude and frequency, and a level-shifted PWM (LS-PWM) strategy based on a voltage vectors unidimensional analysis and a plane analysis are presented. The LS-PWM is capable of mitigating the low-frequency circulating current, thus generating multilevel voltage signals with low harmonic distortion, maximum number of levels, and low dv/dt. In addition, considering a wide range of values of voltages and currents and various power levels, the total converter losses are reduced compared with conventional multilevel converters. Two multilevel conventional inverters with the same number of semiconductor switches are used for comparison. Simulation and experimental results demonstrate the feasibility of the studied converter.**

I. Introduction

INDUSTRIAL applications require power converters with high-power levels. Semiconductor switches to process high-level voltage or current are not always available in the trade or, if they are, they may be very expensive, increasing the system cost. In this context, multilevel converters have been greatly recognized as a solution to employ low-power-rating switches in medium- and high-power applications [1]–[5].

In technical literature, there are three types of classic multilevel topologies: (i) neutral-point-clampled (NPC) converter [6], (ii) flying capacitor (FC) converter [7], and (iii) cascaded H-bridge (CHB) converter [8], [9]. NPC and FC topologies are composed of a single dc-source and legs with series-connected semiconductor switches, while CHB converters provide a large number of levels by simply connecting multiple single-phase converter modules with multiple dc-sources [10], [11]. Modules with low-voltage-rating switches are typically more efficient and cheaper than the high-voltage ones.

On the other hand, by connecting the modules in parallel, the system realiability and redundancy are increased [12]. However, the parallel connections create a path between the different modules and circulating currents appear. One simple way of eliminating these currents is making use of an isolation transformer, but the weight, size and cost associated with the transformer may be considered a drawback. Therefore, alternative solutions to mitigate the circulating currents based on control strategies and connection of inductors between the converters were discussed in [13]–[15].

Thus, by connecting switches (like NPC and FC topologies) or converter modules (like CHB topology) in series, it is possible to share the total dc-link voltage among them, reducing the voltage rating as well as the switching semiconductor losses. On the other hand, by connecting converter modules in parallel, it is possible to share the total current among them, reducing the current rating. So, series connections are indicated for medium- and high-voltage applications, whereas parallel connections are recommended for medium- and high-current applications. Multilevel voltages are generated with both types of connection [16]–[20], thus reducing the harmonic distortion when compared to conventional two-level converters.

Phase-shifted pulsewidth modulation (PS-PWM) and level-shifted PWM (LS-PWM) strategies use high-frequency triangular carriers. In the paper, a space-vector PWM (SV-PWM) based on LS-PWM modulation is presented. The LS-PWM uses level-shifted carriers to determine the converter switching states. The LS-PWM is generally chosen for multilevel converters, where the number of level-shifted carriers is the number of possible levels minus one. The PS-PWM strategy is most commonly used in systems with parallelism. The number of phase-shifted carriers corresponds to the number of parallel paths of the converter. The triangular carriers are shifted from each other following the ratio $360^\circ/\mathrm{M}$ (where M is the number of parallel paths of the converter) [1]–[4]. In this work, the PS-PWM and LS-PWM strategies are used together, since a multilevel system with series and parallel connections is proposed.

This paper aims to determine the range of power levels of ac-loads by using a series/parallel converter to divide the total load voltage and total load current. The analysis takes into account the harmonic distortion and semiconductor losses of the studied topology. These characteristics are compared with the conventional solutions.

Fig. 1 shows a proposed topology that connects H-bridge modules in series and subsequently the branches formed by the series-connected modules are connected in parallel [21]. This

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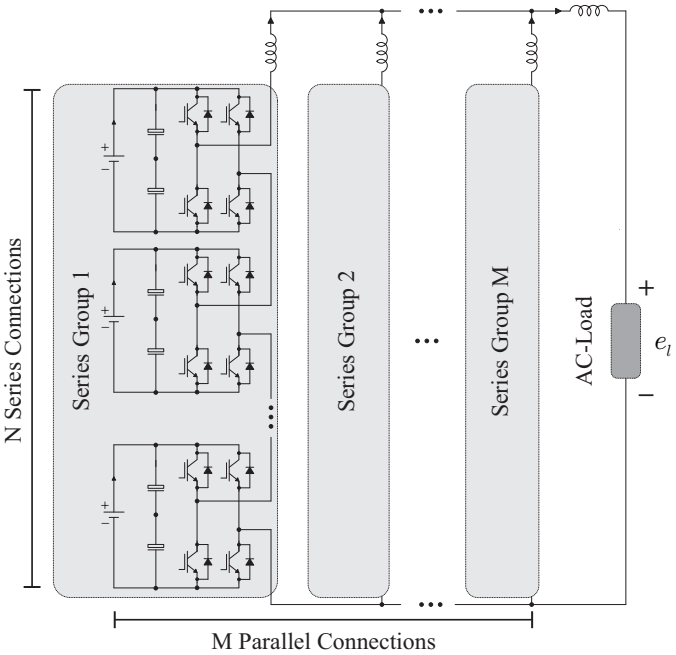

Fig. 1: Generalized schematic diagram of the proposed system.

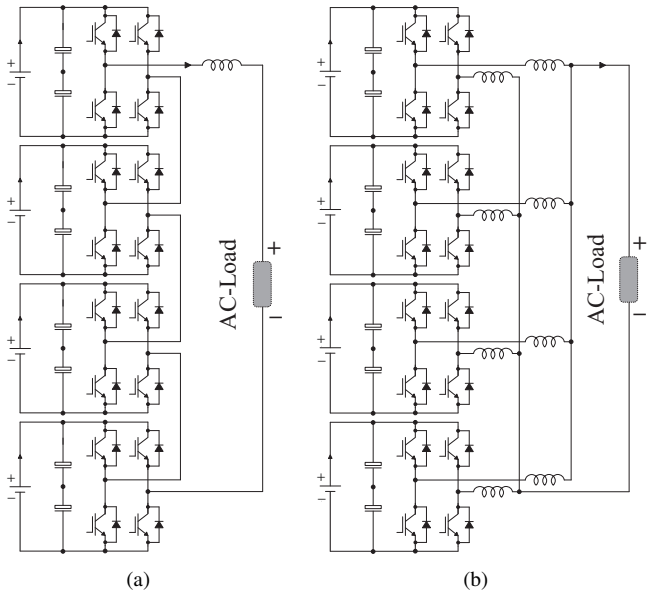

Fig. 2: Schematic diagram of conventional systems. (a) Series system - S-4HB. b) Parallel system - P-4HB.

topology takes advantage of both series and parallel modules, especially sharing the total voltage and current among them, reducing voltage and current ratings simultaneously. The generalized circuit is composed of M parallel connections of N series H-bridges. This topology uses semiconductor switches with nominal voltage N times lower than the load voltage and nominal current M times lower than the load current, thus reducing the semiconductor losses in a range of power levels without reducing the power quality of the generated voltages in comparison to conventional converters.

Fig. 2(a) illustrates the conventional series converter (classical cascaded H-bridge converter) composed of four H-bridges, named here S-4HB. Fig. 2(b) shows the conventional parallel converter employing the same number of H-bridges, named here P-4HB. This paper discusses in which scenarios the use of only series, only parallel and series/parallel converters are suitable. As aforementioned, series converters should be used in medium- and high-voltage applications, while parallel converters should be used in medium- and high-current applications. However, there is a range of power where, independently of the power level, the use of series/parallel converters is more adequate.

In order to make the system analysis clearer, this work presents the case in which semiconductor switches process half the voltage and half the current of the load, i.e., M = N = 2, totalizing four H-bridges, which is the same number of H-bridges employed by the conventional topologies. Considering the same load conditions, the proposed configuration may reduce the control complexity and semiconductor current levels when compared with the conventional converter S-4HB, and also reduces the number of inductors and circulating currents, and the semiconductor voltage levels when compared with the conventional converter P-4HB. Fig. 3 shows the proposed series/parallel-connected inverter with four dc-links, named SP-4HB. This configuration provides a single path for a circulating current, that can be minimized with a proper PWM strategy, as will be shown in this paper.

Two important tasks are performed by the proposed converter: (i) providing sinusoidal voltage with constant magnitude and frequency and (ii) providing low-frequency circulating current controlled close to zero to avoid imbalances. A level-shifted PWM (LS-PWM) strategy is used to obtain the output converter voltage with maximum number of steps, leading to signals with low harmonic content.

II. Model of the Studied System

The proposed configuration SP-4HB, shown in Fig. 3, comprises four series/parallel-connected H-bridges, each one with a dc-link capacitor bank powered by an isolated dc-supply with voltage v_{Ck} and controlled by switches q_{ka} and q_{kb}, with $k = 1, 2, 3, 4$. For better understanding, these H-bridges are named HB1, HB2, HB3 and HB4. The switching conduction state is represented by a homonymous binary variable, e.g., $q_{1a} = 1$ indicates closed switch, and $q_{1a} = 0$ indicates the switch is open. Switches q_{ks} and $\overline{q}_{ks}$ are complementary $(s = a, b)$.

The inductors of the proposed structure can be distributed as shown in Fig. 4. For a low-switching-frequency application, the internal currents may have large ripple, so internal parallel inductors (L_{p1} and L_{p2}) with larger inductances can be required to decrease this ripple. When high switching frequency is used, internal inductors with low inductances may be employed. Fig. 4(a) shows an equivalent inductance to be considered, L_{eq}. The internal parallel inductors can be equal to double of L_{eq} (see Fig. 4(b)) if the main objective is suppress the ripple, or they can be distributed as shown in Fig. 4(c), $L_{p1}/2 = L_{p2}/2 = L_f = L_{eq}/2$, if internal parallel inductors with larger inductance represents a problem.

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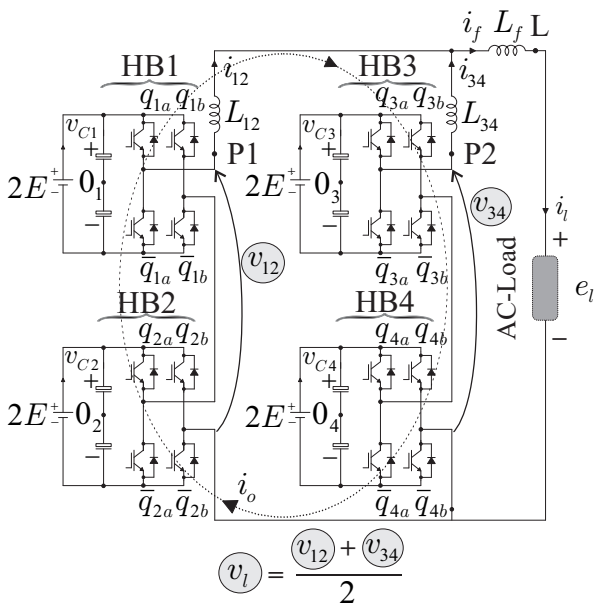

Fig. 3: Schematic diagram of series/parallel system with M = 2 and N = 2 – SP-4HB.

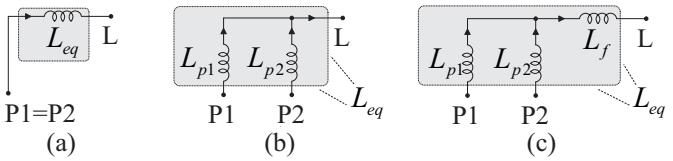

Fig. 4: Inductors arrangement.

By applying Kirchhoff's voltage law to equivalent circuit of configuration SP-4HB, illustrated in Fig. 5, the following relations can be obtained:

$$e_l = L_f i_f + L_{12} i_{12} + v_{12} \quad (1)$$

$$e_l = L_f i_f + L_{34} i_{34} + v_{34} \quad (2)$$

where $v_{12} = v_1 + v_2$ and $v_{34} = v_3 + v_4$ are the series voltages, v_k is the output voltage of H-bridge k, $L_x = r_x + l_x \frac{d}{dt}$, and the symbols r_x and l_x represent the resistances and inductances of the inductors L_x with $x = f, 12, 34$.

The H-bridges voltages are defined by $v_k = v_{ka0_k} - v_{kb0_k}$, where v_{ka0_k} and v_{kb0_k} are the pole voltages of H-bridge k, which depend on the switching states (q_{ka} and q_{kb}) and on the dc-link voltage $2E$, resulting in

$$v_{ks0_k} = (2q_{ks} - 1)E. \quad (3)$$

Considering a balanced and symmetric system ($L_{12} = L_{34} = 2L_f$), and summing (1) and (2), it is possible to obtain

$$2e_l = 2L_f i_f + 2L_f i_{12} + 2L_f i_{34} + v_{12} + v_{34} \quad (4)$$

which is simplified as follows

$$e_l = L_{eq} i_f + v_l \quad (5)$$

where $L_{eq} = 2L_f$, $i_f = i_{12} + i_{34}$ and $v_l = (v_{12} + v_{34})/2$.

To determine the voltage that defines the circulating current,

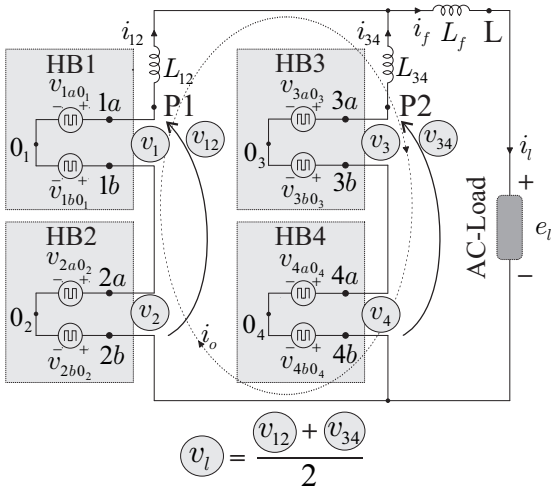

Fig. 5: Equivalent circuit of proposed configuration – SP-4HB.

the following equation can be derived by (1) minus (2)

$$0 = L_{eq} i_{12} - L_{eq} i_{34} + v_{12} - v_{34}. \quad (6)$$

Considering the influence of the circulating current, i_o, the internal currents can be defined by

$$i_{12} = i_f/2 + i_o \quad (7)$$

$$i_{34} = i_f/2 - i_o. \quad (8)$$

Substituting (7) and (8) in (6)

$$0 = 2L_{eq} i_o + v_{12} - v_{34} \quad (9)$$

the voltage that defines the circulating current is

$$v_o = v_{12} - v_{34} = -2L_{eq} i_o. \quad (10)$$

Finally, from v_l and v_o the series voltages, v_{12} and v_{34}, are

$$v_{12} = v_l + v_o/2 \quad (11)$$

$$v_{34} = v_l - v_o/2. \quad (12)$$

From the control point of view, controllers define the reference voltages v_l^* and v_o^* to control the load voltage e_l and the circulating current i_o, respectively. More details about the control system will be discussed in Section IV. The symbol asterisk (*) is used for reference variables.

III. LS-PWM Strategy

The presented LS-PWM strategy is based on vector analysis in v_o x v_l planes, as observed in the Fig. 6. Fig. 6(a) shows the symmetrical case. In this case making $v_o = 0$, voltage v_l can assume the following five levels: $-4E$, $-2E$, 0, $2E$, and $4E$. Four additional levels ($-3E$, $-E$, E, and $3E$) can be generated when $v_o \neq 0$. Additionally, a scenario where the proposed converter operates with different dc-link voltages is illustrated in Fig. 6(b). Considering an asymmetrical condition in which $2v_{C1} = v_{C2} = 2v_{C3} = v_{C4} = 4E$, the series/parallel converter can generate the output voltage with up to seven levels ($-6E$, $-4E$, $-2E$, 0, $2E$, $4E$, and $6E$) when $v_o = 0$ and up to thirteen levels making $v_o \neq 0$. Symmetric operation is more suitable for high-power applications in order to evenly

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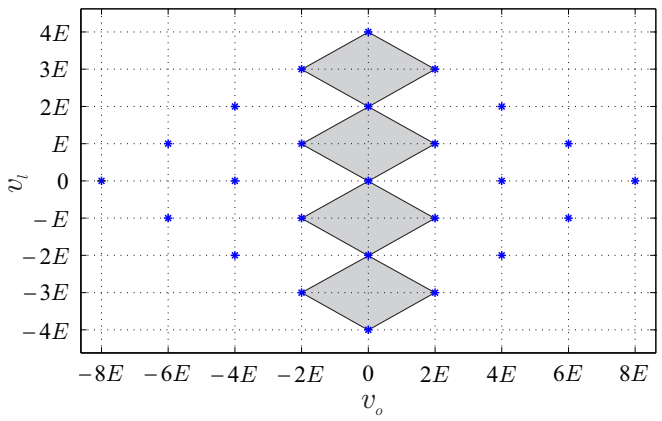
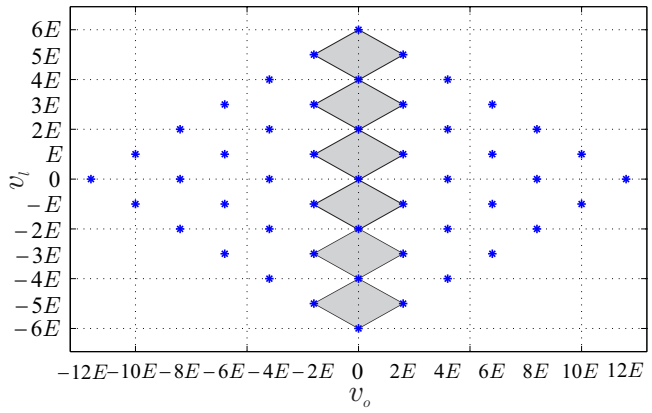


(a)



(b)

Fig. 6: Vector analysis – v_o x v_l planes. (a) Symmetrical case $v_{C1} = v_{C2} = v_{C3} = v_{C4} = 2E$. (b) Asymmetrical case $2v_{C1} = v_{C2} = 2v_{C3} = v_{C4} = 4E$.

divide the voltage levels between the modules and use low-rating semiconductors. Asymmetric operation can be used in low- and medium-power applications to increase the number of levels and minimize distortions in the voltages and currents generated by the converter. In this case, the converter are composed by low and medium-power switches [22].

In this section, a LS-PWM strategy for the investigated series/parallel configuration operating with equal dc-supply voltages, $2E$, is described with the objective of obtaining the maximum number of steps in the output voltage, without causing current imbalances when $v_o \neq 0$. It is also possible to carry out a similar analysis in a scenario of asymmetrical dc-link voltages. The output converter voltage with symmetrical and asymmetrical dc-link voltages will be shown in Section VII. The condition with equal dc-link voltages will be detailed.

In Fig. 6, each vertex represents a vector formed by a sequence of numbers that indicate the states of each H-bridge of the converter SP-4HB. The H-bridge states are defined as 0, 1, 2, and 3, that represent the decimal number equivalent to the upper switches states of each H-bridge. This information is presented in Table I, where the output voltage values, v_k, synthesized by the respective H-bridge are also shown.

Considering the definitions shown in the Table I, the vectors in plane are formed by a sequence with four positions,

TABLE I: Selecting switching states and H-bridge voltages in symmetrical case

q_{ka}	q_{kb}	v_k	HBk state
0	0	0	0
0	1	$-2E$	1
1	0	$2E$	2
1	1	0	3

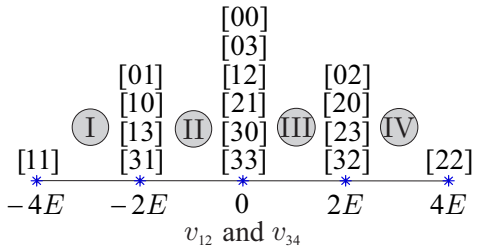


Fig. 7: Unidimensional vector analysis – v_{12} and v_{34} line.

e.g. [2031], which represents the following H-bridge states: HB1→2, HB2→0, HB3→3, HB4→1. It means that this vector generates $v_{12} = v_1 + v_2 = 2E$ and $v_{34} = v_3 + v_4 = -2E$. Consequently, by equations (5) and (9), the converter output voltage is $v_l = 0$ and the voltage $v_o = 4E$. The vectors [2020] and [2002] are redundant, since they provide the same v_l value and v_o value ($v_l = 2E$ and $v_o = 0$).

The v_o x v_l vector plane contains 4^4 vectors, including all redundancies. In order to simplify the analysis, Fig. 7 shows a line with 4^2 possible vectors that generate the series voltages v_{12} and v_{34}. Five non-redundant vectors should be selected to obtain the lower switching. In this unidimensional analysis, the line is subdivided into four sectors (I, II, III, IV), where high-frequency triangular carriers are defined. In this line, the vectors are formed by a sequence of two positions, e.g. [01], which represents the following H-bridge states: HB1→0, HB2→1 to voltage v_{12}, and HB3→0, HB4→1 to voltage v_{34}. The decimal numbers of the line vector are defined by the H-bridge states that generate the series voltages v_{12} (HB1 and HB2) or v_{34} (HB3 and HB4) with five levels ($-4E$, $-2E$, 0, $2E$, and $4E$). Using LS-PWM carriers with the same phase for each series voltage reference, the generated voltage v_l will have five levels and v_o will be null during all the time, as can be seen in Figs. 8(a) and 8(c). The sequence of selected vectors is applied in a sampling period, T_{sw}.

To obtain the additional four levels, it is necessary to make $v_o \neq 0$. However, this fact can introduce low-frequency circulating currents between the H-bridges of the converter. In order to obtain the additional four levels to voltage v_l and to mitigate the low-frequency circulating current, the reference voltages of each series group, v_{12}^* and v_{34}^*, are compared with high-frequency triangular carriers with different levels and mutually shifted by 180°, as illustrated in Figs. 8(b) and 8(d). In others words, the reference voltage of HB1 and HB2, v_{12}^*, must be compared to the LS-PWM carriers with 0°, while the reference voltage of HB3 and HB4, v_{34}^*, must be compared to the LS-PWM carriers with 180°. Thus, the v_o average value is

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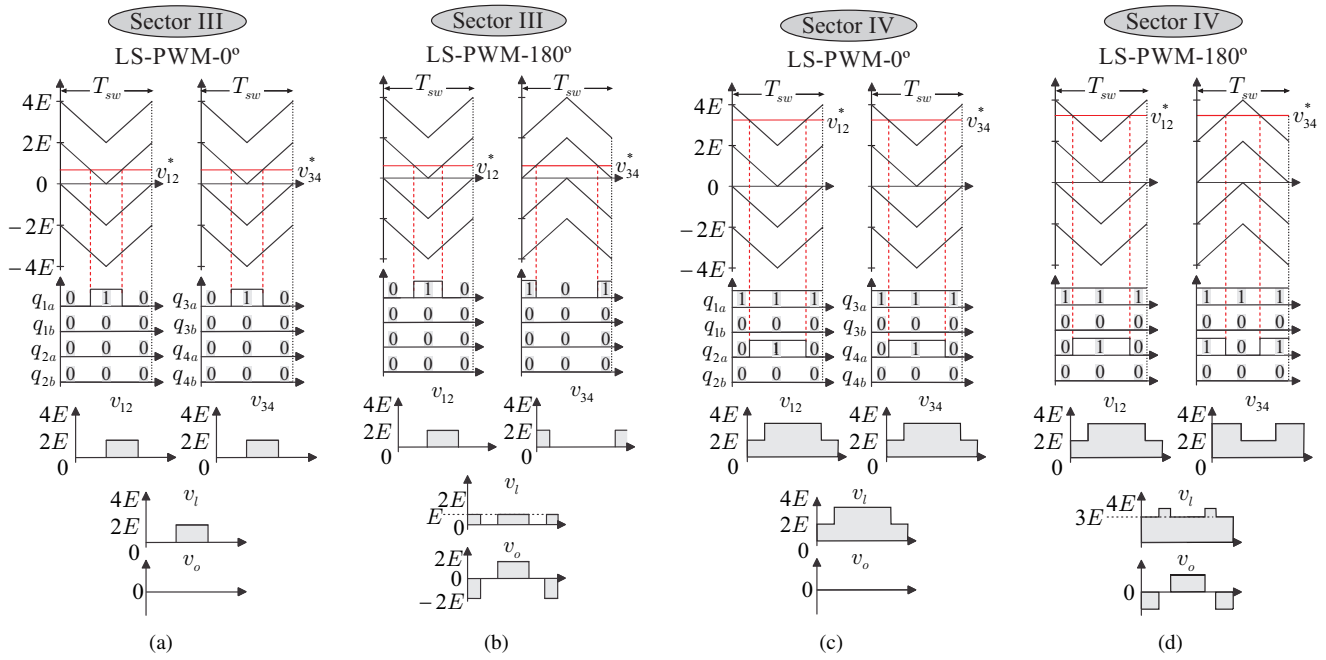

Fig. 8: Pulse pattern of PWM implementation of the series branches of the proposed series/parallel converter. (a) Sector III – LS-PWM-0°. (b) Sector III – LS-PWM-180°. (c) Sector IV – LS-PWM-0°. (d) Sector IV – LS-PWM-180°.

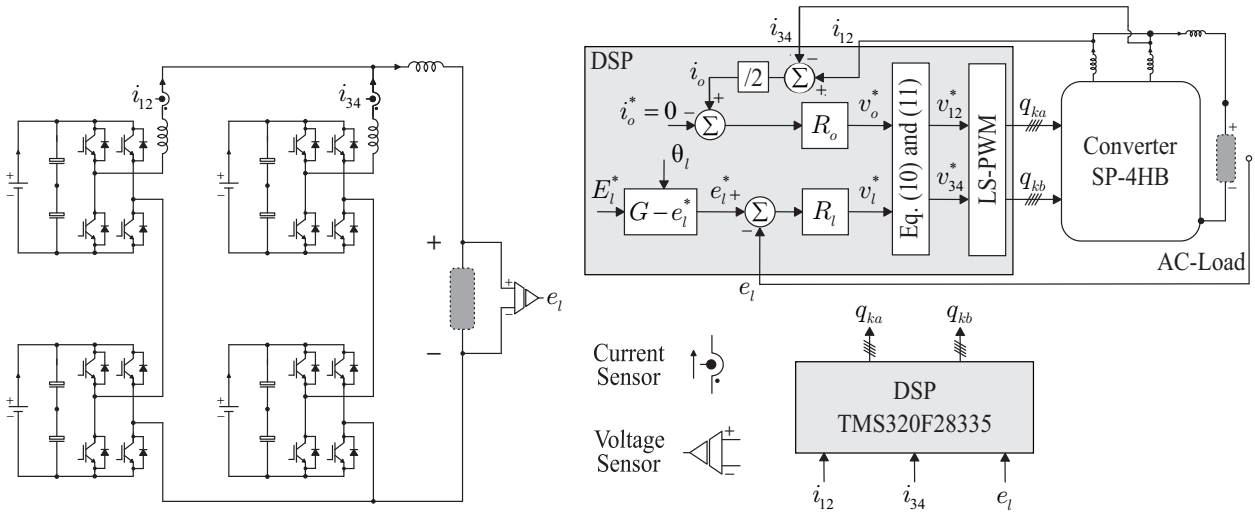

Fig. 9: Control block of topology SP-4HB.

kept null in a sampling period and, additionally, the generated v_l becomes a nine-level voltage (against the five-level one obtained when all carriers are in phase) and presents lower dv/dt.

Therefore, the average voltage v_o is zero in each sampling period and the use of carriers shifted by $180°$ enables the reduction of load current ripple and distortion [23]. Using the described LS-PWM strategy, low harmonic distortion for the proposed topology output voltage can be obtained.

IV. Overall Control Strategy

Fig. 9 shows the control diagram of topology SP-4HB. The sinusoidal reference load voltage is generated by the block $G-e_l^*$, which receives the reference voltage amplitude E_l^* and the voltage angle θ_l. This reference signal is compared with the measured value, e_l, and its error $(e_l^* - e_l)$ is set to zero by the controller R_l (a positive-negative PI controller [24]), which defines the converter reference output voltage v_l^*. Additionally, the circulating current, i_o, is measured according to (7) and (8). The circulating low-frequency current must be controlled close to zero. In this way, the positive-negative PI controller R_o receives the error of circulating current $(i_o - i_o^*)$ and generates the reference voltage v_o^*. In the block LS-PWM, the series voltages v_{12}^* and v_{34}^* are compared with LS-PWM carriers shifted by $180°$, as previously explained, and the switching states are defined. The topology SP-4HB generates voltages with the maximum number of levels that the structure can provide and the low-frequency voltage v_o is made zero.

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V. Harmonic Distortion

The harmonic distortion of the studied topologies (S-4HB, P-4HB, and SP-4HB) has been evaluated by calculating the total harmonic distortion (THD) of the converter internal (i_{12} and i_{34}) and output (i_l) currents and the weighted total harmonic distortion (WTHD) of the converter output voltage (v_l).

The THD is defined as

$$\text{THD}(h) = \frac{100}{\alpha_1}\sqrt{\sum_{h=2}^{N_h}\alpha_h^2} \tag{13}$$

and the WTHD is defined as

$$\text{WTHD}(h) = \frac{100}{\alpha_1}\sqrt{\sum_{h=2}^{N_h}\left(\frac{\alpha_h}{h}\right)^2} \tag{14}$$

where α_1 is the amplitude of the fundamental component; α_h is the amplitude of h^{th} harmonic component; and N_h is the number of harmonics to be considered for the calculation of THD and WTHD and h is the harmonic order ($N_h = 1000$).

For simulation results, including the analysis of harmonic distortion and semiconductor losses (section VI), the following parameters to conventional and proposed configurations are considered: (i) magnitude of the load voltage, $E_l = 1200$ V; (ii) load power, $P_l = 3.5$ kW – 30 kW; (iii) load power factor $pf_l = 0.90$, (iv) average switching frequency, $f_{ave-sw} = 2.50$ kHz; and (v) modulation index, $m = 0.98$.

Table II shows the harmonic distortion values obtained for output variables (v_l and i_l) in all structures. These results were obtained selecting the same average switching frequency value ($f_{ave-sw} = 2.5$ kHz) for all topologies, and applying the switching states aiming at switching losses reduction. It can be observed that all the structures have equivalent values of harmonic distortion in the output variables of the converter. In this scenario, considering the frequencies of the LS-PWM carriers of the SP-4HB, S-4HB e P-4HB topologies being f_{sw-SP}, f_{sw-S}, and f_{sw-P}, respectively. In order to obtain the same average switching frequency, the following relationship between them must be respected: $f_{sw-S} = 2f_{sw-SP} = 4f_{sw-P}$. Since the topology SP-4HB is capable of maintaining the same harmonic distortion levels for the load current and the load voltage over conventional configurations, additional advantages of the proposed structure are highlighted in the semiconductor losses analysis (see Section VI).

It is important to maintain the same average switching frequency for all topologies, so that the comparison between them can be fair. As a converter operates at higher switching frequency, there is a tendency for this converter to have lower harmonic distortion values.

Each multilevel branch generates five-level voltages in the proposed topology considering the symmetrical case, while in the conventional parallel topology, three-level voltages are generated in each parallel H-bridge. Consequently, the THD of the internal currents is higher in topology P-4HB than in topology SP-4HB. This fact can be noted in Fig. 10, which shows the THD of the internal currents of converters SP-4HB and P-4HB for different values of average switching frequency.

TABLE II: Voltage and currents WTHD/THD analysis

Topology	WTHD (%) v_l	THD (%) i_l	f_{ave-sw} (kHz)	f_{sw} (kHz)
SP-4HB	0.0306	0.3282	2.5	10.0
S-4HB	0.0306	0.3287	2.5	20.0
P-4HB	0.0306	0.3285	2.5	5.0

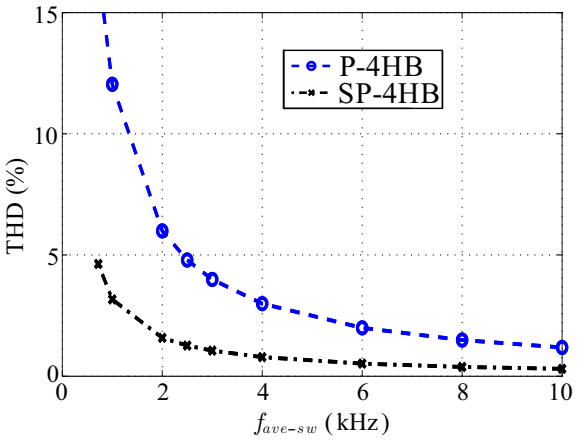

Fig. 10: THD of internal currents – SP-4HB and P-4HB.

Considering the same average switching frequency, the harmonic distortion in the two-level converter (2L) is greater than in the converters that use series- and/or parallel-connected converter modules. In terms of costs with semiconductor switches, the series/parallel configuration is also more cost-effective compared to the converter solution 2L since it uses high-power-rating semiconductor switches. While the configuration SP-4HB uses sixteen switches, the configuration 2L uses four switches. In order to compare the two structures, Table III shows the costs with the semiconductor switches between the proposed series/parallel topology and the two-level solution (high-power H-bridge) [25], [26].

Four different types of load were used. The relationship E_l/I_l of the loads are within the zone where the series/parallel structure is presented as solution. They are: (i) load 1 - E_l = 1200 V and I_l = 12 A; (ii) load 2 – E_l = 1200 V and I_l = 32 A; (iii) load 3 – E_l = 3000 V and I_l = 24 A; and (iv) load 4 - E_l = 3000 V and I_l = 80 A. In all the scenarios shown, the series/parallel configuration has lower costs than the option that uses high-power-rating switches. Even with prices varying each day, converters that use switches with low power rating are widely studied in the technical literature. This fact indicates lower costs associated with the advantages that the series or parallel associations provide to the operation of these systems [1], [2], [4].

VI. Semiconductor Losses

The loss estimation is obtained by using the technique presented in [27]. The semiconductor switch used in the tests was: insulated-gate bipolar transistor (IGBT) with dual module CM50DY-24H (POWEREX) drive SKHI23 (SEMIKRON). The switch loss model includes: IGBT and diode conduction losses, IGBT turn-on losses, IGBT turn-off losses and diode

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TABLE III: Comparison of costs with semiconductor switches: proposed converter SP-4HB *versus* high-power H-bridge

	Load 1 (1.2 kV and 12 A)		Load 2 (1.2 kV and 32 A)		Load 3 (3.0 kV and 24 A)		Load 4 (3.0 kV and 80 A)	
Converter	SP-4HB	HP-2L	SP-4HB	HP-2L	SP-4HB	HP-2L	SP-4HB	HP-2L
Manufacturer	ON[1]	IXYS	ON	IXYS	IXYS	IXYS	IXYS	IXYS
Switch voltage rating (V)	600	1200	600	1200	1700	3000	1700	3000
Switch current rating (A)	6	12	16	32	12	30	40	80
Price/switch (USD)	0.38	2.55	0.98	10.00	4.55	26.40	9.71	41.54
Total price (USD)	6.08	10.20	15.68	40.00	72.80	105.60	155.36	166.16

[1]ON Semicondutor

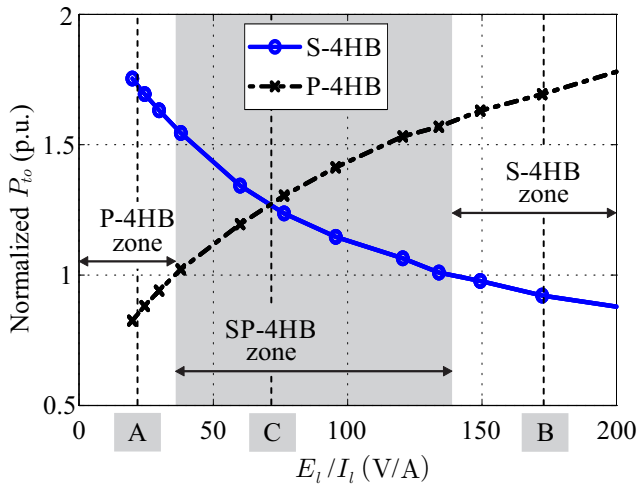

Fig. 11: Normalized semiconductor total losses – comparison of proposed and conventional topologies – E_l/I_l x P_{to}.

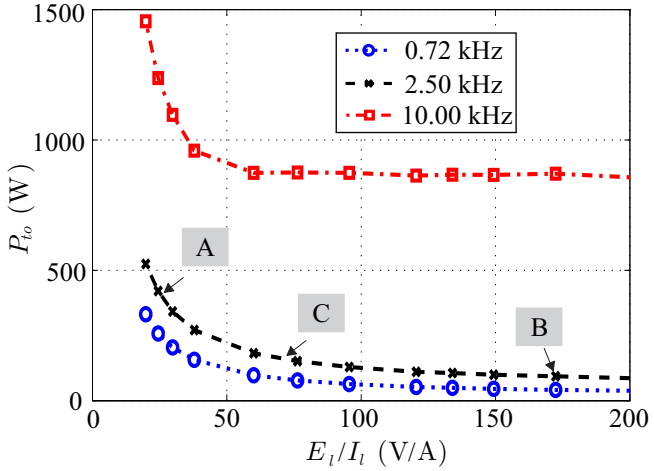

Fig. 12: Total losses of proposed topology, SP-4HB, for $f_{ave-sw} = 0.72$, 2.50, and 10.00 kHz – E_l/I_l x P_{to}.

turn-off energy. These results were obtained by fixing the value of the load voltage at 1200 V and varying the value of the load current from 6 A to 50 A.

Fig. 11 shows the normalized semiconductor total losses (P_{to}) as a function of the relationship between voltage and current load amplitudes, E_l/I_l, for conventional topologies. These values are normalized in relation to the total losses of the topology SP-4HB when $f_{ave-sw} = 2.50$ kHz, in each operating point E_l/I_l, shown in Fig. 11. Therefore, if $P_{to} < 1$, the conventional topologies (P-4HB and S-4HB) present smaller total losses than SP-4HB. Otherwise, if $P_{to} > 1$, the conventional topologies present larger total losses.

TABLE IV: Losses analysis ($f_{sw-SP} = 2.50$ kHz)

Point	Topology	P_{cd} (W)	P_{sw} (W)	P_{to} (W)
A	P-4HB	79.75	290.82	370.57
	S-4HB	476.08	236.56	712.64
	SP-4HB	191.60	229.00	420.60
B	P-4HB	9.20	148.01	157.21
	S-4HB	39.99	44.73	84.72
	SP-4HB	18.74	73.48	92.22
C	P-4HB	22.95	179.16	202.11
	S-4HB	117.45	83.91	201.36
	SP-4HB	50.44	108.22	158.66

As mentioned in Section V, for the same average switching frequency, all topologies present equal harmonic distortion for the load voltage or load current. In order to select the best topology among S-4HB, P-4HB and SP-4HB the criterion observed is the semiconductor losses. It is observed that the choice of the topology SP-4HB must be made when $36 < E_l/I_l < 140$ approximately (denominated here as SP-4HB zone – normalized $P_{to} > 1$), since the conventional topologies present higher losses in this zone, as highlighted in Fig. 11.

Outside the highlighted range, the total losses of the structure SP-4HB are higher than the total losses of the conventional topologies, so there are two choices: (i) conventional series topology, S-4HB, if the load voltage is high in relation to the load current (S-4HB zone) or (ii) conventional parallel topology, P-4HB, if the load current is high relative to the load voltage (P-4HB zone).

Fig. 12 shows the total losses values for the topology SP-4HB in different average switching frequency scenarios. It is observed that as the average frequency decreases, the values of losses decrease due to the reduction of switching losses.

Table IV details three points of operation: point A ($E_l/I_l \approx 24$), point B ($E_l/I_l \approx 175$), and point C ($E_l/I_l \approx 72$), in terms of conduction losses (P_{cd}), switching losses (P_{sw}), and total losses. These points are indicated in Figs. 11 and 12. In a scenario in which the relation E_l/I_l is high, it is recommended to use S-4HB topology (point B) to divide the output voltage

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TABLE V: Parameters used in experimental results

Parameter		Value
$E_{l,RMS}$	Load voltage (RMS)	220 V
P_l	Load power - transient	1.42 – 1.00 kW
fp_l	Load power factor (lagging)	0.92 – 0.95
f_l	Load frequency	60 Hz
f_{ave-sw}	Average switching frequency	2.5 kHz
m	Modulation index	0.95
v_{Ck}	DC symmetrical voltages	164 V
	DC asymmetrical voltages	109/218 V
C	DC capacitance	2200 µF
T_{sw}	Sampling period	100 µs

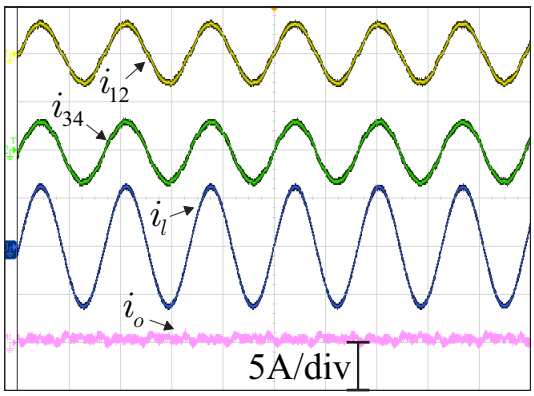
converter. On the other hand, the conduction losses increase as the relation E_l/I_l decreases, since it means that current amplitude grows. This can be clearly observed in point A. In such a scenario, the most recommended topology is the P-4HB. For the intermediate values of voltage and current (point C), the series/parallel connection is the more advantageous option. Since this pattern of converter power losses levels is repeated for various power values, the advantages of the series/parallel connection in terms of semiconductor losses are evident compared with only series or only parallel structures.

VII. Experimental Results

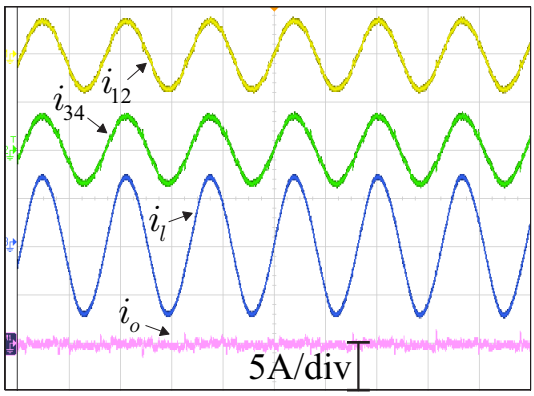
Experimental results are presented to validate the proposed system, as well as the described PWM and control strategy when the system operate at SP-4HB zone ($E_l/Il \approx 45$). Parameters used in the tests are shown in Table V. Figs. 13, 14, and 15 show the experimental results during steady-state operation, while Fig. 16 shows the transient-state results for topology SP-4HB. The experimental setup is a downscaled prototype based on power devices from SEMIKRON, with the switches being IGBTs with dedicated drives (SKHI23). A digital signal processor (DSP) TMS320F28335 with appropriated plug-in boards and sensors are used to the gating signals generation and to measure variables. A RL load is used to perform the transient-state and the steady-state operations of the proposed system.

The internal currents (i_{12} and i_{34}), load current (i_l), and the circulating current (i_o) of the converter SP-4HB are illustrated in Fig. 13. Fig. 14 shows the internal currents (i_1, i_2, i_3, and i_4) and the circulating current (i_o) of the converter P-4HB. The low-frequency circulating current is close to zero when $i_{12} = i_{34}$ to SP-4HB and when $i_1 = i_2 = i_3 = i_4$ to P-4HB. The series converter, S-4HB, has no circulating currents since it does not have parallel paths to the converter currents.

Fig. 15 shows the series voltages (v_{12} and v_{34}) and the output converter voltage (v_l). Fig. 15(a) shows the symmetrical case in which five-level series voltages and the output nine-level voltage are obtained by applying the described LS-PWM with phase-shifted carriers technique. The asymmetrical case, in which it is possible to obtain the series voltages with seven levels and the output voltage with thirteen levels is shown in Fig. 15(b).



(a)



(b)

Fig. 13: Internal, load and circulating currents os series/parallel converter SP-4HB – i_{12}, i_{34}, i_l, and i_o. (a) Symmetrical condition ($v_{C1} = v_{C2} = v_{C3} = v_{C4}$). (b) Asymmetrical condition ($2v_{C1} = v_{C2} = 2v_{C3} = v_{C4}$).

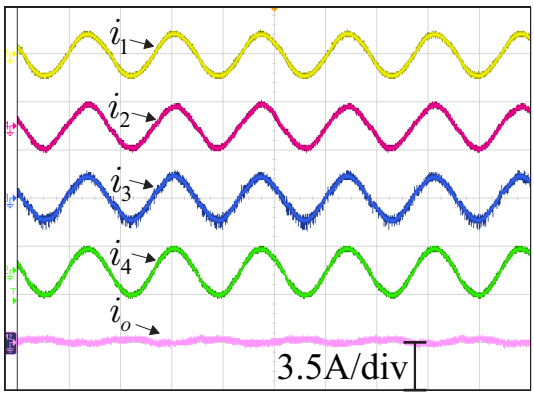


Fig. 14: Internal and circulating current of parallel converter P-4HB – i_1, i_2, i_3, i_4, and i_o.

Fig. 16 shows the behaviour of the system in transient-state operation when a load modification is performed. After increasing the load resistance (about 40%), the power decreases from approximately $P_l = 1.42$ kW to $P_l = 1.00$ kW. In this scenario, the load current i_l becomes smaller and the load voltage, e_l, has the amplitude and the frequency maintained by the control action.

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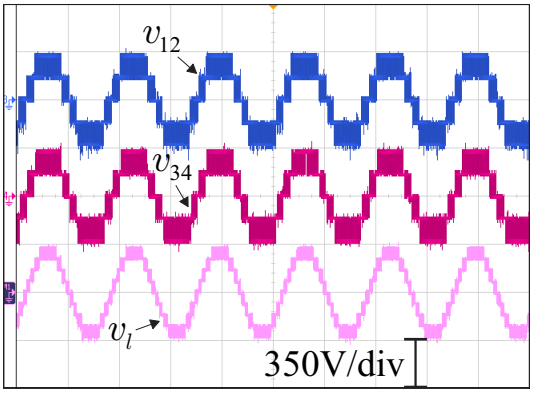
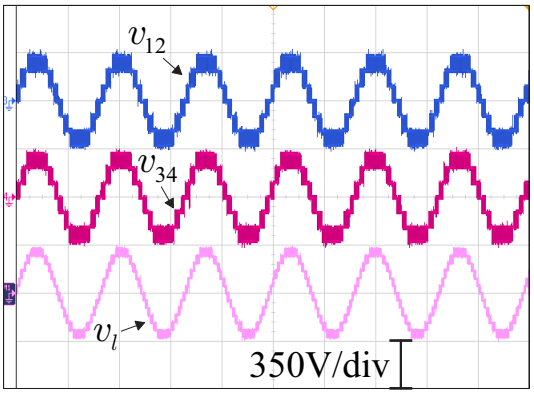


(a)



(b)

Fig. 15: Converter multilevel voltages – v_{12}, v_{34}, and v_l. (a) Symmetrical condition ($v_{C1} = v_{C2} = v_{C3} = v_{C4}$). (b) Asymmetrical condition ($2v_{C1} = v_{C2} = 2v_{C3} = v_{C4}$).

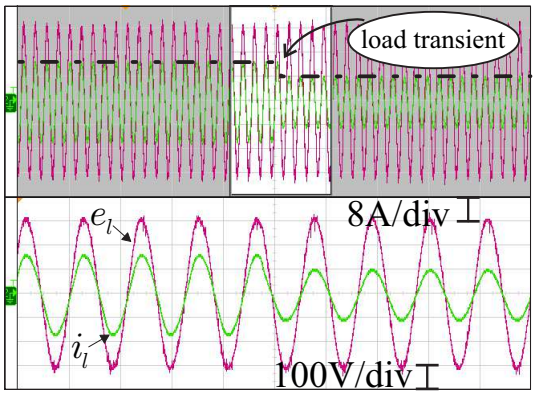


Fig. 16: Load transient experimental result of configuration SP-4HB – load voltage e_l and load current i_l.

VIII. Conclusions

A multilevel power converter formed by four series/parallel-connected H-bridges was investigated. The converter can be used for applications in which it is intended to use semiconductor switches with low voltage and low current ratings. The solution presented can be applied to various power levels and it is best used in cases where the relationship between voltage and current has intermediate values. Comparing to conventional topologies in which the H-bridges are connected either in series (S-4HB) or in parallel (P-4HB), the structure with the H-bridges connected in both series and parallel keeps the same harmonic distortion of the output variables of the converter, considering that the average switching frequency is the same. The system model and an overall control, including the LS-PWM strategy to mitigate the low-frequency circulating current were presented, as well as the generation of voltages and currents with low harmonic content. The total losses of the proposed converter can be reduced when compared to the conventional topologies. Therefore, the proposed series/parallel converter appears as an option between classic serial or parallel connections. In terms of costs, the series/parallel converter is cheaper in relation to high-power two-level solution, once it uses low-power-rating semiconductor switches. Simulation and experimental results demonstrated the feasibility of the studied converter.

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