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Monolithic active pixel sensors (MAPS) in a VLSI CMOS technology

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Abstract

Monolithic Active Pixel Sensors (MAPS) designed in a standard VLSI CMOS technology have recently been proposed as a compact pixel detector for the detection of high-energy charged particle in vertex/tracking applications. MAPS, also named CMOS sensors, are already extensively used in visible light applications. With respect to other competing imaging technologies, CMOS sensors have several potential advantages in terms of low cost, low power, lower noise at higher speed, random access of pixels which allows windowing of region of interest, ability to integrate several functions on the same chip. This brings altogether to the concept of 'camera-on-a-chip'.

In this paper, we review the use of CMOS sensors for particle physics and we analyse their performances in term of the efficiency (fill factor), signal generation, noise, readout speed and sensor area. In most of high-energy physics applications, data reduction is needed in the sensor at an early stage of the data processing before transfer of the data to tape. Because of the large number of pixels, data reduction is needed on the sensor itself or just outside. This brings in stringent requirements on the temporal noise as well as to the sensor uniformity, expressed as a Fixed Pattern Noise (FPN).

A pixel architecture with an additional transistor is proposed. This architecture, coupled to correlated double sampling of the signal will allow cancellation of the two dominant noise sources, namely the reset or kTC noise and the FPN. A prototype has been designed in a standard 0.25 μm CMOS technology. It has also a structure for electrical calibration of the sensor. The prototype is functional and detailed tests are under way.

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1. Introduction

Silicon devices have been used since the 1960s for the detection of radiation (see Ref. [1] for a detailed review). The interest of MOS devices was

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immediately recognised and arrays were designed. But the world of solid-state imaging was going to be revolutionised by the invention of the Charge-Coupled Devices (CCD) at the Bell Laboratory in 1970 [2]. CCD took over all the competing technologies. In 1981, C. Damerell et al. proposed the use of CCD for the detection of Minimum Ionising Particles for precise vertex reconstruction (see, for example, Ref. [3]). In 1983, Hitachi and Sony introduced the first consumer camera and in the same year Texas Instruments introduced the first mega-pixel device [4]. During about twenty years, from the invention of CCDs till the late 1980s, CMOS sensors were confined to very specialised applications, namely to IR focal-plane detectors, where CMOS sensors were used as readout circuits of bump-bonded low-band gap semiconductor detectors [5]. Different amplifier architectures have been integrated and tested [6–8]. In 1987, pixel sensors were also proposed for the detection of minimum ionising particles [9]. For this application, the detecting element is integrated in high-resistivity silicon in order to exploit the full depletion of the detector with reasonable voltages. Both the monolithic and the hybrid approach were proposed but in the following years, it was only the latter one, which gave interesting results [10]. Today many high energy-physics experiments have a vertex layer of hybrid pixel detectors [11]. Monolithic active pixel sensors (MAPS) based on high-resistivity silicon as a detecting element were demonstrated by S. Parker [12] in 1989. Good results were obtained only on small structures (about $1\,mm^2$ active area) [13], but no further results have been published on usable size devices.

In the late 1980s–beginning of 1990s, new developments on sensors based on a standard CMOS technology took place. CMOS technology uses low-resistivity substrates. In the literature, those sensors are normally referred to as CMOS sensors. The late 1980s developments took place at the University of Edinburgh, UK and were based on the so-called Passive Pixel Sensors (see Fig. 1a). These devices work much as amorphous silicon arrays. Only one selection transistor is integrated in the pixel together with the diode. The charge generated by the radiation is integrated in the diode. The readout is done by closing the selection switch and dumping the charge to a charge preamplifier, common to all the pixels in one column. This solution has the minimum amount of in-pixel electronics and thus has a very high fill factor, defined as the ratio between the detecting area and the total area of the pixel. It has however serious disadvantages in terms of speed and noise.

In the early 1990s, the first Active Pixel Sensors (Fig. 1b) were introduced [14,15]. The development was mainly pushed by the requirements of low power and low weight for space applications. In the minimum configuration of an APS, three transistors are integrated in the pixel (Fig. 1b). The transistor MRST is used to reset the pixel by dumping the integrated charge to the positive power supply line. The transistor MSEL is activated to select the readout of the pixel and MIN is the input transistor of a source follower.

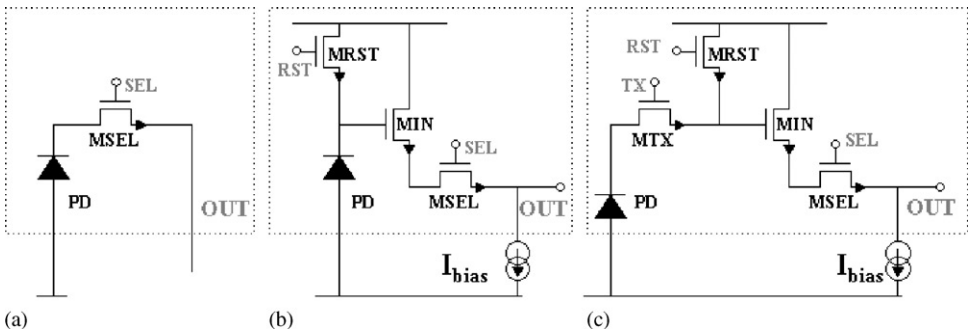

Fig. 1. The dashed line indicates the pixel area: (a) Schematic of a Passive Pixel Sensor (PPS). (b) Baseline, 3-MOS Active Pixel Sensor (APS). (c) 4-MOS APS with transfer gate (MTX).

The current source is common to all the pixels in one column.

With respect to other competing imaging technologies, CMOS sensors have several potential advantages in terms of low cost, low power, lower noise at higher speed (see, for example, Ref. [16]), random access of pixels which allows windowing of region of interest, ability to integrate several functions on the same chip. This brings altogether to the concept of 'camera-on-a-chip' [1].

The use of CMOS sensors in particle physics was proposed in 1999 [17]. The main difference with respect to visible light applications is that the sensor has to be 100% efficient. This can be achieved by using a structure which is readily available in most CMOS technologies and which was originally proposed for visible light detection [18]. A schematic view of the cross-section of a CMOS technology is shown in Fig. 2. In most modern CMOS process, n- and p-wells are fabricated on top of a thin p-doped epitaxial layer, with resistivity of the order of 1–10 Ω cm. The epitaxial layer thickness ranges between a few and up to about 20 μm and it is lightly doped with respect to the underlying p-substrate, whose main function is for mechanical support. A p–n junction exists between the n-well and the p-epilayer and can be used as the detecting element. Because of the difference in doping between the epitaxial layer and the p-well and the p-substrate, a potential difference of a few times kT/q is created. The epitaxial layer acts as a shallow potential well for the electrons, which are the minority carriers. Electrons created by the radiation diffuse in the epitaxial layer till they are close enough to the n-well/p-epi diode, where they experience an electric field. They are then collected by the diode.

Following the proposition of the concept, experimental results have shown the excellent properties of CMOS sensors as particle detectors, in terms of signal-over-noise, spatial resolution, detection efficiency [19–21]. In general, the interest in using CMOS sensors as particle detectors stems from their low multiple scattering, since a thin detective layer is used, high spatial resolution and good radiation tolerance.

In a CMOS Active Pixel Sensor (Fig. 1b), the diode is reverse biased by connecting to VDD through the reset switch. During the acquisition period, the charge generated in the diode is there stored, lowering the voltage on the diode. The charge-to-voltage conversion gain G_{in} at the input is given by $1/C_{in}$, where C_{in} is the total capacitance seen in the input node, and mainly determined by the diode capacitance and the gate-to-source capacitance of the input transistor. A simple

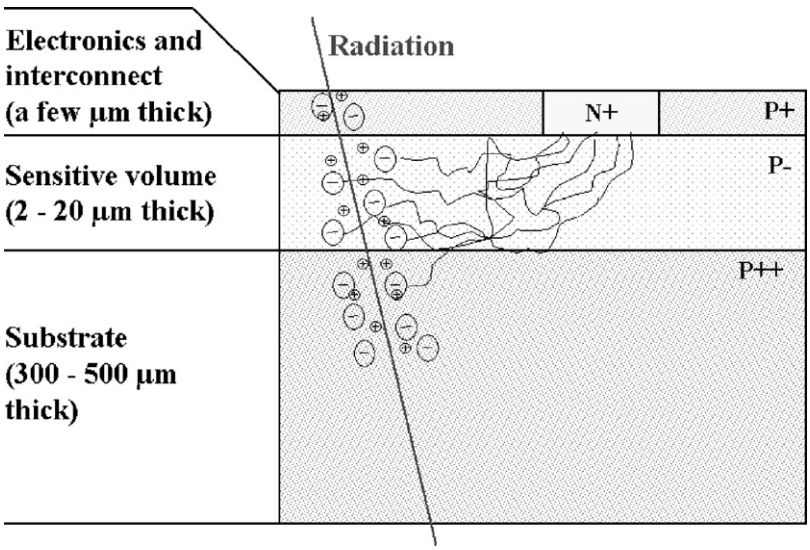

Fig. 2. Cross-section of a CMOS process showing the functioning of the proposed 100% fill factor structure.

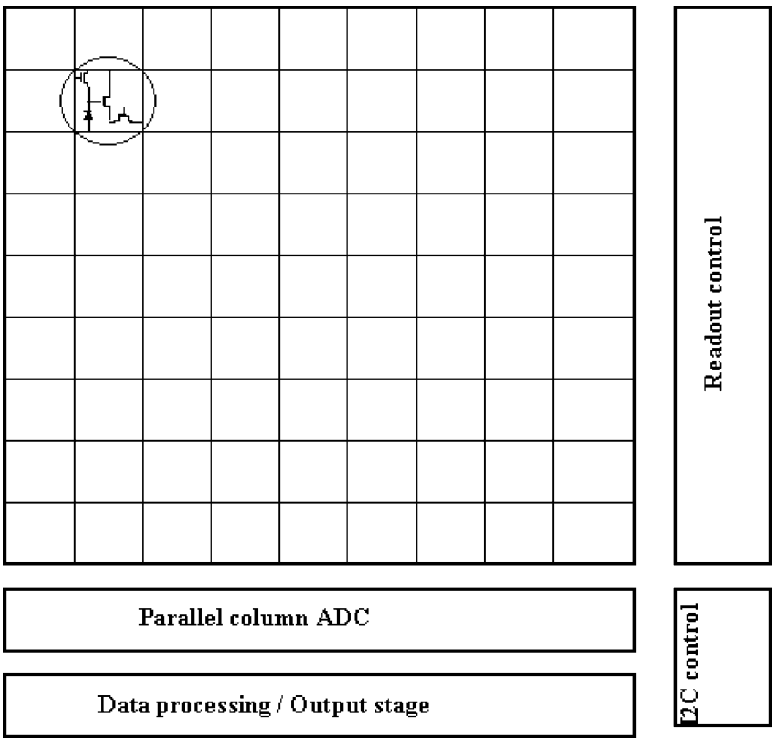

Fig. 3. Architecture of a CMOS sensor. The pixels are read in column and the data are digitised in parallel. On the periphery, other blocks can be integrated for the control of the circuits and for the data processing.

calculation shows that

$$G_{\text{in}}(\mu\text{V}/\text{e}^-) = \frac{160}{C_{\text{in}}(\text{fF})}.$$

Typical values of the input capacitances are in the range of a few fF up to about 10. The in-pixel source follower has also some voltage gain, normally in the range of 0.7–0.9 since the bulk of the NMOS is connected to ground. The gain G_{out} at the output of the source follower is thus given by

$$G_{\text{out}}(\mu\text{V}/\text{e}^-) = AG_{\text{in}} = \frac{160A}{C_{\text{in}}(\text{fF})}.$$

Typical gains G_{out} are in the range of 10–50 μV/e$^-$.

In Fig. 3, the architecture of a star tracker designed in RAL is shown [22]. Every column has a 10-bit single-slope ADC, and the conversion is done in parallel on every column. Data are output on a 10-bit wide digital bus. An analogue output is also integrated for test purposes. A state machine generates the control signals, in particular, the reset and the row select pointers. The distance between the two determines the integration time used in the sensor, which works in the rolling shutter mode.

2. CMOS sensors for particle detection

A CMOS sensor for particle physics applications has to satisfy specific constraints, different from the ones found in visible light applications.

Fill factor: As said before, sensors for visible light applications do not require 100% fill factor. This is however compulsory for HEP applications. It can be achieved by using the structure mentioned before.

Signal: Minimum Ionising Particles (MIP) generate about 80 e/h pairs per micron. The detecting volume in a CMOS sensor is mainly the epitaxial

layer. Some contribution comes from the underlying substrate. This can be explained by the diffusion of carriers from the substrate to the epitaxial layer helped by the small depletion layer generated by the potential differences at the interface [23–25]. In first approximation, the thickness of the epitaxial layer determines the generated charge. The thickness of the layer depends on the technology and it is of the order of a few microns and up to about 20. In standard microelectronics circuit, the thickness of the layer tends to decrease with the scaling of the technology, because thinner layers provide a better latch-up immunity [26]. For image sensors, the thickness of the layer is important for the absorption of light For example, absorption length of red light varies between about 2.5 and 4 μm. This explains the need for relatively thick absorption layers for visible light sensors. The conclusion we can draw from this discussion is that the expected charge signal for CMOS sensors in HEP is in the range of about 1000 electrons. This is without considering charge spread over pixels.

Temporal noise: The requirements on noise can be derived from the request of a small numbers of noise hits. The relative frequency f_{noise} of noise hits can be derived by the zero-crossing statistics [27]. A derivation for the simple case of a band-pass filter gives [28]

$$f_{\text{noise}} = 2f_0 \exp\left(-\frac{V_{\text{th}}^2}{2\sigma^2}\right)$$

where f_0 is the central frequency of the filter, V_{th} is the threshold voltage and σ is the noise voltage standard deviation. Considering half the high-pass frequency as the central frequency of the band-pass filter, the previous formula can be used to calculate the density of noise hits and hence the number of noise hits for a given number of pixels. It is interesting to note that the number of noise hits is proportional to the integrating time and to the frequency of the filter. The frequency of the filter is however also important in determining the noise of the readout chain which appears in the exponential factor. Depending on the actual parameters of the readout system, the threshold for which the density of noise hits is 10^{-5} lies in the range between 5 and 10. We can conclude that noise should be less than 50 e^- rms, taking into account a signal of a few hundreds electrons per pixel (this is after charge spread). This has to include also the 'noise' due to non-uniformity in the sensor response.

In a CMOS sensor the dominant noise source is the so-called kTC or reset noise. This is generated whenever a capacitance C is reset to a given voltage through a resistance R. The resistor has a thermal noise whose two-sided voltage noise power spectral density is $2kTR$. The RC network filters this noise and the total voltage noise power turns out to be kT/C. Since the voltage-to-charge relation is through the capacitance C, the equivalent noise charge generated through the reset is

$$\text{ENC}_{\text{reset}}^2 = kTC.$$

At room temperature this translates into a noise of

$$\text{ENC}_{\text{reset}}(e^- \text{ rms}) = 12.7\sqrt{C(\text{fF})}.$$

In a CMOS sensor the R is provided by the reset transistor and the C is the total capacitance at the input node. Typical reset noise contributions are thus of the order of 30–50 e^- rms.

The reset noise can be reduced in two ways. The first one is based on correlated sampling. The voltage on the diode is sampled a first time after the reset and then after the image acquisition. The first sample is determined by the reset noise, while the second one is the sum of the reset noise and of the actual signal. Differential readout of the two samples gives the signal without the reset noise. Of course, the differential readout increases the other noise sources basically by a factor of two, but this, as it will be discussed below is less important. This technique is called Correlated Double Sampling (CDS) and is a technique well-known to people working with imaging devices, in particular, CCDs.

The second way of reducing the reset noise is by using active reset schemes. Most of these techniques work by band-limiting the system, so that the filtering network is different from the original RC network [7,29,30,31]. It has to be noticed that because of the band-limiting operation, the reset cycle can be longer than in a normal reset. This can

be an important limitation while dealing with fast-readout as for high-energy physics system. Another limitation comes from the need of 100% detection efficiency. So far, this basically limits the choice of diode to the n-well/p-epistructure depicted in Fig. 2. In turn, this translates into a constraint on all-NMOS pixel electronics, which means that a limited choice of structures is available for the pixel architecture. This limitation could be overcome by the use of existing triple-well technologies.

In most of the systems, the readout noise can be reduced to less than $10\,e^-$ rms (see, for example, Ref. [21]). Another noise source is in the dark current. In modern, optimised process the leakage current is of the order of $1000\,e^-/s$ in a pixel of $20 \times 20\,\mu m$. The corresponding equivalent noise charge is

$$ENC_{leakage} = \sqrt{I_{leakage} T_{int}}$$

This yields $1\,e^-$ rms for an integration time of 1 ms.

Fixed pattern noise (FPN): In high-energy physics, where zero suppression is a need in most applications, an important source of noise is the so-called FPN. This is generated by non-idealities of the components. An important distinction is between pixel- and column-FPN. Pixel-FPN comes from parameters dispersion in the in-pixel transistors. It is mainly generated by threshold spread in the reset transistor and in the source follower input as well as in gain dispersion in the source follower. Column-FPN comes from parameter dispersion in the column amplifiers. The correction of column-FPN is less critical since on the periphery of the circuit there is some more space for additional, corrective circuitry. Pixel-FPN correction is critical and it can again be achieved by CDS. A simple structure is proposed in the following section:

Dynamic range: In visible light application, a high dynamic range is required. The full well capacity, which is normally in the order of 10^5 electrons is exploited. In the detection of MIPs, only a small dynamic range is required. This means that there is room for pixel amplification. Inverting amplifiers can be designed with only NMOS transistors. Because the output node is connected to the low-impedance terminal of the transistor, the overall gain is given by the ratio of transconductances [7]. As a first approximation, the gain is hence given by the ratio of the aspect ratio of the input over the load transistors, so it is limited to low values because of the limited space available in the pixel and on constraints on noise optimisation.

Another choice is to use a bias resistor. High value resistors are needed in order to get high open-loop gain. The charge-to-voltage gain is in this case dominated by the amplifier effect and determined by the effective feedback capacitance. Dispersion arising by the use of very small capacitances can be reduced by the use of T-networks [32].

Readout speed and data sparsification: In most applications, the readout rate is too high to be able to cope with full readout of the sensor. High readout speed and data reduction can be necessary. An example can be found in the Linear Collider application. It is interesting to note that for the Tesla design, the beam is active during only 1 ms every 200 ms. Data could be sampled in the pixel at high-speed and then read out during the no-beam periods, much in the same way as it is done for ultrahigh-speed cameras [33,34].

Sensor area: This is an important issue for high-energy physics. In microelectronics design, the size of the circuit is limited by the reticle size. This is normally in the range of about 2 cm. There is however no technological limitation to the stitching of different reticles to obtain a larger sensor. Alternatively, one can tolerate the dead area existing between reticles (which is less than 100 μm) and keep different sensors on the same substrate by a 'clever dicing'. This is probably the most cost-effective solution for a sensor for high-energy physics, where redundancy can be implemented in the overall detector. Whichever technology is selected for large area sensors, a sensor with full-wafer area coverage can in principle be designed. Modern deep submicron technology uses 8″ (200 mm) wafers and there is a move towards 12″ (300 mm) wafers. While designing a very large area sensor, one should take into account yield considerations and possibly add some redundancy in order to obtain a good yield.

3. Pixel Architecture for HEP

As discussed above, in HEP applications CDS is needed in order to reduce kTC noise and FPN. In a baseline 3-transistor structure (see Fig. 1b), FPN reduction can be achieved by sampling the signal, then resetting the pixel, sampling the reset value and taking the difference between the signal and the reset value. Reset noise is increased by a factor $\sqrt{2}$ since the two samples are not correlated. True CDS is needed in order to reduce the noise at level manageable in a large experiment.

Rutherford Appleton Laboratory, in collaboration with the Universities of Liverpool and Glasgow and the Imperial College of London, has started an R&D program to develop CMOS sensors for HEP applications. In this program, deep submicron technologies are used because of their inherent radiation hardness [35,36]. A first prototype sensor (RAL_HEPAPS1) has been designed in a standard 0.25 μm CMOS process. The thickness of the epitaxial layer in this technology is limited to about 2 μm, which indicates that a total signal of about 200 e^- is expected from a MIP. The aim of this prototype is mainly to test the electronic performances of the new structures implemented there.

The sensor consists of 8 arrays, each of 8×8 pixels at a pitch of 15 μm, with a single analogue output. The first four arrays use a photodiode as detecting element while the other 4 ones use a photogate. In the photodiode-based arrays, the baseline architecture is implemented in three of them: the first array has a single n-well/p-epidiode, the second one has four n-well/p-epidiodes connected in parallel, and the third one has a metal line running over the diode. A voltage step can be applied to this line to inject charge in the pixel for calibration purposes.

The fourth array in the photodiode-based half has a 4-transistor structure (Fig. 1c). The timing diagram is shown in Fig. 4. The first pulse on the TX transistor applies the reset to the diode. At the same time, the acquisition period starts. The arrival of a particle ('hit') on the sensor produces a negative step on the input diode. At the end of the integration period, the pixel is selected for readout. First the reset value is sampled, then the reset is released and a second TX pulse is applied. This transfers the collected charge on the input of the in-pixel source follower. The voltage here is the

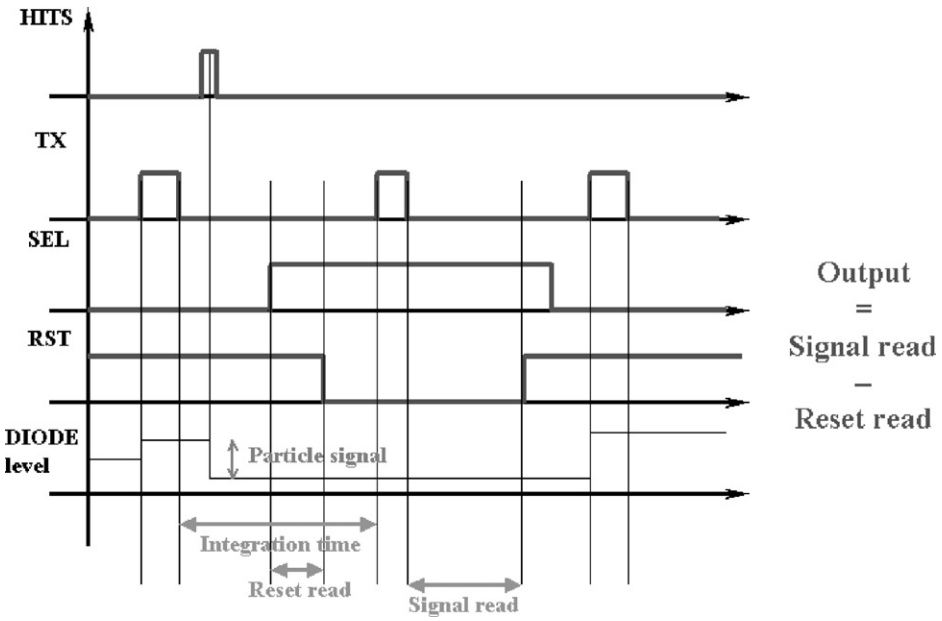

Fig. 4. Timing diagram of the 4-MOS pixel with transfer gate.

sum of the reset value plus the collected charge; subtracting the reset value yields the signal generated by the particle. Reset noise is thus eliminated as well as the FPN coming from threshold variation in the reset and the input transistors.

In the photogate-based sensor, the only differences between arrays is in the dimension and layout of the photogate. In this architecture, a transfer gate is also implemented and the functioning of the pixel is very much like that of an array of single cell CCD with individual amplifiers.

4. Conclusions

Monolithic Active Pixel Sensors (MAPS) designed in a standard VLSI CMOS technology have recently been proposed as compact pixel detectors for the detection of high-energy charged particle in vertex/tracking applications. MAPS, also named CMOS sensors, are already extensively used in visible light applications. With respect to other competing imaging technologies, CMOS sensors have several potential advantages in terms of low cost, low power, lower noise at higher speed, random access of pixels which allows windowing of region of interest, ability to integrate several functions on the same chip. This brings altogether to the concept of 'camera-on-a-chip'. Because of these advantages and of their low-cost, CMOS sensors are currently becoming the dominant imaging technology for consumer applications and enabling other applications, especially related to mobile imaging [37].

Here we reviewed the use of CMOS sensors for particle physics and we analyse their performances in term of the efficiency (fill factor), signal generation, noise, readout speed and sensor area. In most of high-energy physics applications, data reduction is needed in the sensor at an early stage of the data processing before transfer of the data to tape. Because of the large number of pixels, data reduction is needed on the sensor itself or just outside. This brings stringent requirements on the temporal noise as well as to the sensor uniformity, expressed as a Fixed Pattern Noise (FPN).

A pixel architecture with an additional transistor is proposed. This architecture, coupled to Correlated Double Sampling (CDS) of the signal will allow cancellation of the two dominant noise sources, namely the reset or kTC noise and the FPN. A prototype has been designed in a standard 0.25 μm CMOS technology. It has also a structure for electrical calibration of the sensor. The prototype is functional and detailed tests are under way.

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