

A Novel Single-Input Dual-Output Three-Level DC-DC Converter

Amir Ganjavi, Hoda Ghoreishy, and Ahmad Ale Ahmad

Abstract— This paper proposes a novel non-isolated single-input dual-output three-level dc-dc converter (SIDO-TLC) appropriate for medium and high voltage applications. The SIDO-TLC is an integration of the three-level buck and boost converters, whose output voltages are regulated simultaneously. Reducing voltage stress across semiconductor devices, improving efficiency, and reducing inductors size are among the main merits of the new topology. Moreover, due to the considerably reduced volume of the step-down filter capacitor, a small film capacitor can be used instead, whose advantages are lower ESR and a longer lifespan. A closed-loop control system has been designed based on a small-signal model derivation in order to regulate the output voltages along with the capacitors' voltage balancing. In order to verify the theoretical and simulation results, a 300 W prototype was built and experimented. The results prove the aforementioned advantages of the SIDO-TLC, and the high effectiveness of the balancing control strategy. Furthermore, the converter shows very good stability, even under simultaneous step changes of the loads and input voltage.

Index Terms— Multiport converter, non-isolated dc-dc converter, single-input dual-output dc-dc converter (SIDOC), single-input dual-output three-level dc-dc converter (SIDO-TLC), three-level converter.

I. INTRODUCTION

MULTI-PORT dc-dc converters have attracted a great deal of research interest recently, which could be attributed to the growing demand of renewable energy, the development of power electronic systems, and the increasing use of microgrids. Compared to several separate dc-dc converters, multiport dc-dc converters suggest a compact structure with a lower cost and less component counts [1]–[5]. At higher voltages, switches voltage stress is a major challenge for multiport dc-dc converters. The reason for that are the issues such as the cost and the inaccessibility of high voltage switches, which could also have a negative effect on overall efficiency due to their

high forward voltage drop and ON-state resistance. Moreover, the typical semiconductors used in high voltage applications are IGCT and high voltage IGBT [6], [7], which are not good solutions for multiport dc-dc converters. Due to the very high switching losses of those switches, their switching frequency is practically limited to about 1 KHz [6], [7]; therefore, the size of the passive components will increase dramatically. This study aimed at designing a high-efficiency multiport dc-dc converter with reduced voltage stress across semiconductor devices and shrunken passive components size.

Reference [8] proposes a bidirectional multiple-input multiple-output dc-dc converter based on the triangular modular multilevel dc-dc converter. In this converter, the voltage stress on switches is shared amongst the levels. In addition to its complex control system, the converter is not capable of generating buck and boost output voltages at the same time. As a result, it requires two separate circuits with different topologies to generate each voltage separately. In [9], a non-isolated single-input dual-output dc-dc converter (SIDOC) is proposed, which one of its outputs is boost and the other one is buck at the same time. The converter's topology is achieved through the substitution of two series-connected switches with the control switch of the conventional boost converter. The voltage stress on each switch and the diode is equal to the boost output voltage, making the converter appropriate for low-voltage applications. Meanwhile, because of high voltage stress on the diode and the series added switches, and also due to the lack of proper high input current distribution (which is typically the case in the single-input multiple-output converters) among the switches, the converter's both conduction and switching losses are high, which can lead to a fairly low system efficiency. Reference [10] proposes an isolated SIDOC, which comprises four diodes and only one power switch. However, in order to increase the efficiency and cope with the high current stress, two paralleled high-current switches with soft-switching method have been used in the experimental prototype. A number of studies have been found proposing multiport multi-level converters [11]–[13]. In [12], a non-isolated SIDOC is proposed, which is a combination of the sepic and five-level boost converters. The converter is composed of one switch and 10 diodes. The voltage stress on the switch is reduced to one-fifth of the high voltage side. Yet, high number of diodes may affect the reliability of the system. Moreover, reducing the passive components size,

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which is one of the advantages of the multi-level structures, has not been achieved through the proposed converter.

This paper presents a newly designed, non-isolated single-input dual-output three-level dc-dc converter (SIDO-TLC). With an appropriate control strategy, the converter benefits from both the three-level and multiport structures. Owing to its three-level structure, the proposed converter has the advantages of reduced voltage stress on switches and diodes, reduced passive components size, and improved efficiency. This paper has been arranged as follows: the following section offers the proposed converter and describes its operation principles and the related switching states. This section also analyzes the steady-state operation. In section III, the closed-loop and balancing control strategies are proposed, and the dynamic characteristics of the SIDO-TLC are analyzed through the obtained small-signal model. In section IV, the experimental results are demonstrated to verify the converter's behavior. Finally, a summary is provided in section V.

II. PRINCIPLE OF OPERATION

A. Switching States, Main Waveforms, and Operating Cases

Fig. 1 shows the circuit diagram of the proposed SIDO-TLC. In this figure, v_{in} is the input voltage, v_{o1} is the step-up output voltage, and v_{o2} is the step-down output voltage. The series capacitors C_{11} and C_{12} are the filter capacitors of the step-up output, while C_2 is the filter capacitor of the step-down output. The converter is composed of four power switches: S_1 , S_2 , S_3 , and S_4 , with anti-parallel diodes, and two power diodes: D_{11} and D_{12} . Table I shows the switching states, the unfiltered step-down output voltage v_{ab} , the instantaneous voltages of inductors v_{L1} and v_{L2} , the series capacitors' currents i_{C11} and i_{C12} , and also the capacitors' voltage change (magnitude and direction).

As can be seen from Table I, several switching states can not only generate the same output voltages, but also have the same charging states. In other words, they have identical equivalent circuits. Furthermore, some other switching states generate the same output voltages and just their charging states are different ((5, 6) & (7, 8); (9, 10) & (11, 12); 13 & 14). It appears that this wide variety of redundancies can guarantee the precise balancing of the series capacitors, which will be discussed in next sections.

Regarding the duty-cycles of the switches, there are three possible operating cases named A, B, and C for the SIDO-TLC. In the ideal situation, the control signals of S_1 and S_4 have the same duty-cycles ($d_{S1}=d_{S4}=d_1$) and are 180 degree phase-shifted. In the same way, the control signals of S_2 and S_3 have the same duty-cycles ($d_{S2}=d_{S3}=d_2$) and are 180 degree phase-shifted. In order to achieve the afore-mentioned phase-shifts, two saw-tooth carriers with the same frequency and 180 phase-shift are used in each operating case. Depending on d_1 and d_2 values, the operating cases can be expressed as follows:

Case A: $(1/2 < d_1 \text{ \& } d_2 < 1) \text{ \& } (d_1 > d_2)$.

Case B: $(1/2 < d_1 \text{ \& } d_2 < 1) \text{ \& } (d_1 < d_2)$.

Case C: $(d_2+1/2 < d_1 < 1) \text{ \& } (0 < d_2 < 1/2)$.

According to all possible duty-cycles and output voltage

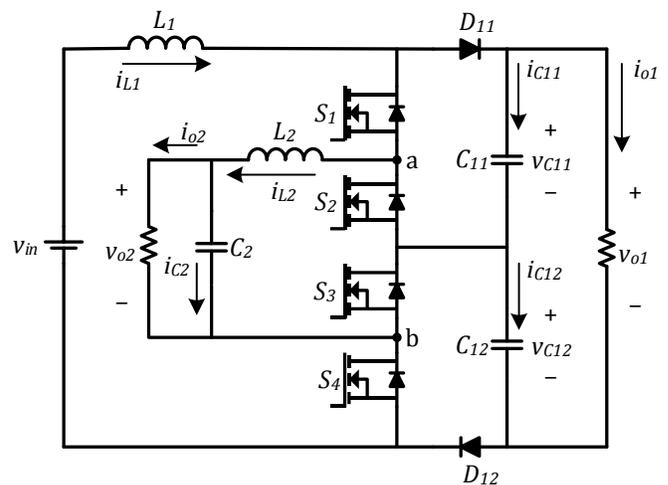


Fig. 1. The proposed SIDO-TLC.

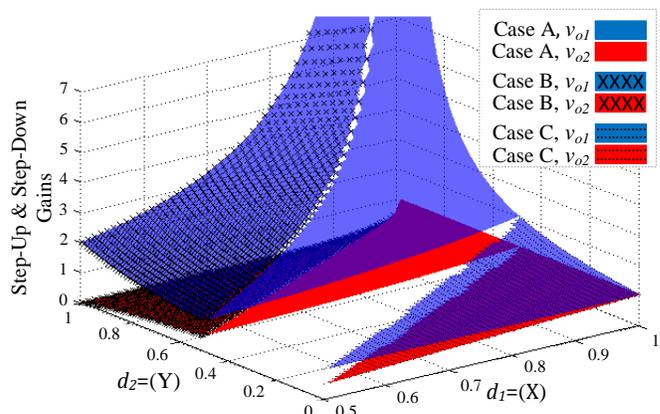


Fig. 2. Operating range of the output voltage gains with variation of duty-cycles d_1 , and d_2 .

limits in each case, the operating range of the SIDO-TLC is defined in Table II based on the steady-state evaluation. Accordingly, Fig. 2 illustrates the operating range of the SIDO-TLC by showing the voltage gain surfaces with variation of duty-cycles d_1 and d_2 . As it is seen in Fig. 2, although the proposed converter regulates two output voltages independently and at the same time fulfill the task of a three-level control strategy, the converter spans a wide range of duty-cycles. That is because all three possible cases in which the converter can regulate the output voltages along with its three-level control strategy are defined for the proposed converter. Also, Fig. 3 shows the main waveforms of the SIDO-TLC as well as its switching states in each case. As depicted in Fig. 3, v_{ab} varies between 0 and $V_{o1}/2$ in the operating cases A and B, while it varies between $V_{o1}/2$ and V_{o1} in case C. Meanwhile, due to the utilized switching sequence in each case, the effective ripple frequencies of the inductors currents and v_{ab} are twice as much as the switching frequency. This will help the designer to reduce the passive components size without increasing the switching frequency.

B. Static Gain

By applying inductors' volt-second balance in one-second of the switching period, both step-up and step-down gains can be

TABLE I

SWITCHING STATES FOR THE SIDO-TLC (ARROWS INDICATE MAGNITUDE AND DIRECTION- R_{o1} IS THE RESISTIVE LOAD AT THE STEP-UP TERMINAL)

| Switching state | S_1 | S_2 | S_3 | S_4 | v_{ab} | v_{L1} | v_{L2} | i_{C11} | i_{C12} | C_{11} | C_{12} |
|-----------------|-------|-------|-------|-------|------------|-------------------|-------------------|-------------------------------|-------------------------------|----------|----------|
| 1 | 0 | 0 | 0 | 0 | | | | | | | |
| 2 | 0 | 0 | 1 | 0 | 0 | $v_{in}-v_{o1}$ | $-v_{o2}$ | $i_{L1}-v_{o1}/R_{o1}$ | $i_{L1}-v_{o1}/R_{o1}$ | ↑ | ↑ |
| 3 | 0 | 1 | 0 | 0 | | | | | | | |
| 4 | 0 | 1 | 1 | 0 | | | | | | | |
| 5 | 0 | 0 | 1 | 1 | 0 | $v_{in}-v_{o1}/2$ | $-v_{o2}$ | $i_{L1}-v_{o1}/R_{o1}$ | $-v_{o1}/R_{o1}$ | ↑ | ↓ |
| 6 | 0 | 1 | 1 | 1 | | | | | | | |
| 7 | 1 | 1 | 0 | 0 | 0 | $v_{in}-v_{o1}/2$ | $-v_{o2}$ | $-v_{o1}/R_{o1}$ | $i_{L1}-v_{o1}/R_{o1}$ | ↓ | ↑ |
| 8 | 1 | 1 | 1 | 0 | | | | | | | |
| 9 | 0 | 0 | 0 | 1 | $v_{o1}/2$ | $v_{in}-v_{o1}$ | $v_{o1}/2-v_{o2}$ | $i_{L1}-v_{o1}/R_{o1}$ | $i_{L1}-i_{L2}-v_{o1}/R_{o1}$ | ↑↑ | ↑ |
| 10 | 0 | 1 | 0 | 1 | | | | | | | |
| 11 | 1 | 0 | 0 | 0 | $v_{o1}/2$ | $v_{in}-v_{o1}$ | $v_{o1}/2-v_{o2}$ | $i_{L1}-i_{L2}-v_{o1}/R_{o1}$ | $i_{L1}-v_{o1}/R_{o1}$ | ↑ | ↑↑ |
| 12 | 1 | 0 | 1 | 0 | | | | | | | |
| 13 | 1 | 0 | 1 | 1 | $v_{o1}/2$ | $v_{in}-v_{o1}/2$ | $v_{o1}/2-v_{o2}$ | $i_{L1}-i_{L2}-v_{o1}/R_{o1}$ | $-v_{o1}/R_{o1}$ | ↑ | ↓ |
| 14 | 1 | 1 | 0 | 1 | $v_{o1}/2$ | $v_{in}-v_{o1}/2$ | $v_{o1}/2-v_{o2}$ | $-v_{o1}/R_{o1}$ | $i_{L1}-i_{L2}-v_{o1}/R_{o1}$ | ↓ | ↑ |
| 15 | 1 | 0 | 0 | 1 | v_{o1} | $v_{in}-v_{o1}$ | $v_{o1}-v_{o2}$ | $i_{L1}-i_{L2}-v_{o1}/R_{o1}$ | $i_{L1}-i_{L2}-v_{o1}/R_{o1}$ | ↑ | ↑ |
| 16 | 1 | 1 | 1 | 1 | 0 | v_{in} | $-v_{o2}$ | $-v_{o1}/R_{o1}$ | $-v_{o1}/R_{o1}$ | ↓ | ↓ |

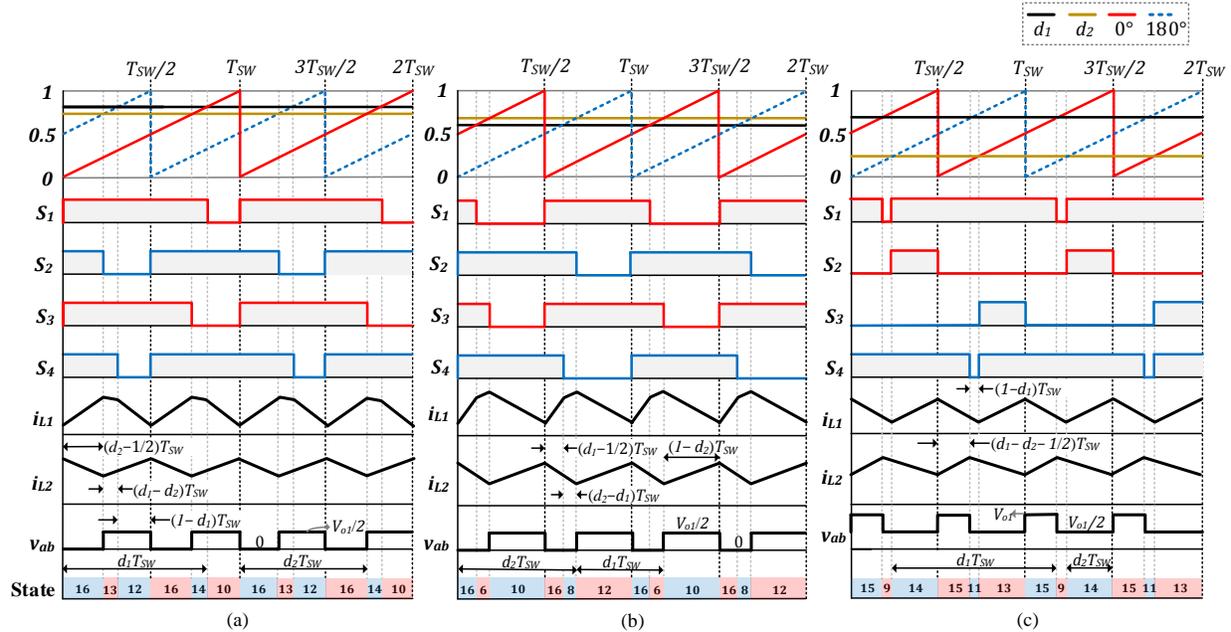


Fig. 3. Typical waveforms of the proposed converter, including the control signals of the switches, inductors currents, unfiltered step-down output voltage v_{ab} , and the switching states for all operating cases: (a) case A, (b) case B, (c) case C.

obtained in each case independently. According to Table I and the switching sequences in Fig. 3(a), the output voltages' conversion ratio can be obtained for case A as follows:

For the inductor L_1 ,

$$\underbrace{v_{in} \left(d_2 - \frac{1}{2} \right)}_{\text{State 16}} + \underbrace{\left(v_{in} - \frac{v_{o1}}{2} \right) (d_1 - d_2)}_{\text{State 13}} + \underbrace{\left(v_{in} - v_{o1} \right) (1 - d_1)}_{\text{State 12}} = 0$$

Hence,
$$\frac{v_{o1}}{v_{in}} = \frac{1}{2 - d_1 - d_2}. \quad (1)$$

TABLE II
OPERATING RANGE OF THE SIDO-TLC

| Case | Duty-cycle limits | Voltage limits |
|------|--|---|
| A | $1/2 < d_1 \text{ \& } d_2 < 1$ $d_1 > d_2$ | $v_{in}/2 < v_{o2} < v_{o1}/2$ |
| B | $1/2 < d_1 \text{ \& } d_2 < 1$ $d_1 < d_2$ | $0 < v_{o2} < v_{in}/2$ $v_{o1} > 2(v_{in}-v_{o2})$ |
| C | $d_2+1/2 < d_1 < 1$ $0 < d_2 < 1/2$ | $v_{o1}/2 < v_{o2} < v_{o1}$ $v_{in} < v_{o1} < 2v_{in}$ |

And for the inductor L_2 ,

$$\underbrace{(-v_{o2})\left(d_2 - \frac{1}{2}\right)}_{\text{State16}} + \underbrace{\left(\frac{v_{o1}}{2} - v_{o2}\right)(d_1 - d_2)}_{\text{State13}} + \underbrace{\left(\frac{v_{o1}}{2} - v_{o2}\right)(1 - d_1)}_{\text{State12}} = 0$$

Hence,
$$\frac{v_{o2}}{v_{o1}} = 1 - d_2. \quad (2)$$

Thus,
$$\frac{v_{o2}}{v_{in}} = \frac{v_{o2}}{v_{o1}} \times \frac{v_{o1}}{v_{in}} = \frac{1 - d_2}{2 - d_1 - d_2}. \quad (3)$$

The voltage gains in cases B and C can also be achieved in the same way as the above procedure.

Voltage gains for all three cases become

$$\frac{v_{o1}}{v_{in}} = \begin{cases} \frac{1}{2 - d_1 - d_2}, & \text{Case A \& Case B} \\ \frac{1}{1 - d_2}, & \text{Case C} \end{cases} \quad (4)$$

$$\frac{v_{o2}}{v_{in}} = \begin{cases} \frac{1 - d_2}{2 - d_1 - d_2}, & \text{Case A \& Case B} \\ \frac{d_1 - d_2}{1 - d_2}, & \text{Case C} \end{cases} \quad (5)$$

From (4) and (5), it can be seen that d_1 and d_2 are the control parameters for both output voltages. In cases A and B, the step-up output voltage is related to both d_1 and d_2 , while in the case C, it is only related to d_2 . On the other hand, the step-down output voltage in all three cases is related to both d_1 and d_2 . More detailed study of the control strategy will be conducted in the following section.

III. CONTROL AND DYNAMICS

A. Closed-Loop Control Strategy

In this paper, the method utilized for control strategy is taken from the conventional three-level buck and boost converters. Nonetheless, due to the novelty of the SIDO-TLC, a new control design is required. As previously mentioned, the proposed converter consists of three separate cases. In order to regulate both step-up and step-down output voltages, two proportional-integral (PI) compensators have been employed for each case. Having its own switching sequence, each case

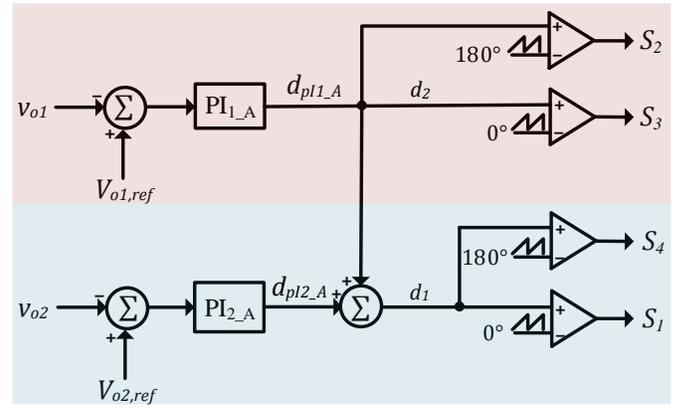


Fig. 4. Block diagram of the closed-loop control system for case A (excluding the balancing control system).

has exclusive PI controllers (e.g. PI_{1_A} & PI_{2_A} for case A in Fig. 4). In this study, the control strategy will be described for case A, and other cases will be designed with the same approach. According to Fig. 4, both output voltages are compared with their reference values ($V_{o1,ref}$ and $V_{o2,ref}$ for boost and buck outputs, respectively). The generated error signals will then pass through PI_{1_A} and PI_{2_A} , producing d_{p11_A} and d_{p12_A} , respectively. According to Table II, d_1 is greater than d_2 . To meet this condition, d_1 and d_2 are obtained as follows:

$$\begin{aligned} d_2 &= d_{p11_A} \\ d_1 &= d_{p11_A} + d_{p12_A}. \end{aligned} \quad (6)$$

Thus, the step-up output is regulated by d_2 , and the step-down output is regulated by d_1 , while d_2 is constant.

B. Voltage Balancing Control Strategy

In practice, the voltages of the series capacitors C_{11} and C_{12} will deviate from each other due to the asymmetry of the series switches and their drive signals [14], [15], as well as the leakage currents of the capacitors [16]. Another reason could be the electronic elements which are not essentially identical despite the fact that their factory specifications are the same. This unbalancing will cause problems such as damaging the switches and diodes, reducing the quality of the output waveforms, and reducing the total lifetime of the circuit. The objective of the balancing control strategy for the proposed converter is meeting (7):

$$v_{C11} \approx v_{C12} \approx \frac{v_{o1}}{2}. \quad (7)$$

For pursuing that, one of the voltages of the capacitors should be sensed and compared with $v_{o1}/2$. Again the balancing control procedure will be explained for case A.

On the assumption that the SIDO-TLC operates in case A, if $v_{C11} > v_{o1}/2$, v_{C11} should be decreased in comparison with v_{C12} . Thus, according to Table I, the time lengths of the switching states 12 and 14 should be increased, and the time lengths of 10 and 13 should be decreased. To fulfill the aim, as shown in Fig. 5, the pulse width of S_1 and S_2 should be increased, and the pulse width of S_3 and S_4 should be decreased, which means:

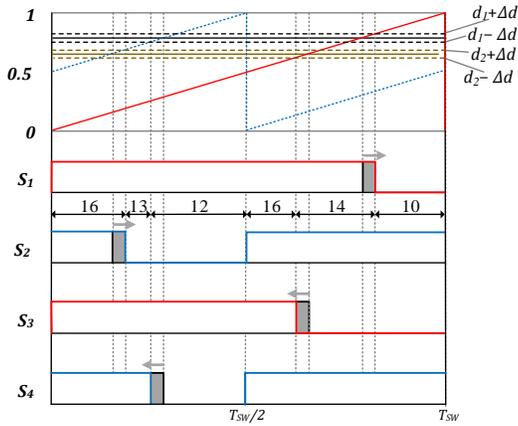


Fig. 5. Effect of balancing duty-cycle on the control signals of the switches and time length of the switching sates in case A.

$$\begin{aligned} d_{S1} &= d_1 + \Delta d \\ d_{S2} &= d_2 + \Delta d \\ d_{S3} &= d_2 - \Delta d \\ d_{S4} &= d_1 - \Delta d \end{aligned} \quad (8)$$

where Δd is the balancing duty-cycle.

C. Small-Signal Modeling

Obtaining the small-signal model of a converter is a high priority in designing the control system. In this paper, the balancing control strategy has been taken into account in the small-signal modeling of the SIDO-TLC. In the proposed approach, averaging of inductors currents and capacitors voltages in one switching period has been done for each case separately. The state space averaging in one switching period, for each case, can be expressed as

$$\langle x \rangle = \frac{1}{T_{SW}} \int_t^{t+T_{SW}} x(\tau) d\tau = X + \hat{x} \quad (9)$$

where T_{SW} is the switching period, X is a dc steady-state value, and \hat{x} is a small perturbation around X . The dynamic variables of the proposed converter are

$$\begin{aligned} \langle i_{L1} \rangle &= I_{L1} + \hat{i}_{L1} & \langle i_{L2} \rangle &= I_{L2} + \hat{i}_{L2} \\ \langle v_{o1} \rangle &= V_{o1} + \hat{v}_{o1} & \langle v_{o2} \rangle &= V_{o2} + \hat{v}_{o2} \\ \langle \Delta v_c \rangle &= \Delta V_c + \Delta \hat{v}_c & \Delta d &= \Delta D + \Delta \hat{d} \\ d_1 &= D_1 + \hat{d}_1 & a d_2 &= D_2 + \hat{d}_2. \end{aligned} \quad (10)$$

The voltage balancing error $\Delta v_c = v_{c11} - v_{c12}$ caused by the voltage unbalancing across the series capacitors is controlled by Δd . The relation between the step-up output voltage and its capacitors voltages is

$$\langle v_{c11} \rangle = \left\langle \frac{v_{o1}}{2} + \frac{\Delta v_c}{2} \right\rangle \quad \langle v_{c12} \rangle = \left\langle \frac{v_{o1}}{2} - \frac{\Delta v_c}{2} \right\rangle. \quad (11)$$

The state-space model in each case can finally be expressed as:

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{o1} \\ \hat{v}_{o2} \\ \Delta \hat{v}_c \end{bmatrix} &= [A] \cdot \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{o1} \\ \hat{v}_{o2} \\ \Delta \hat{v}_c \end{bmatrix} + [B] \cdot \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \Delta \hat{d} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_m \\ \begin{bmatrix} \hat{v}_{o1} \\ \hat{v}_{o2} \\ \Delta \hat{v}_c \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{o1} \\ \hat{v}_{o2} \\ \Delta \hat{v}_c \end{bmatrix} \end{aligned} \quad (12)$$

where $[A]$ and $[B]$ are the system and control matrices, respectively. Also, \hat{v}_{o1} , \hat{v}_{o2} , and $\Delta \hat{v}_c$ compose the outputs of the control system.

In the ideal situation, the steady-state voltage balancing error (ΔV_c) and also ΔD are equal to zero. However, due to the non-idealities such as the leakage currents (i.e. when using electrolytic capacitors), ΔV_c has a non-zero value. If so, the designed balancing control system should produce an appropriate Δd to tend Δv_c to zero. The leakage currents of the series capacitors are modeled with two constant dc current sources (I_{Leak1} and I_{Leak2}) paralleled with C_{11} and C_{12} , respectively [16]. The relation between the leakage currents and the steady-state balancing duty-cycle, in case A, can be expressed as:

$$\Delta D = \frac{I_{Leak2} - I_{Leak1}}{4I_{L1} - 2I_{L2}} = \frac{\Delta I_{Leak}}{4I_{L1} - 2I_{L2}}. \quad (13)$$

In order to obtain the linearized state-space equations, the inductors' volt-second balance and capacitors' charge balance are analyzed in one switching period then the second-order ac terms are neglected. By assuming $C_{11} = C_{12} = C_1$, and considering the resistive loads R_{o1} and R_{o2} at the step-up and step-down terminals, respectively, the matrices $[A]$ and $[B]$ can be expressed as:

$$\begin{aligned} [A] &= \begin{bmatrix} 0 & 0 & \frac{D_1 + D_2 - 2}{L_1} & 0 & \frac{2\Delta D}{L_1} \\ 0 & 0 & \frac{1 - D_2}{L_2} & -\frac{1}{L_2} & -\frac{\Delta D}{L_2} \\ -\frac{2(D_1 + D_2 - 2)}{C_1} & -\frac{2(1 - D_2)}{C_1} & -\frac{2}{R_{o1}C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{C_2R_{o2}} & 0 \\ -\frac{4\Delta D}{C_1} & \frac{2\Delta D}{C_1} & 0 & 0 & 0 \end{bmatrix} \end{aligned} \quad (14)$$

$$[B] = \begin{bmatrix} \frac{V_{o1}}{L_1} & \frac{V_{o1}}{L_1} & \frac{2\Delta V_c}{L_1} \\ 0 & -\frac{V_{o1}}{L_2} & -\frac{\Delta V_c}{L_2} \\ -\frac{2I_{L1}}{C_1} & \frac{2(I_{L2} - I_{L1})}{C_1} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{2(I_{L2} - 2I_{L1})}{C_1} \end{bmatrix} \quad (15)$$

D. Compensator Design

The operation of the SIDO-TLC has been validated using a lab prototype. The converter's specifications for a design example are shown in Table III. Regarding these specifications, the SIDO-TLC operates in case A, as in compliance with the relations in Table II. Also, Table IV shows the selected components of the converter. From (12), (14), and (15), the control transfer functions of the converter is obtained through MATLAB software. The corresponding Bode diagrams have also been plotted in order to design the optimal control system. As previously mentioned, the step-up output voltage is regulated by d_2 , and the step-down output voltage is regulated by d_1 . The control transfer functions with constant coefficients are expressed in (16)–(18) at the ideal situation ($\Delta D = 0$) as well as at the condition when the leakage currents of the series capacitors are included ($\Delta D = 0.004$). The constant coefficients of (16)–(18) are provided in APPENDIX.

TABLE III
DESIGN EXAMPLE SPECIFICATIONS FOR THE SIDO-TLC

| Parameter | Value |
|---------------------------------------|-------------|
| Total Output Power (P_o) | 300 W |
| Input Voltage (V_{in}) | 60 V |
| Step-Up Output Voltage (V_{o1}) | 125 V |
| Step-Down Output Voltage (V_{o2}) | 36 V |
| Step-Up Resistive Load (R_{o1}) | 65 Ω |
| Step-Down Resistive Load (R_{o2}) | 20 Ω |
| Switching Frequency (f_{sw}) | 20 KHz |

TABLE IV
COMPONENT LIST OF THE SIDO-TLC

| Component | Attribute | Specification |
|--------------------------------|-------------|---|
| Inductor (L_1) | 401 μ H | Iron powder core: T184-26 Wire: AWG #20 |
| Inductor (L_2) | 740 μ H | |
| Capacitor (C_{11}) | 31 μ F | Film capacitor |
| Capacitor (C_{12}) | 30 μ F | |
| Capacitor (C_2) | 4.5 μ F | |
| MOSFETs (S_1 - S_4) | 100 V/ 33 A | IRF540NPbF (International Rectifier) |
| Diodes (D_{11} - D_{12}) | 600 V/ 15 A | MUR1560G (On Semiconductor) |

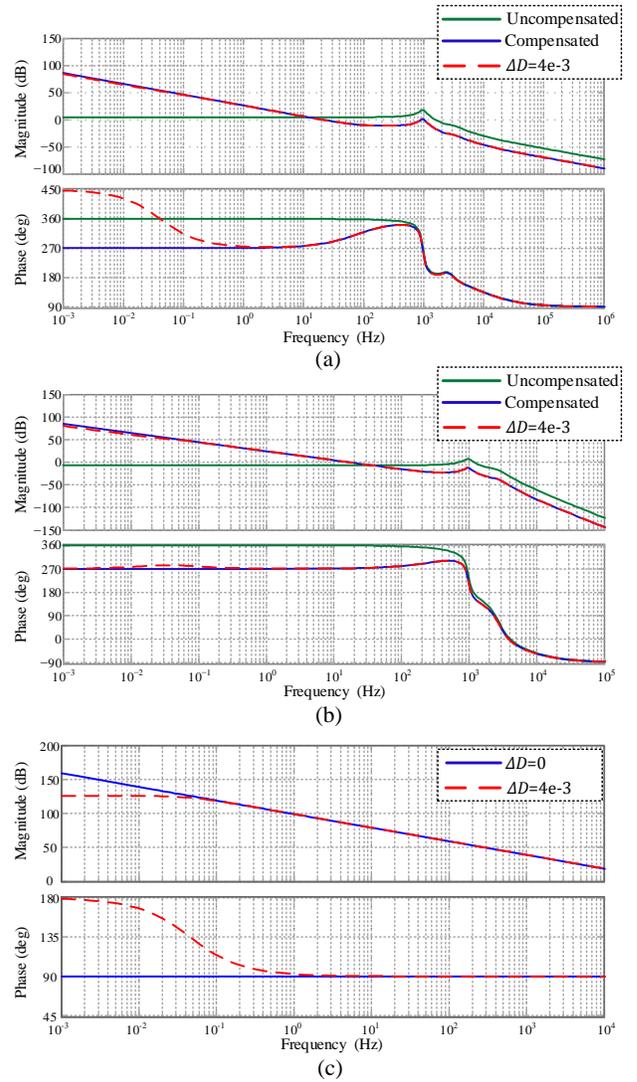


Fig. 6. Bode diagrams of the designed SIDO-TLC. (a) Loop gain of the step-up output before the compensation, after the compensation with $\Delta D=0$, and after the compensation with $\Delta D=0.004$ [see (16)]. (b) Loop gain of the step-down output —, [see (17)]. (c) Balancing control transfer function ($\Delta \hat{v}_c / \Delta \hat{d}$) with $\Delta D=0$, and $\Delta D=0.004$ [see (18)].

$$\frac{\hat{v}_{o1}}{\hat{d}_2} \Big|_{\Delta D=0} = \frac{\alpha_3 s^3 + \alpha_2 s^2 + \alpha_1 s + \alpha_0}{s^4 + \beta_3 s^3 + \beta_2 s^2 + \beta_1 s + \beta_0} \quad (16)$$

$$\frac{\hat{v}_{o1}}{\hat{d}_2} \Big|_{\Delta D=4 \times 10^{-3}} = \frac{\alpha'_4 s^4 + \alpha'_3 s^3 + \alpha'_2 s^2 + \alpha'_1 s + \alpha'_0}{s^5 + \beta'_4 s^4 + \beta'_3 s^3 + \beta'_2 s^2 + \beta'_1 s + \beta'_0}$$

$$\frac{\hat{v}_{o2}}{\hat{d}_1} \Big|_{\Delta D=0} = \frac{\gamma_1 s + \gamma_0}{s^4 + \delta_3 s^3 + \delta_2 s^2 + \delta_1 s + \delta_0} \quad (17)$$

$$\frac{\hat{v}_{o2}}{\hat{d}_1} \Big|_{\Delta D=4 \times 10^{-3}} = \frac{\gamma'_2 s^2 + \gamma'_1 s + \gamma'_0}{s^5 + \delta'_4 s^4 + \delta'_3 s^3 + \delta'_2 s^2 + \delta'_1 s + \delta'_0}$$

$$\frac{\Delta \hat{v}_c}{\Delta \hat{d}} \Big|_{\Delta D=0} = \frac{\lambda_0}{s} \quad (18)$$

$$\frac{\Delta \hat{v}_c}{\Delta \hat{d}} \Big|_{\Delta D=4 \times 10^{-3}} = \frac{\lambda'_4 s^4 + \lambda'_3 s^3 + \lambda'_2 s^2 + \lambda'_1 s + \lambda'_0}{s^5 + \xi'_4 s^4 + \xi'_3 s^3 + \xi'_2 s^2 + \xi'_1 s + \xi'_0}$$

From (16)–(18), the Bode diagrams of the loop gains for both outputs are illustrated in Fig. 6.

As can be seen in Figs. 6(a) and 6(b), before the compensation, the phase for both the step-up and step-down loops are 360 degree at the gains more than unity, which can lead to system instability. In order to make the gain plots pass 0 dB line at the slope of -20 dB/dec, and at the same time have sufficient phase and gain margins, a simple PI controller has been used for each loop. In this case, the selected PI controller's proportional and integral gains for the step-up loop are 0.15 and 74, and for the step-down loop are 0.09 and 228, respectively.

After the compensation, the step-up loop's phase margin is 63 degree and its gain margin is 28.1 dB. Also, the step-down loop's phase margin is 91 degree and its gain margin is 15.75 dB.

IV. EXPERIMENTAL RESULTS

As shown in Fig. 7, a 300 W SIDO-TLC lab prototype has been built with the parameters of Tables III and IV.

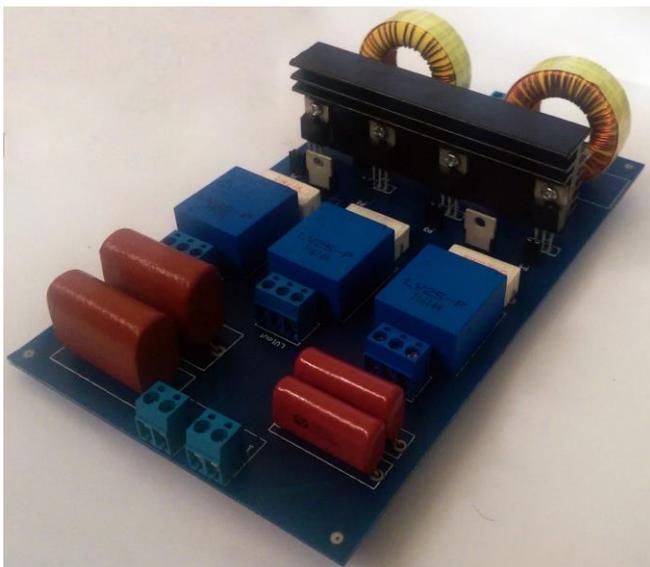


Fig. 7. Photo of the designed experimental prototype.

It should be noted that the power diodes used in the experimental prototype are oversized ones available in our laboratory (which 100 V diodes could be used instead). The control algorithm was executed by the DSP TMS320F28335 from Texas Instruments with the sampling period (T_S) equal to the switching period. The control specifications are first designed in the continuous-time S domain then they are transferred to the discrete-time Z domain to be feasible in the digital controller. In order to implement the PI compensators in the control algorithm, a Forward Euler method has been used. This approximation is

$$\frac{1}{S} = \frac{T_S}{Z-1}, \quad T_S = T_{SW} = 5 \times 10^{-5} \text{ (s)}. \quad (19)$$

A. Steady State Test

1) Main Waveforms

Fig. 8 shows the steady-state behavior of the proposed converter. In Fig. 8(a), it is seen that the ripple frequency of the inductors currents is twice as much as the switching frequency. Also, a 180 degree phase shift between the control signals of S_2 and S_3 can be seen from the figure. In Figs. 8(b) and 8(c), it is shown that the voltage stress on the switches and diodes is 62.5 V i.e. half of the step-up output voltage. It is also seen in Fig. 8(c) that v_{ab} is between 0 and 62.5 V ($V_{o1}/2$), which is in compliance with Fig. 3(a) in case A.

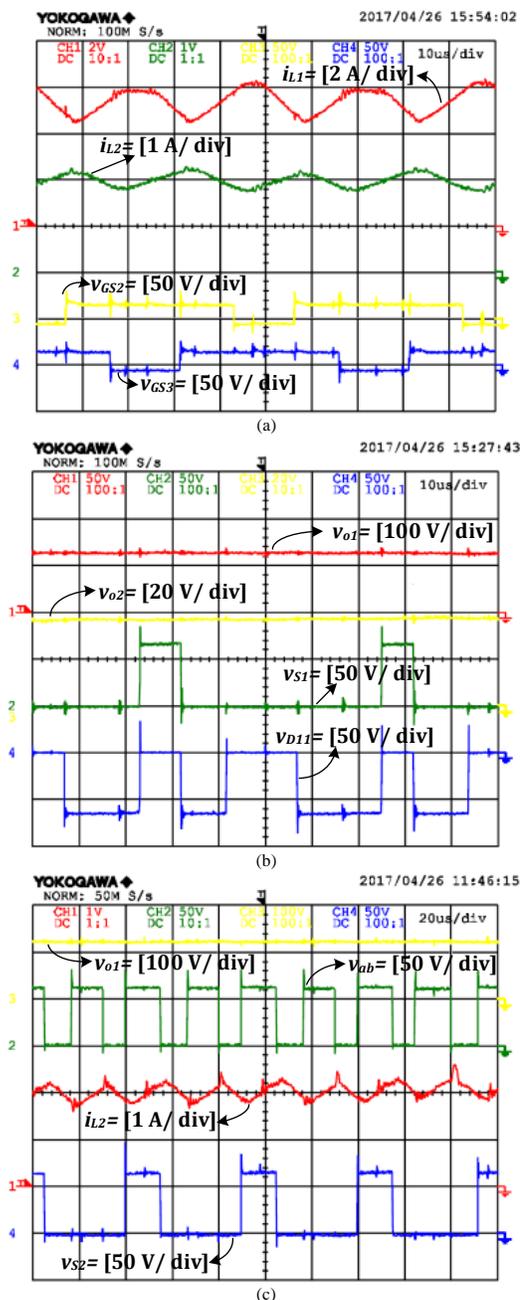


Fig. 8. Steady-state experimental waveforms of the SIDO-TLC ($V_{in}=60$ V, $V_{o1}=125$ V, $V_{o2}=36$ V, $R_{o1}=65$ Ω , $R_{o2}=20$ Ω). (a) Inductors currents and the control signals of S_1 and S_2 . (b) Output voltages, voltage across S_1 and D_{11} . (c) Step-up output voltage, current of L_2 , unfiltered step-down output voltage v_{ab} , voltage across S_2 .

2) Effect of Non-Idealities

Like the conventional dc-dc converters, the SIDO-TLC is affected by non-idealities such as inductors' series resistance and switches ON-state resistance. To illustrate the effect of these non-idealities on the operation of the proposed converter, the steady-state output voltages are compared in calculation (through (4), and (5)), ideal simulation, and experimentation for various ranges of duty-cycles. Figs. 9 and 10 Show the comparison at different duty-cycles. The comparisons are conducted at the constant input voltage of $V_{in}=60$ V, and of the two duty-cycles, one is kept constant and the other one is varying to see the change in the output voltages. Fig. 9 shows the variation in the step-up output voltage with the variation of D_1 and D_2 , respectively, while keeping one of them constant and the other one varying; with the same approach, Fig. 10 shows the variation in the step-down output voltage. As a result, the experimental values of V_{o1} and V_{o2} deviate from those of calculation or simulation typically about 2.5% and 2%, respectively. The calculation and ideal simulation match accurately with each other, proving that the calculated equations for gains are precisely obtained. Also, all in all, there is a good match of the experimental values with those of calculation or simulation.

B. Transient State Test

1) Step Change of Loads

In order to test the stability of the system under dynamic changes, two different situations are considered. In the first situation, step changes are applied to the input voltage and the step-up output load, and in the second situation, step changes are applied to the input voltage and the step-down output load. In fact, the simultaneous step changes of load and input voltage can be regarded as a bigger challenge for the control system rather than the individual change of the load or the input voltage. In Fig. 11(a), the resistive load at the boost terminal changes from $R_{o1}=65\ \Omega$ to $R_{o1}=303\ \Omega$, and at the same time, the input voltage steps up from $V_{in}=56$ V to $V_{in}=60$ V. Under this condition, v_{o1} settles to its reference value in about 60 ms with a 20% overshoot (25 V), and v_{o2} in about 80 ms with a 12% undershoot (4.2 V). It is clear that the output voltages are stably regulated at their predetermined values of $V_{o1}=125$ V and $V_{o2}=36$ V under dynamic changes, owing to the satisfactory performance of the closed-loop control system.

In Fig. 11(b), the resistive load at the buck terminal changes from $R_{o2}=135\ \Omega$ to $R_{o2}=20\ \Omega$, and at the same time, the input voltage steps down from $V_{in}=60$ V to $V_{in}=59$ V. As it can be seen, the output voltages are insensitive to the simultaneous changes of the input voltage and step-down terminal load.

2) Autonomous Transition Through Cases

As seen in Fig. 12, with the sudden change of the input voltage from 60 V to 92 V, the control system autonomously switches from case A to B, and the output voltages are well regulated at their predetermined values.

C. Balancing Strategy Test

In order to test the proposed balancing strategy of the SIDO-TLC practically, an unbalanced condition at the step-up terminal has been provided. Fig. 13 shows i_{L1} , v_{C11} , v_{C12} , and v_{o1} with and without the balancing control strategy. As can be seen

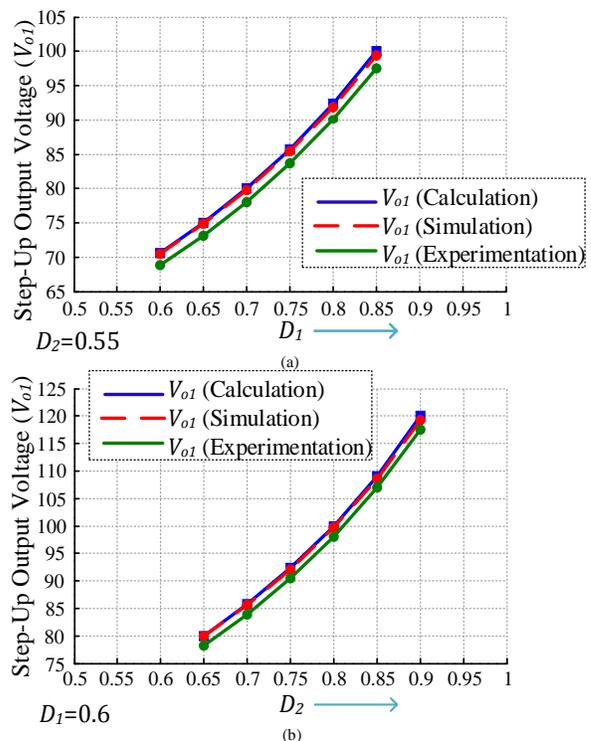


Fig. 9. Comparative analysis of calculated, simulated, and experimental results of the output voltages with variations in D_1 and D_2 for V_{o1} .

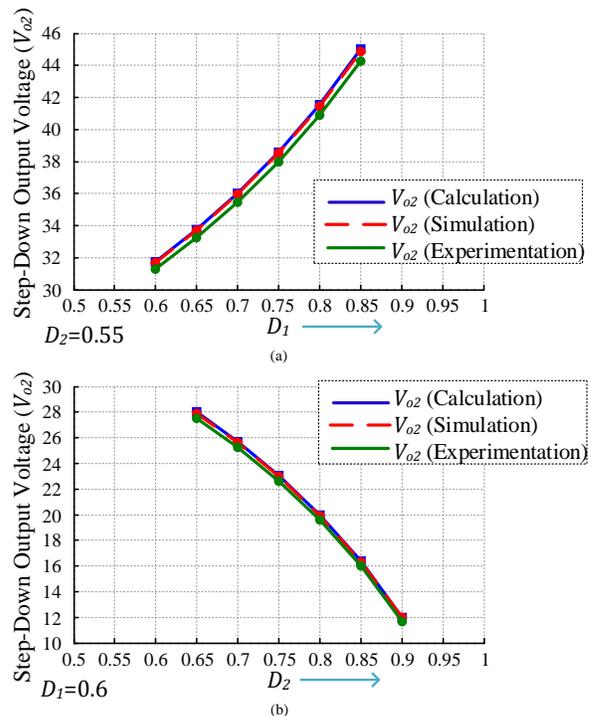
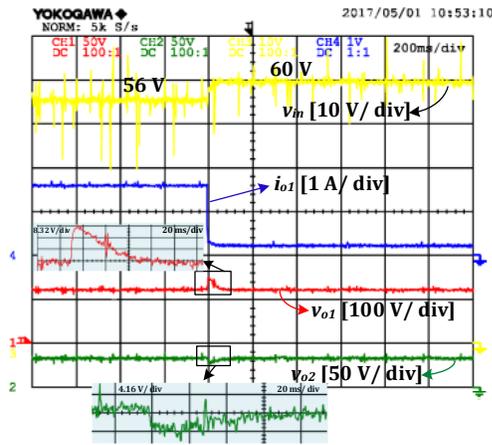
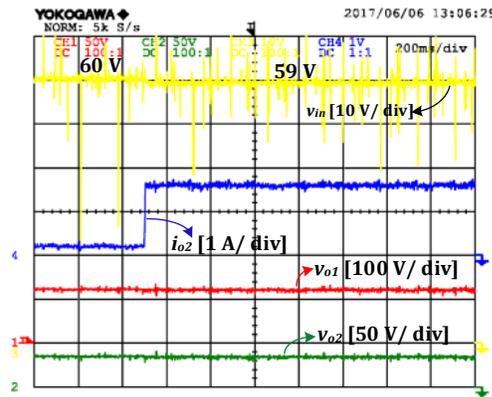


Fig. 10. Comparative analysis of calculated, simulated, and experimental results of the output voltages with variations in D_1 and D_2 for V_{o2} .

in Fig. 13(a), without the balancing control technique, the voltage difference between the series capacitors reaches 20 V, yet if the unbalancing increases, the switches and diodes will be damaged. By applying the balancing control strategy, as seen in Fig. 13(b), the voltages are precisely balanced, and the output

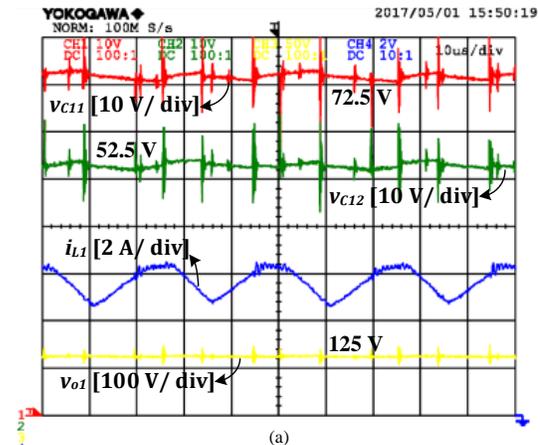


(a)

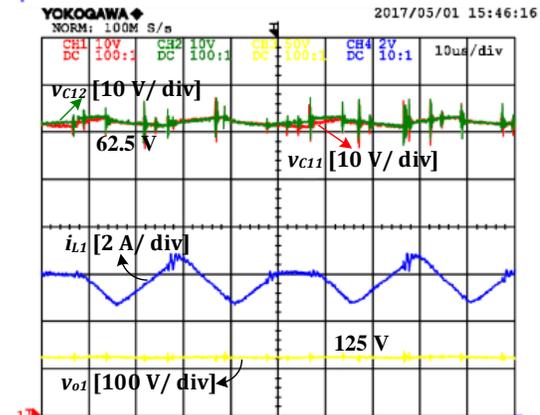


(b)

Fig. 11. Transient state experimental waveforms of the SIDO-TLC due to the varied load and input voltage. (a) Load at the step-up terminal changes from $R_{o1}=65 \Omega$ to $R_{o1}=303 \Omega$, and input voltage changes from 56 V to 60 V. (b) Load at the step-down terminal changes from $R_{o2}=135 \Omega$ to $R_{o2}=20 \Omega$, and input voltage changes from 60 V to 59 V.



(a)



(b)

Fig. 13. Experimental waveforms of series capacitors voltages, step-up output voltage, and i_{L1} in an unbalanced condition. (a) Without the balancing control system, (b) with the proposed balancing control technique.

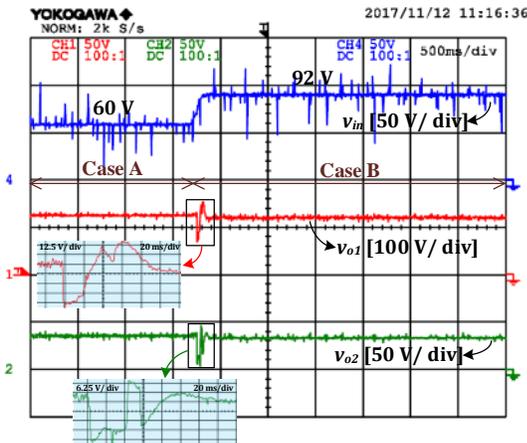


Fig. 12. Autonomous transition from case A to case B with the sudden change of the input voltage from 60 V to 92 V.

voltages stay regulated at the same time. This highly accurate balance of the series capacitors voltages is due to the wide variety of the switching state redundancies. This makes the converter appropriate for the applications such as the three-level diode clamped inverters in which the dc link capacitors voltage balancing is very important.

D. Efficiency and Comparison

The efficiency of the SIDO-TLC has been measured in two different conditions: Firstly, when the powers of the two outputs are equal to each other, namely $P_{o1}=P_{o2}$. Secondly, when the power of the step-up output is twice as much as that of the step-down, namely $P_{o1}=2P_{o2}$. In both conditions, the terminal voltages are fixed at $V_{in}=60$ V, $V_{o1}=125$ V, and $V_{o2}=36$ V. Fig. 14 illustrates the measured efficiencies. The average of the measured efficiencies is 95.03%, and the efficiency peaks at 95.9%. Despite using the oversized diodes, the obtained efficiencies are high. This could be attributed to the fact that both conduction and switching losses are reduced in comparison with the conventional two-level structures. The conduction losses are reduced because MOSFETs with less ON-state resistance could be used due to the considerable reduction of the voltage stress across the switches [17]. Also, the diode reverse recovery losses are reduced because the voltage stress on the diodes is only half of the step-up output voltage, so the total switching losses are significantly reduced [17]. In Table V, some SIDOCs have been found to be compared with the proposed SIDO-TLC in terms of voltage stress and efficiency. As can be seen in Table V, most of the SIDOCs in previous works are buck-type converters, such as [19]–[21]. In fact, very few references propose converters generating both step-up and step-down outputs

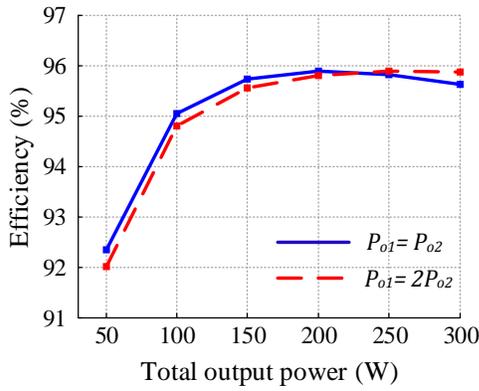


Fig. 14. Efficiency curve of the prototype as a function of the total output power in the conditions where $P_{o1}=P_{o2}$, and $P_{o1}=2P_{o2}$.

TABLE V
PERFORMANCE COMPARISON OF THE PROPOSED SIDO-TLC WITH OTHER ANNOUNCED SIDOCS

| Reference | Terminal voltages | Efficiency | Maximum voltage stress on semiconductor devices |
|-----------------|--|-----------------|---|
| [9] | $V_{in}=12$ V $V_{o1}=18$ V $V_{o2}=6$ V | Around 90% | v_{o1} |
| [18] | $V_{in}=15$ V $V_{o1}=20$ V $V_{o2}=10$ V | N/A | More than $(v_{o1}+v_{o2})$ |
| [19] | $V_{in}=300$ V $V_{o1}=24$ V $V_{o2}=48$ V | 93.2% (Maximum) | v_{in} |
| [20] | $V_{in}=100$ V $V_{o1}=40$ V $V_{o2}=80$ V | 96.8% (Nominal) | v_{in} |
| [21] | $V_{in}=400$ V $V_{o1}=12$ V $V_{o2}=5$ V | 92.5% (Maximum) | More than v_{in} |
| Proposed | $V_{in}=60$ V $V_{o1}=125$ V $V_{o2}=36$ V | 95.9% (Maximum) | $v_{o1}/2$ |

similar to the one in this study. As it can be seen, in the proposed converter, the voltage stress on the semiconductor devices is significantly less than of its counterparts. Also, it can be concluded that the novel SIDO-TLC is among the high-efficiency multiport dc-dc converters.

V. CONCLUSION

This paper proposed a high-efficiency non-isolated SIDO-TLC, whose outputs are boost and buck simultaneously. Owing to the converter's three-level control and structure, the voltage stress across the semiconductor devices is only half as much as the boost output voltage. Also, the size of the inductors shrank, and the step-down terminal's capacitor volume was reduced so dramatically that a small 4.5 μ F film capacitor was used in the experimental prototype. The results showed that the proposed converter was well stable under dynamic changes. Meanwhile, the converter's two split series capacitors at the step-up terminal and also its highly effective balancing control makes it attractive for applications such as the three-level diode

clamped inverters in which the dc link capacitors voltage balancing is of great importance.

APPENDIX

CONTROL TRANSFER FUNCTION COEFFICIENTS [(16) – (18)]

$$\hat{v}_{o1}/\hat{d}_2:$$

$$\alpha_3 = -2.184E5, \alpha_2 = 1.084E10, \alpha_1 = 7.84E13, \alpha_0 = 2.996E18, \\ \beta_3 = 1.191E4, \beta_2 = 3.572E8, \beta_1 = 8.048E11, \beta_0 = 1.15E16, \\ \alpha'_4 = -2.249E5, \alpha'_3 = 1.077E10, \alpha'_2 = 7.644E13, \alpha'_1 = 2.995E18, \\ \alpha'_0 = -6.874E17, \beta'_4 = 1.191E04, \beta'_3 = 3.572E08, \beta'_2 = 8.049E11, \\ \beta'_1 = 1.151E16, \beta'_0 = 3.281E15.$$

$$\hat{v}_{o2}/\hat{d}_1:$$

$$\gamma_1 = -2.906E13, \gamma_0 = 8.627E17, \delta_3 = 1.191E4, \delta_2 = 3.572E8, \\ \delta_1 = 8.048E11, \delta_0 = 1.15E16, \gamma'_2 = -2.963E13, \gamma'_1 = 8.629E17, \\ \gamma'_0 = 1.51E17, \delta'_4 = 1.191E4, \delta'_3 = 3.572E8, \delta'_2 = 8.049E11, \\ \delta'_1 = 1.151E16, \delta'_0 = 3.281E15.$$

$$\Delta\hat{v}_c/\Delta\hat{d}:$$

$$\lambda_0 = -5.545E5, \lambda'_4 = -5.675E5, \lambda'_3 = -6.761E9, \lambda'_2 = -2.027E14, \\ \lambda'_1 = -4.567E17, \lambda'_0 = -6.528E21, \xi'_4 = 1.191E4, \\ \xi'_3 = 3.572E8, \xi'_2 = 8.049E11, \xi'_1 = 1.151E16, \xi'_0 = 3.281E15.$$

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