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Model Predictive Control with Power Self-balancing of the Output Parallel DAB DC-DC Converters in Power Electronic Traction Transformer

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Abstract- This paper focuses on the output parallel dual active bridge (DAB) dc-dc converters in power electronic traction transformers (PETT). A model predictive control with current-stress-optimized (MPC-CSO) scheme based on dual phase-shift (DPS) is proposed to improve the dynamic performance, balance the transmission power, and realize the current stress optimization. The dynamic behavior of output voltage in the next horizon is predicted accurately under the input voltage fluctuation and load disturbance conditions by developing the prediction model. In addition, the proposed MPC-CSO with DPS scheme can realize the output voltage to track the desired value directly with no overshoot during the start-up process. Combining the model predictive control and current-stress optimized scheme, the fast dynamic response and high-efficiency performance of DAB converters can be realized simultaneously. And the transmission power of each DAB cell can be self-balanced. Finally, three control schemes consisting of traditional voltage closed-loop control (TVCL) with single phase-shift (SPS), traditional CSO control with DPS, and MPC-CSO with DPS schemes are compared in a scale-down three DAB dc-dc converter cells experimental prototype by using TMS320F28335+FPGA_6SLX45 as core controller. And extensive experimental results have verified the excellent performance of the proposed MPC-CSO scheme and associated analysis in this work.

***Index Terms*—Power electronic traction transformer (PETT), dual active bridge (DAB) dc-dc converter, predictive control, power balance control, efficiency, dynamic performance.**

I. INTRODUCTION

In recent years, remarkable progress has been made in the high-speed railway, which has greatly changed the way of people's daily travel and boosted the economic development. However, the bulky and low-efficiency line-frequency transformer is utilized to realize electrical isolation and voltage matching in the traditional locomotive traction unit, which leads to large energy consumption of the high-speed train and low power density of the traction onboard equipment. Thus, power electronic traction transformers (PETT) with the salient features of energy-saving, low-carbon, high-power density, environmental protection are considered as the core equipment of next generation high-speed trains [1, 2].

After many years of development, the topology of PETT has formed a representative three stage structure [3] shown in Fig. 1, consisting of a single-phase cascade H-bridge (CHB) converter, the output parallel dual active bridge (DAB) dc-dc converters with medium/high frequency transformers and a three-phase inverter.

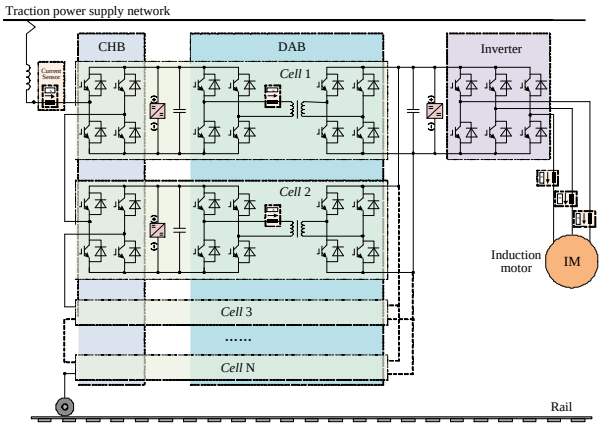

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Fig.1 The topology of train traction drive system with power electronic traction transformer

In practice, due to the circuit parameter mismatch such as storage inductor in DAB converters, transmission power unbalance problem cannot be avoided [4]. It may cause high current stress, low efficiency, large current/voltage deviation and even the breakdown of power devices if the balancing control scheme is not adopted [5, 6]. So it is significant to keep the transmission power balance between different PETT cells.

In order to balance the voltage in CHB stage as well as the power in the DAB stage with parameter mismatch, a voltage and power control scheme is proposed in [7] to balance dc-link capacitor voltages of the adopted CHB converter and the actual power through the parallel DAB modules. Although the proposed scheme is simple, the high-frequency inductor current sensors are necessary in all DAB modules, which leads an increase of system cost greatly. In addition, a coordinating control solution for the CHB and DAB converters without inductor current sensors is proposed in [8]. A common duty ratio controller for the CHB stage in the single phase d-q coordinate and feedback feed-forward controller for the DAB stage are adopted in the coordinating control scheme. Although the scheme gets rid of the inductor current sensor in the DAB converters, the efficiency and dynamic performance of the scheme is a little poor.

For the transformerless train traction drive system shown in Fig.1, there always exists twice-grid-frequency ripple in dc-link voltage of the CHB converter, which may result in the beat frequency phenomenon of traction motor [9]. Thus, the fast dynamic response of DAB converters in PETT is necessary to face with the input voltage fluctuation. In [10, 11], the state space averaging model and small signal model of DAB converters based on the single-phase-shift (SPS) control are constructed to analyze the dynamic characteristics, and then a model-based feed-forward control scheme is proposed to improve the dynamic response. Similarly, a feed-forward compensation control scheme for DAB converters is proposed in [12] by developing a linearized dynamic harmonic model to enhance the load step-change response. But the linearized harmonic model of DAB converters is very complicated and the scheme is realized with off-line lookup table solution, so it's not suitable for modularization. Furthermore, a simple virtual direct power control scheme based on SPS control is proposed in [13]. The control scheme can achieve excellent dynamic performance under the input voltage fluctuation and load disturbance conditions for DAB converters. However, in traditional SPS control, power flow of the DAB converter is mainly dependent on the transformer leakage inductor that will cause high current stress when the voltage transfer ratio deviates far from one [14-16]. Thus, control performance of the virtual direct power control scheme combined with other phase-shift control method needs to be discussed and verified in further.

As a result, in order to overcome the shortcomings of SPS control and improve the efficiency of DAB converters, various optimized phase-shift control strategies are reported, including dual phase-shift (DPS) control [17], extended phase-shift (EPS) control [18] and triple phase-shift (TPS) control [19]. Meanwhile, the corresponding efficiency optimization control schemes for DAB converters are discussed in [20-26]. But most of these control schemes require off-line computations according to various operating conditions due to its complexity, so it is difficult to implement in multiple DAB modules. For the output parallel DAB modules in PETT, the control scheme should be as simple as possible besides the dynamic and efficiency performance improvement. However, throughout the existing literatures, the control scheme that is suitable for the output parallel DAB modules in PETT is rarely reported.

In recent years, model predictive control (MPC) has been widely reported and applied in PWM rectifiers [27], grid-side inverters [28], motor drives [29] and other fields [30] to achieve fast dynamic response and reduce current harmonics. However, most of the conclusions about MPC scheme applied in DAB dc-dc converters need the time-consuming trial-and-error tuning procedure to achieve satisfactory performance, which results in slow dynamic response and abundant computational burden for the controller [31-33].

Aimed at improving dynamic response and balancing the transmission power on the premise of realizing efficiency optimization for parallel DAB modules in PETT on-line and in real-time, a simple model predictive control with current-stress-optimized (MPC-CSO) scheme based on DPS control is proposed in this paper. For dynamic performance improvement, the prediction model of output voltage for DAB dc-dc converters under DPS control is developed to predict dynamic behavior of

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the output voltage under the input voltage fluctuation and load disturbance conditions. Meanwhile, combining the CSO scheme, the efficiency of DAB converters can be enhanced on the basis of maintaining the excellent dynamic performance and realizing the transmission power self-balance.

The rest of the paper is organized as the following: In Section II, the current-stress optimization under DPS control is analyzed. In Section III, the prediction model of output voltage is described, and the predicted phase-shift ratios are estimated and deduced. On the basis of this, Section IV shows a comprehensive description of MPC-CSO scheme under DPS control for DAB dc-dc converters, especially for the transmission power self-balancing. In Section V, a scale-down three cells experimental platform is designed to verify the theoretic analysis and the proposed scheme by comprehensive experimental comparison of traditional voltage closed-loop (TVCL) control with SPS control, traditional CSO with DPS control [23] and MPC-CSO scheme with DPS control. Finally, the work is concluded in Section VI

II. Current Stress Optimization Analysis Under DPS Control

A. Switching Control Analysis of DPS Control

The output parallel DAB modules in PETT can be equivalent to the input independent output parallel (IIOP) connected converters when the CHB converter controls intermediate-dc-voltage balance [7]. And the equivalent circuit composed of N DAB cells is shown in Fig. 2, where C_{gi} and C_{fi} are the dc input and output capacitors of the i-th DAB cell respectively; L_i is the energy-storage inductor of the i-th DAB cell; U_{abi} and U_{cdi} are the equivalent ac output voltages of two H-bridges on the primary and secondary sides of the mediate/high frequency transformer, respectively; and the turn radio of the transformer is n; U_{dci} and i_{oi} are the input voltage and output current of the i-th DAB cell; U_o is the output voltage of the parallel DAB modules while i_o is the load current; and R is the load resistance.

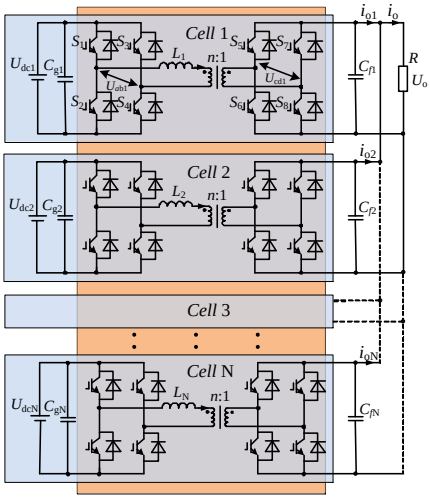

Fig.2 The equivalent input independent output parallel connection circuit of DAB converters in PETT

Taking the i-th DAB cell as an example to simplify analysis and calculation, the main waveforms of DAB converter in DPS control can be divided into two conditions [23]: $0 \le D_{i1} \le D_{i2} \le 1$ and $0 \le D_{i2} \le D_{i1} \le 1$, as shown in Fig. 3, where D_{i1} and D_{i2} are the inner and outer phase-shift ratios of the i-th DAB cell, respectively; T_s represents a switching cycle; and i_{Li} is the inductor current. In addition, the phase-shift angle between the output voltage U_{abi} of primary H bridge in each DAB cell is $360°/N$ to reduce the output voltage ripple [7].

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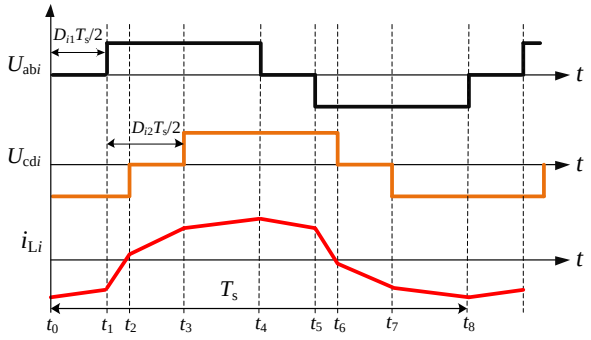
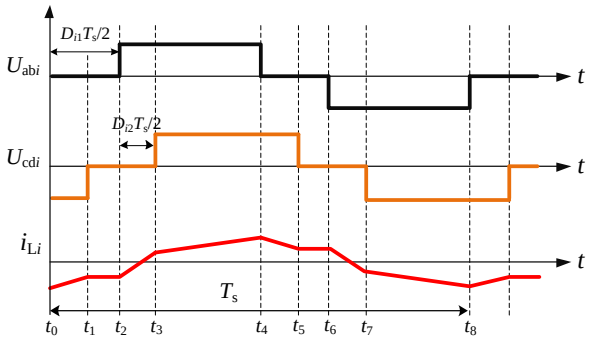


(a) $0 \le D_{i1} \le D_{i2} \le 1$



(b) $0 \le D_{i2} \le D_{i1} \le 1$

Fig. 3 The voltage and current waveforms of the *i*-th DAB cell in DPS control

Assuming voltage transfer ratio $k_i=U_{dci}/nU_o$, and $k_i \ge 1$ (the other condition $k_i<1$ can be analyzed similarly), the average transmission power of the *i*-th DAB cell with DPS control can be expressed as follows [23]:

$$P_{D_i} = \frac{1}{T_s}\int_0^{T_s} U_{ab_i} i_{L_i}(t)dt = \begin{cases} \dfrac{nU_{dci}U_o}{4fL_i}(2D_{i2} - D_{i1}^2 - 2D_{i2}^2), & 0 \le D_{i1} \le D_{i2} \le 1 \\ \dfrac{nU_{dci}U_o}{4fL_i}(2D_{i2} - 2D_{i1}D_{i2} - D_{i2}^2), & 0 \le D_{i2} \le D_{i1} \le 1 \end{cases} \tag{1}$$

where $f=1/T_s$ is the switching frequency. And the inductor current stress of the *i*-th DAB cell with DPS control can be derived as

$$I_{pD_i} = \max\left\{\left|i_{L_i}(t)\right|\right\} = \frac{nU_o}{4fL_i}[(k_i - 1)(1 - D_{i1}) + 2D_{i2}] \tag{2}$$

According to (1) and (2), the unified transmission power and current stress of the *i*-th DAB cell in DPS control can be deduced as,

$$\begin{cases} p_{D_i} = \dfrac{P_{D_i}}{P_{N_i}} = \begin{cases} 2(2D_{i2} - D_{i1}^2 - 2D_{i2}^2), & (0 \le D_{i1} \le D_{i2} \le 1) \\ 2(2D_{i2} - 2D_{i1}D_{i2} - D_{i2}^2), & (0 \le D_{i2} \le D_{i1} \le 1) \end{cases} \\ i_{pD_i} = \dfrac{I_{pD_i}}{I_{N_i}} = 2\left[(k_i - 1)(1 - D_{i1}) + 2D_{i2}\right] \end{cases} \tag{3}$$

where P_{Ni} and I_{Ni} are the maximum transmission power and the maximum average value of input current of the *i*-th DAB cell under SPS control, respectively, i.e.,

$$\begin{cases} P_{N_i} = \dfrac{nU_{dci}U_o}{8fL_i} \\ I_{N_i} = \dfrac{P_N}{U_{dci}} = \dfrac{nU_o}{8fL_i} \end{cases} \tag{4}$$

Similarly, the unified transmission power and current stress of the *i*-th DAB cell under SPS control can be obtained as,

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$$\begin{cases} p_{S_i} = 4D_i(1-D_i) & (0 \le D_i \le 1) \\ i_{pS_i} = 2(2D_i - 1 + k_i) \end{cases} \tag{5}$$

B. Current-Stress-Optimized control Based on Lagrange Multiplier Method

Lagrange multiplier method (LMM) is one of the most frequently-used optimization methods to solve the extreme optimization problem with equivalent constraint, which can obtain the simple relationship between phase-shift ratios to realize the current stress optimal control for the DAB converters.

Firstly, the relationship between D_{i1} and D_{i2} is described by using LMM for the i-th DAB cell under DPS control as,

$$E_i = i_{pD_i} + \lambda(p_{D_i} - p_i^*) \tag{6}$$

where E_i is the Lagrangian function; λ is the Lagrangian multiplier; and p_i^* is the unified transmission power reference value of the i-th DAB cell.

Meanwhile, the relationship between D_{i1} and D_{i2} of the i-th DAB cell can be described by LMM,

$$\begin{cases} \dfrac{\partial E_i}{\partial D_{i1}} = 0 \\ \dfrac{\partial E_i}{\partial D_{i2}} = 0 \end{cases} \tag{7}$$

Substituting (3) and (6) into (7), the phase-shift ratios D_{i1} and D_{i2} can be derived as,

$$D_{i2} = \begin{cases} \dfrac{k_i - 1 - 2D_{i1}}{2(k_i - 1)} & (\dfrac{k_i^2 + 2k_i - 3}{2k_i^2} \le p_{D_i} \le 1) \\ \dfrac{(k_i - 1)(1 - D_{i1})}{k_i + 1} & (0 \le p_{D_i} < \dfrac{k_i^2 + 2k_i - 3}{2k_i^2}) \end{cases} \tag{8}$$

Combining (3) and (8), the phase-shift ratios D_{i1} and D_{i2} of the i-th DAB cell under DPS control can be further expressed as,

$$\begin{cases} \begin{cases} D_{i1} = (k_i - 1)\sqrt{\dfrac{1 - p_{D_i}}{2(k_i^2 - 2k_i + 3)}} \\ D_{i2} = \dfrac{1}{2} - \sqrt{\dfrac{1 - p_{D_i}}{2(k_i^2 - 2k_i + 3)}} \end{cases} & (\dfrac{k_i^2 + 2k_i - 3}{2k_i^2} < p_{D_i} \le 1) \\ \begin{cases} D_{i1} = 1 - \sqrt{\dfrac{p_{D_i}(k_i - 1)}{2(k_i + 3)}} - \sqrt{\dfrac{2p_{D_i}}{(k_i - 1)(k_i + 3)}} \\ D_{i2} = \dfrac{p_{D_i}(k_i - 1)}{2(k_i + 3)} \end{cases} & (0 \le p_{D_i} \le \dfrac{k_i^2 + 2k_i - 3}{2k_i^2}) \end{cases} \tag{9}$$

where the power range $0 \le p_{Di} < (k_i^2 + 2k_i - 3)/(2k_i^2)$ is corresponding to the phase-shift condition $0 \le D_{i2} \le D_{i1} \le 1$, and the power range $(k_i^2 + 2k_i - 3)/(2k_i^2) \le p_{Di} \le 1$ is corresponding to the phase-shift condition $0 \le D_{i1} \le D_{i2} \le 1$.

Based on (2), (5) and (9), the unified current-stress of the i-th DAB cell under DPS and SPS controls can be deduced with the voltage transfer ratio and the unified transmission power as,

$$\begin{cases} i_{pD_i} = \begin{cases} 2k_i - \sqrt{2(1 - p_{D_i})(k_i^2 - 2k_i + 3)} & (\dfrac{k_i^2 + 2k_i - 3}{2k_i^2} < p_{D_i} \le 1) \\ \sqrt{2p_{D_i}(k_i - 1)(k_i + 3)} & (0 \le p_{D_i} \le \dfrac{k_i^2 + 2k_i - 3}{2k_i^2}) \end{cases} \\ i_{pS_i} = 2k_i - 2\sqrt{1 - p_{S_i}} \qquad (0 \le p_{S_i} \le 1) \end{cases} \tag{10}$$

where i_{pDi} and i_{pSi} are the unified current stress of the i-th DAB cell under DPS and SPS control schemes, respectively.

And the premise of comparison is that the transmission power of the i-th DAB cell under DPS and SPS control schemes

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is equal, e.i. satisfies $p_{Di}=p_{Si}= p_i$. For the convenience of analysis, the current-stress ratio M_{pi} from i_{pDi} to i_{pSi} of the i-th DAB cell is defined as,

$$M_{p_i}=\frac{i_{pS_i}}{i_{pD_i}}=\begin{cases}\dfrac{2k_i-2\sqrt{1-p_i}}{2k_i-\sqrt{2(1-p_i)(k_i^2-2k_i+3)}} & (\dfrac{k_i^2+2k_i-3}{2k_i^2}<p_i\le 1)\\ \dfrac{2k_i-2\sqrt{1-p_i}}{\sqrt{2p_i(k_i-1)(k_i+3)}} & (0\le p_i\le\dfrac{k_i^2+2k_i-3}{2k_i^2})\end{cases} \tag{11}$$

Thus, the 3-D curves of the current-stress ratio M_{pi} with respect to p_i and k_i is shown in Fig. 4.

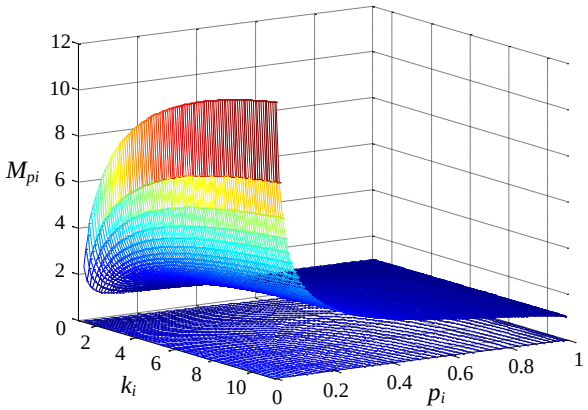

Fig. 4 The 3-D curves of the current-stress ratio M_{pi} with respect to p_i and k_i

It is clear that the current-stress ratio M_{pi} increases with the decrease of the unified transmission power p_i for the given voltage transfer ratio k_i. And for the given unified transmission power p_i, the current-stress ratio M_{pi} increases with the increase of the voltage transfer ratio k_i. Thus, DPS control can reduce the current-stress significantly, especially for high voltage transfer ratio and light load condition. Based on the above analysis, Fig. 5 shows the block diagram of traditional CSO scheme based on DPS control for DAB dc-dc converters [23].

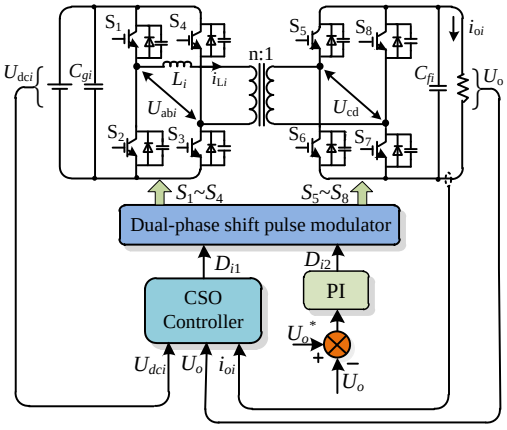

Fig. 5 The block diagram of traditional CSO scheme based on DPS control for DAB dc-dc converters

In traditional CSO scheme, it is obvious that the proportion and integral (PI) controller is adopted to control the power, and the inner phase-shift ratio is calculated according to (9). Although the scheme can realize the current stress optimization and efficiency improvement, the dynamic performance of converters is poor due to the use of integrator in PI regulator, and the scheme is not suitable to the output parallel DAB dc-dc converter because the transmission power balance cannot be kept.

III. Model Predictive Control Scheme For DAB Converters Under DPS Control

A. State Space Averaging Model of DAB Converters in DPS Control

For MPC scheme, mathematical models of power electronic converters are the basis to design the controller. Generally, the inductor current and capacitor voltage are chosen as state variables to construct the average model. For the DAB converters

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in PETT, the control objective is to track the output voltage with the desired value, and the input capacitors mainly play the role of voltage support. Meanwhile, from Fig. 3, it can be known that the inductor current is a purely ac component and its dc term is zero, so it is meaningless for the inductor current to averaging model. Thus, only the output capacitor voltage is selected to develop the state space averaging model.

Taking the condition $0\le D_{i1}\le D_{i2}\le 1$ as an example and combining Fig. 3, it can be obtained that there are eight operation modes in a switching cycle for the adopted DAB cell. However, it can be noticed that the state space averaging model can be described in half a switching cycle due to the waveform symmetry of inductor current and output voltage of H-bridges. Thus, the inductor current of the *i*-th DAB cell at each instant time can be expressed as follows,

$$\begin{cases} i_{L_i}(t_0)=\dfrac{nU_o}{4fL_i}\left[(D_{i1}-1)k_i-(2D_{i2}+D_{i1}-1)\right] \\ i_{L_i}(t_1)=\dfrac{nU_o}{4fL_i}\left[(D_{i1}-1)k_i+(1+D_{i1}-2D_{i2})\right] \\ i_{L_i}(t_2)=\dfrac{nU_o}{4fL_i}\left[(2D_{i2}-D_{i1}-1)k_i+(1-D_{i1})\right] \\ i_{L_i}(t_3)=\dfrac{nU_o}{4fL_i}\left[(2D_{i2}+D_{i1}-1)k_i-(D_{i1}-1)\right] \\ i_{L_i}(t_4)=\dfrac{nU_o}{4fL_i}\left[1-D_{i1})k_i+(2D_{i2}+D_{i1}-1)\right] \end{cases} \tag{12}$$

Applying Kirchhoff current law (KCL) in the load side, four differential equations can be derived, corresponding to four operation states for the *i*-th DAB cell respectively. Based on Fig. 2 and Fig. 3, it can be known that relationship between inductor current, load current and capacitor current is mainly related to the ac output voltage U_{cdi} of secondary H-bridge. Thus, the differential equations of output capacitor voltage for the *i*-th DAB cell can be expressed as follows,

$$\begin{cases} C_{fi}\dfrac{dU_o}{dt}=-\overline{i}_{L1_i}-i_{oi} & t\in[0,\dfrac{D_{i1}T_s}{2}] \\ C_{fi}\dfrac{dU_o}{dt}=-\overline{i}_{L2_i}-i_{oi} & t\in[\dfrac{D_{i1}T_s}{2},\dfrac{D_{i2}T_s}{2}] \\ C_{fi}\dfrac{dU_o}{dt}=-i_{oi} & t\in[\dfrac{D_{i2}T_s}{2},\dfrac{(D_{i1}+D_{i2})T_s}{2}] \\ C_{fi}\dfrac{dU_o}{dt}=\overline{i}_{L4_i}-i_{oi} & t\in[\dfrac{(D_{i1}+D_{i2})T_s}{2},\dfrac{T_s}{2}] \end{cases} \tag{13}$$

where $\overline{i}_{L1_i}$, $\overline{i}_{L2_i}$ and $\overline{i}_{L4_i}$ are the average values of inductor current of the *i*-th DAB cell in corresponding time interval, which can be expressed as,

$$\begin{cases} \overline{i}_{L1_i}=\dfrac{i_{L_i}(t_0)+i_{L_i}(t_1)}{2} \\ \overline{i}_{L2_i}=\dfrac{i_{L_i}(t_1)+i_{L_i}(t_2)}{2} \\ \overline{i}_{L4_i}=\dfrac{i_{L_i}(t_3)+i_{L_i}(t_4)}{2} \end{cases} \tag{14}$$

However, each differential equation in (13) only represents the relationship of voltage and current in the adopted operating interval. Thus, the differential equation that can describe the system characteristic of the *i*-th DAB cell throughout the switching period is needed to be developed. Combining (12), (13) and (14), the state space averaging model of the *i*-th DAB cell under DPS control can be derived according to time-averaging principle as follows,

$$C_{fi}\frac{dU_o}{dt}=\frac{2D_{i2}(1-D_{i2})-D_{i1}^2}{4fL_i}U_{dci}-i_{oi} \tag{15}$$

Similarly, when the relationship between the inner and outer phase-shift ratios meets the condition $0\le D_{i2}\le D_{i1}\le 1$, the state space averaging model of the *i*-th DAB cell under DPS control can be obtained as,

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$$C_{fi}\frac{dU_o}{dt}=\frac{D_{i2}(2-2D_{i1}-D_{i2})}{4fL_i}U_{dci}-i_{oi} \tag{16}$$

B. Development of Output Voltage Prediction Model

In order to predict the output voltage in the next switching cycle according to the circuit parameters and the sampling information at the current moment, a prediction model of the output voltage needs to be shown. Taking the condition $0\le D_{i1}\le D_{i2}\le 1$ as an example, it can be noticed that the differential term of output voltage reflects variation tendency of the output voltage. Thus, the differential term of the output voltage in (15) can be discretized by utilizing Forward Euler method as,

$$\frac{dU_o}{dt}=\frac{U_{oi}(t_{k+1})-U_o(t_k)}{t_{k+1}-t_k}=\frac{U_{oi}(t_{k+1})-U_o(t_k)}{T_s} \tag{17}$$

where $U_o(t_k)$ represents the sampling output voltage at the kth sampling instant, while $U_{oi}(t_{k+1})$ is the predictive output voltage at the $(k+1)$th instant.

By substituting (17) into (15), a prediction model of the output voltage for the i-th DAB cell under DPS control can be expressed as,

$$U_{oi}(t_{k+1})=U_o(t_k)+\frac{2D_{i2}(1-D_{i2})-D_{i1}^2}{4f^2L_iC_{fi}}U_{dci}(t_k)-\frac{i_{oi}(t_k)}{fC_{fi}} \tag{18}$$

where $U_{dci}(t_k)$ and $i_{oi}(t_k)$ represent the sampling input voltage and output current of the i-th DAB cell at the kth sampling instant, respectively.

Similarly, when the relationship between the inner and outer phase-shift ratios meets the condition $0\le D_{i2}\le D_{i1}\le 1$, the prediction model of output voltage for the i-th DAB cell under DPS control can be derived as,

$$U_{oi}(t_{k+1})=U_o(t_k)+\frac{D_{i2}(2-2D_{i1}-D_{i2})}{4f^2L_iC_{fi}}U_{dci}(t_k)-\frac{i_{oi}(t_k)}{fC_{fi}} \tag{19}$$

Based on (18) and (19), the dynamic behavior of the output voltage, with respect to the variation of input voltage and desired voltage, can be predicted to analyze dynamic performance of the adopted DAB dc-dc converter.

C. Calculation and Compensation of the Optimal Phase-Shift Ratio

The cost function is an important segment in MPC scheme. In order to obtain the optimal phase-shift ratio to track the output voltage with the desired value rapidly and accurately under all operating conditions, the cost function can be defined as the square of the difference between the predicted output voltage and the desired voltage as,

$$J_i=[U_{oi}(t_{k+1})-U_o^*(t_k)]^2 \tag{20}$$

where $U_o^*(t_k)$ is the desired output voltage at kth instant time, and J_i is the cost function of the i-th DAB cell.

It is clear that the smaller the cost function is, the closer the output voltage is to the desired value. Thus, the relationship between the inner and outer phase-shift ratios that minimizes cost function can be derived from cost function derivation with respect to D_{i2} i.e.,

$$\frac{\partial J_i}{\partial D_{i2}}=0 \tag{21}$$

Taking the condition $0\le D_{i1}\le D_{i2}\le 1$ as an example, according to (18), (20) and (21), the predicted phase-shift ratio D_{i2} can be expressed as,

$$D_{i2}=\frac{1}{2}-\sqrt{\frac{1}{4}-\frac{D_{i1}^2}{2}-\frac{2fL_ii_{oi}(t_k)+2f^2L_iC_{fi}(U_o^*(t_k)-U_o(t_k))}{U_{dci}(t_k)}} \tag{22}$$

According to (22), Fig. 6 shows the curve of the predicted phase-shift ratio with respect to the normalized output voltage to reflect the essence of MPC scheme for DAB dc-dc converters more clearly. The simulation parameters are same as the

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experimental parameters (cell 1) shown in Table I, and D_{11} are set as 0.1.

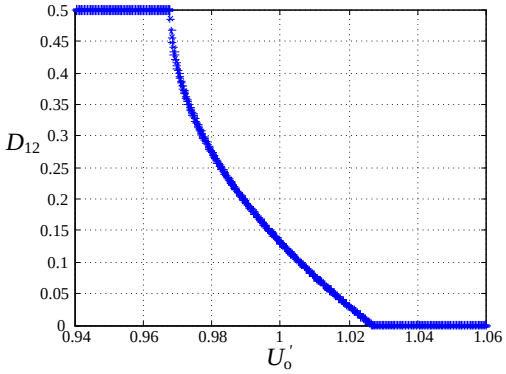

Fig. 6 The curve of the predicted phase-shift ratio with respect to normalized output voltage.

where $U'_o(t_k)$ is the normalized output voltage, and defined as $U'_o(t_k)= U_o(t_k) /U_o^*$.

It can be seen that there is an approximately linear regulatory region when the output voltage is closed to the desired value. Thus, it is clear that MPC scheme is realized by combining the nonlinear characteristic of DAB converter itself, which is also the reason that the dynamic performance of MPC scheme is better than other linear control methods. In addition, when the output voltage is far away from the desired value, the controller always adjust the converter with the greatest effort (D_{12} reaches the boundary) to track the output voltage with the desired value again.

However, the transmission power model in (1) and the inductor current value in (12) of DAB converters are not accurate in the practical application because of switch parameters mismatch, dead time and perform precision of micro-controller etc., which directly causes the error between the prediction model and the physical model of DAB converters. Thus, a virtual dynamic voltage compensation component ΔU_o is adopted to adjust the prediction model as accurate as possible on the basis of the estimated steady operation point according to (22). And ΔU_o only acts as dynamic compensation without affecting other performance because the predicted phase-shift ratio is quite close to the desired value.

Thus, (22) can be rewritten as,

$$D_{i2} = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{D_{i1}^2}{2} - \frac{2fL_i i_{oi}(t_k) + 2f^2 L_i C_{fi}(U_o^*(t_k) - U_o(t_k) + \Delta U_o(t_k))}{U_{dci}(t_k)}} \tag{23}$$

And $\Delta U_o(t_k)$ is set as the output value of PI voltage controller with the difference between the desired voltage and the sampling output voltage as the input value.

Similarly, when the relationship between the inner and outer phase-shift ratios meets the condition $0 \le D_{i2} \le D_{i1} \le 1$, the predicted phase-shift ratio D_{i2} can be expressed as,

$$D_{i2} = 1 - D_{i1} - \sqrt{(1-D_{i1})^2 - \frac{4fL_i i_{oi}(t_k) + 4f^2 L_i C_{fi}(U_o^*(t_k) - U_o(t_k) + \Delta U_o(t_k))}{U_{dci}(t_k)}} \tag{24}$$

IV. Model Predictive Control with Current-Stress- Optimized Scheme Under DPS Control

A. Power Self-balancing control

For the output parallel DAB dc-dc converters in practical application, there is always existing the differences between the main circuit parameters (such as storage inductors) of each cells. Thus, it can be known that transmission power is unbalanced if there is no power balance control in the existing control methods.

From Fig. 5, it can be seen that the outer phase-shift ratio is obtained by PI controller, and the inner phase-shift ratio is calculated according to the sampling voltage, current and the circuit parameter in the traditional CSO scheme. However, when the voltage transfer ratio k_i is close to one, the inner phase-shift ratio is close to zero, and the DPS control can be approximately equivalent to SPS control. Therefore, all the DAB cells is applied to the same outer phase-shift ratio based on PI controller.

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According to (1), it can be known that the transmission power of DAB cell with smaller inductance is larger, and the corresponding current stress is larger. When the voltage transfer ratio k_i is far from one, the inner phase-shift ratio is applied to reduce the current stress and improve the efficiency. Because the inner phase-shift ratio is estimated with relation to the storage inductance, thus the degree of transmission power balance under DPS control is better than SPS control. Meanwhile, in traditional CSO scheme, the closer voltage transfer ratio k_i is to one, the more terrible the unbalanced degree of transmission power is.

In order to realize the transmission power balance in various operation conditions, the prediction model in (18) and (19) need to be reconstructed, and the output current of each DAB cell should satisfy,

$$i_{o1} = i_{o2} = \cdots = i_{oi} = \cdots = i_{oN} = \frac{i_o}{N} \tag{25}$$

By substituting (25) into (23) and (24), the predictive phase-shift ratio for the condition $0 \le D_{i1} \le D_{i2} \le 1$ can be rewritten as,

$$D_{i2} = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{D_{i1}^2}{2} - \frac{2fL_i i_o(t_k) + 2Nf^2 L_i C_{fi}(U_o^*(t_k) - U_o(t_k) + \Delta U_o(t_k))}{NU_{dci}(t_k)}} \tag{26}$$

And the predictive phase-shift ratio for the condition $0 \le D_{i2} \le D_{i1} \le 1$ can be rewritten as,

$$D_{i2} = 1 - D_{i1} - \sqrt{(1 - D_{i1})^2 - \frac{4fL_i i_o(t_k) + 4Nf^2 L_i C_{fi}(U_o^*(t_k) - U_o(t_k) + \Delta U_o(t_k))}{NU_{dci}(t_k)}} \tag{27}$$

From (26) and (27), it can be known that the outer phase-shift ratio is estimated with relative to the inductance values even if the inner phase-shift ratio is zero. Thus, the proposed MPC scheme can realize self-balance of the transmission power in various operation conditions.

B. MPC-CSO Scheme under DPS Control

Generally, in most optimization algorithms of DAB dc-dc converters, the calculated phase-shift ratios according to (9) can't be applied to the converter directly. Instead, a PI controller is adopted to adjust one phase-shift ratio to boost the converter to the desired power, and then the other phase-shift ratios are calculated with lookup table or the unified transmission power and the voltage transfer ratio to achieve optimal control. It is no doubt that it leads to the poor dynamic performance of DAB dc-dc converters. In order to realize a comprehensive performance optimization, including excellent dynamic performance and high efficiency, the model predictive control with current-stress-optimized (MPC-CSO) scheme under DPS control is proposed.

For the *i*-th DAB cell, MPC-CSO scheme can be implemented by the following steps: firstly, the unified transmission power p_i and the voltage transfer ratio k_i are calculated with the sampling voltage and current. The unified transmission power p_i can be estimated from (28), and the voltage transfer ratio k_i can be calculated with U_o^* to avoid that k_i is closed to infinitely large because U_o is very small during the start-up stage. Then, the optimal phase-shift ratios D_{i1} can be obtained from (9) by judging the power range according to k_i and p_i. Finally, D_{i2} can be calculated from (26) and (27). Obviously, when the converter reaches the desired power, the phase-shift ratio D_{i2} is unique if D_{i1} is obtained from (9). The current-stress control can be achieved by applying D_{i1} calculated from (9), because the MPC control is essentially equivalent to power control and the converter can be boosted to the desired power with (26) or (27) based on the aforementioned analysis.

$$p_i = \frac{U_o i_o}{NP_N} = \frac{8fL_i i_o}{nNU_{dci}} \tag{28}$$

The block diagram of the proposed MPC-CSO scheme under DPS control for parallel DAB dc-dc converters in PETT can be summarized in Fig. 7.

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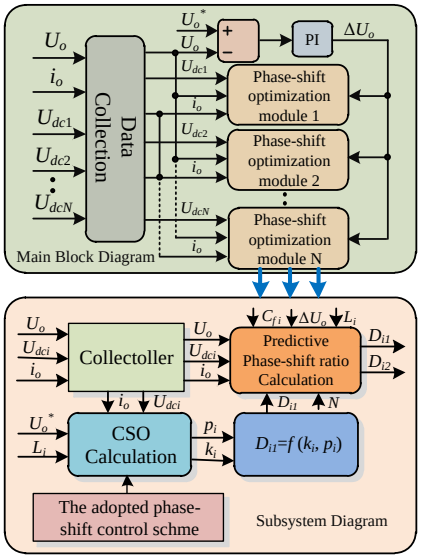

Fig. 7 Block diagram of the proposed MPC-CSO scheme for parallel DAB dc-dc converters in PETT.

As it can be seen, the proposed MPC-CSO scheme under DPS control for parallel DAB dc-dc converters in PETT can be realized based on (9), (26), (27) and (28). In addition, when the output voltage are close to the desired voltage with the predictive control, the transmission power is also close to the desired value. Thus, dynamic performance of the control system is just a little bit relative to the PI controller and it can maintain excellent dynamic performance in a wider power range than traditional CSO scheme.

V EXPERIMENTS

In order to verify the effectiveness of the proposed MPC-CSO scheme in this paper, a scale-down three cells experimental platform is developed with TMS320F28335+FPGA_6SLX45 as the main digital controller. A photo of the experimental prototype with three-cells is shown in Fig. 8.

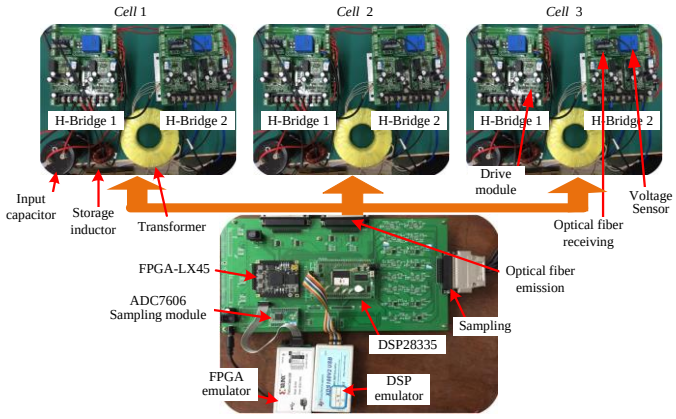

Fig.8 A photo of the scale-down experimental hardware prototype with three cells

And electrical parameters of the adopted prototype are shown in Table I.

TABLE I

ELECTRICAL PARAMETERS OF THE DAB DC-DC CONVERTER EXPERIMENTAL PROTOTYPE WITH THREE CELLS

Parameters	Value
Transformer voltage ratio	n=1
Switching frequency	f= 10kHz
Inductor of Cell 1	L_1=184.5μH
Inductor of Cell 2	L_2=352μH
Inductor of Cell 3	L_3=226.7μH

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Input-side capacitor	C_{g1}= C_{g2}= C_{g3}=1.12mF
Output-side capacitor	C_{f1}= C_{f2}= C_{f3}=1.12mF
load resistor	R=30/20/10Ohm

Due to the restriction of the hardware resource port of the DSP controller, the control system of three cells experimental platform is realized with DSP and FPGA at the same time, and both of them exchange data through a dual port virtual RAM inside the FPGA. The structure diagram of the control system is shown in Fig. 9.

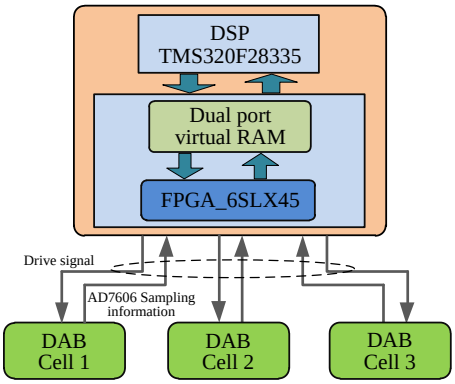
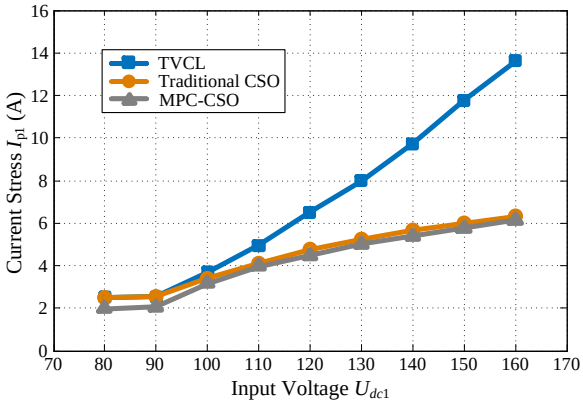


Fig.9 The structure diagram of the control system

Specifically, the voltage and current signals are sampled through the AD7606 sampling module, and then FPGA controller sends the sampled data to DSP controller through the dual port virtual RAM. After completing the numerical calculation of control scheme by DSP controller, the optimized phase shift is transmitted to FPGA controller. Finally, the corresponding driving pulse is generated by the FPGA controller.

A. Experimental Comparison of Current Stress and Efficiency

When the experimental parameters are set as U_o^*=80V, R=20Ω, Fig. 10 shows the inductor current stress of DAB cell 1 and the efficiency with respect to the input voltage under TVCL control, traditional CSO control [23] and the proposed MPC-CSO control schemes, respectively. Obviously, the current stress increases sharply with an increase of the input voltage under TVCL scheme, which results in large conduction loss and low efficiency of DAB converters. In the traditional CSO and proposed MPC-CSO schemes, it can be seen that the current stress can be reduced significantly, and the efficiency can be improved effectively. It means that the proposed scheme can also achieve the current-stress optimized control based on DPS control. Meanwhile, the efficiency of DAB dc-dc converters under MPC-CSO scheme is slightly higher than traditional CSO scheme even though the same phase-shift control is adopted. It is because the unbalanced power transmission will make the current stress of part of the cells larger, which will reduce the efficiency of the entire system.



(a) The current stress

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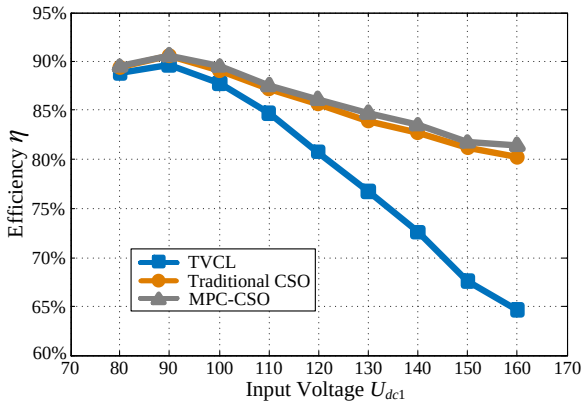


(b) The efficiency

Fig.10 The experimental waveforms of current stress and efficiency with respect to the input voltage under TVCL control, traditional CSO control and MPC-CSO control schemes.

B. Experimental Comparison of Transmission Power Balance

When the experimental parameters are set as U_{dc1}=U_{dc2}=U_{dc3}=90V, U_o^*=80V and R=20Ω, Fig.11 shows the output current waveforms of each DAB cell in the process from TVCL scheme to MPC-CSO scheme. It can be seen that the transmission power of each DAB cell is not balance under TVCL scheme, and the output current of DAB cell 1 is larger than other two DAB cells due to the smaller storage inductor. When the MPC-CSO scheme is implemented, the transmission power balance can be realized instantly without the output voltage fluctuation.

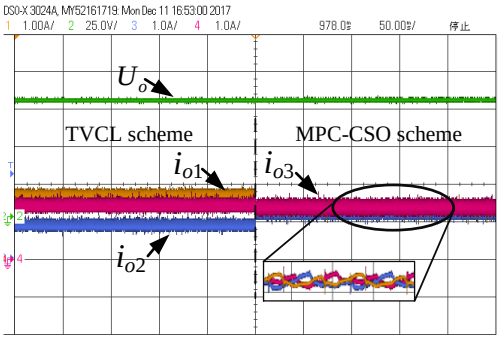
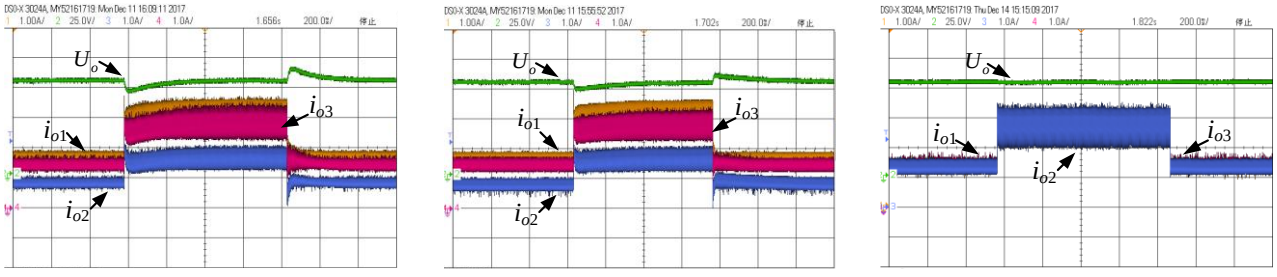


Fig.11 The output current waveforms of each DAB cell in the process from TVCL scheme to MPC-CSO scheme. (i_{o1}: 1A/div; U_o:25V/div; i_{o2}: 1A/div; i_{o3}: 1A/div; time:50ms/div)

When the experimental parameters are set as U_{dc1}=U_{dc2}=U_{dc3}=90V and U_o^*=80V, Fig. 12 shows the transient experimental results of the output current of each DAB cells under three control schemes when the load steps down from 20Ω to 10Ω. It can be known that the transmission power of each DAB cell can always be balanced under MPC-CSO scheme even though the transmission power of DAB cells steps change, and the output voltage of DAB cells keeps almost constant.



(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.12 The transient experimental results of output current of each DAB cells under three control schemes when the load

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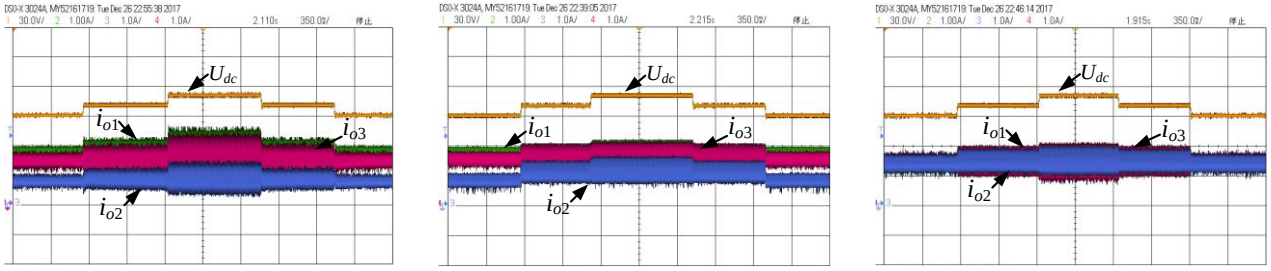
steps down from 20Ω to 10Ω. (i_{o1}: 1A/div; U_o:25V/div; i_{o2}: 1A/div; i_{o3}: 1A/div; time:200ms/div)

When the experimental parameters are set as U_o^*=80V and R=20Ω, Fig. 13 shows the transient experimental results of the output current of each DAB cells under three control schemes when the input voltage steps up from 90V to 100V and then to 110V successively, and then steps down back to 90V successively. It can be seen that when the input voltage is 90V (voltage transfer ratio k is close to one), the unbalanced degree of transmission power under TVCL and traditional CSO schemes is similar. And when the input voltage is 110V, the unbalanced degree of transmission power under TVCL scheme is more terrible than traditional CSO scheme, which is consistent with the theoretical analysis. However, transmission power balance can always be achieved under the proposed MPC-CSO scheme no matter how the input voltage steps up or down.



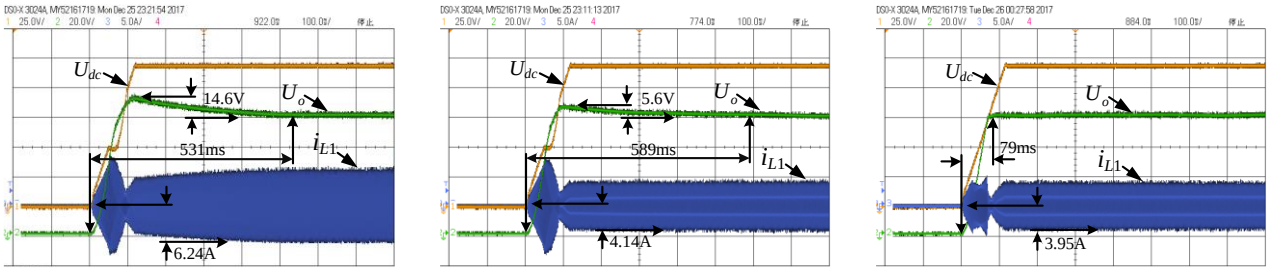
(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.13 The transient experimental results of output current of each DAB cells under three control schemes when the input voltage steps change. (U_{dc}:30V/div; i_{o1}: 1A/div; i_{o2}: 1A/div; i_{o3}: 1A/div; time:350ms/div)

C. Experimental Comparison of Dynamic Response

In order to test the excellent dynamic performance of the proposed MPC-CSO scheme under DPS control. A comprehensive experimental comparison of MPC-CSO scheme, traditional CSO scheme and TVCL scheme is carried out.

When the experimental parameters are set as U_{dc1}=U_{dc2}=U_{dc3}=120V, U_o^*=80V and R=30Ω, Fig. 14 shows the transient experimental results of three control schemes during start-up process. It is clear that TVCL scheme takes a long settling time (over 500ms) with overshoot about 14.6V. And the output voltage overshoot can be reduced effectively under the traditional CSO scheme, but the settling time is still very long, about 589ms. However, the output voltage can reach the desired value directly without overshoot using the shortest start-up time (about 79ms) under the proposed MPC-CSO scheme. Meanwhile, compared with TVCL and traditional CSO schemes, the current-stress of the DAB converter under MPC-CSO scheme is smallest, about 3.95 A.



(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.14 The transient experimental results of three control schemes during start-up process. (U_{in}: 25V/div; U_o:20V/div; i_L:5A/div; time:100ms/div)

When the experimental parameters are set as U_{dc1}=U_{dc2}=U_{dc3}=100V, U_o^*=80V, the transient experimental results of three control schemes under load step-change are shown in Fig. 15 and Fig. 16, where the load steps down from 30Ω to 10Ω in Fig. 15, and steps up from 10Ω to 30Ω in Fig. 16. It can be seen that the transient response under TVCL scheme [Fig. 15(a) and Fig. 16(a)] is very slow (over400ms) in both the load step-up or step-down conditions. Furthermore, in the traditional CSO scheme [Fig. 15(b) and Fig. 16(b)], the fluctuation of output voltage can be reduced obviously and the settling time is still very

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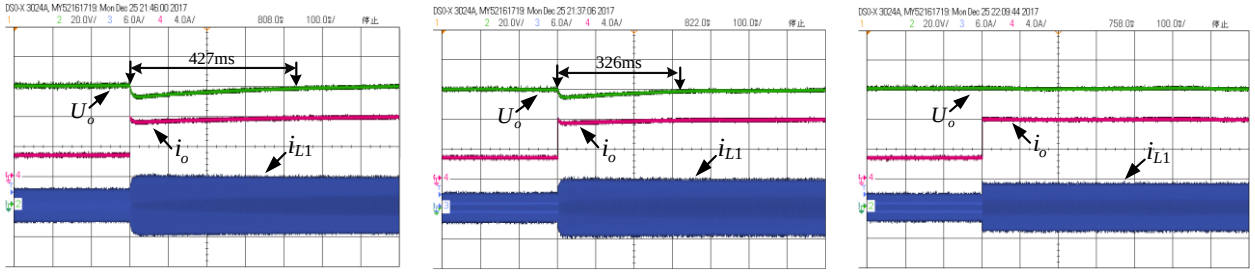
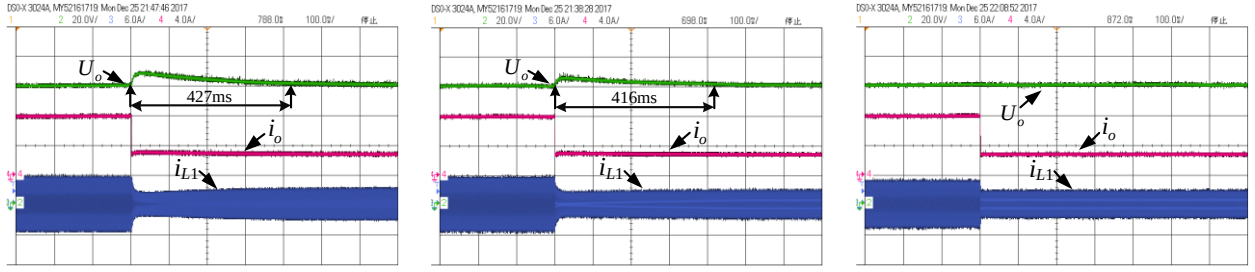
long, over 300ms. Nevertheless, the output voltage keeps almost constant in MPC-CSO scheme [Fig. 15(c) and Fig. 16(c)] no matter the load steps up or down. Thus, the proposed MPC-CSO scheme can achieve fastest dynamic response when the load steps up or down. Besides, it can be seen that the current stress of MPC-CSO is also the smallest.



(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

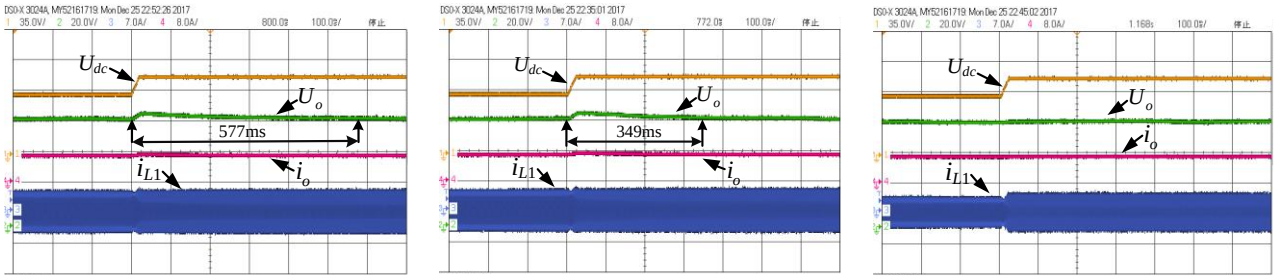
Fig.15 The transient experimental results when the load steps down from 30Ω to 10Ω. (U_o:20V/div; i_o:6A/div; i_L:4A/div; time:100ms/div).



(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.16 The transient experimental results when the load steps up from 10Ω to 30Ω. (U_o:20V/div; i_o:6A/div; i_L:4A/div; time:100ms/div).

When the experimental parameters are set as U_o^*=70V, R=10Ω, Fig. 17 and Fig. 18 show the transient experimental results of DAB dc-dc converter with input voltage step-change, where the input voltage U_{dc1}, U_{dc2} and U_{dc3} step up from 70V to 90V in Fig. 17, and step down from 90V to 70V in Fig. 18. It is clear that the output voltage under TVCL scheme [Fig. 17(a) and Fig. 18(a)] takes a long settling time about 400ms and the fluctuation of output voltage is very obvious. For the traditional CSO scheme [Fig. 17(b) and Fig. 18(b)], the settling time of output voltage can be reduced, but the fluctuation of output voltage can not be suppressed effectively. And it is obvious that the output voltage is almost unchanged in both the input voltage step-up or step-down processes in MPC-CSO scheme [Fig. 17(c) and Fig. 18(c)]. Thus, the proposed MPC-CSO scheme can achieve the excellent dynamic performance when the input voltage steps down or up.



(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.17 The transient experimental results when the input voltage steps up from 100V to 120V. (U_{in}:35V/div; U_o:20V/div; i_o:8A/div; i_L:7A/div; time:100ms/div).

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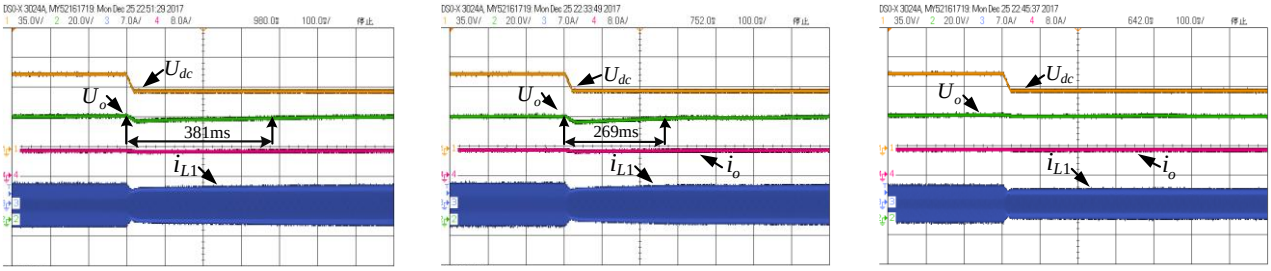
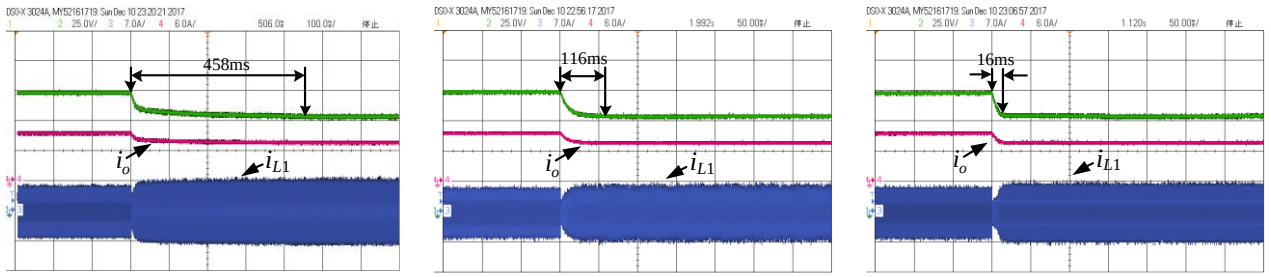


(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.18 The transient experimental results when the input voltage steps up from 120V to 100V. (U_{in}:35V/div; U_o:20V/div; i_o:8A/div; i_L:7A/div; time:100ms/div).

When experimental parameters are set as U_{dc1}=U_{dc2}=U_{dc3}=120V, R=10Ω, Fig. 19 shows experimental results of the DAB dc-dc converter when the desired voltage steps down from 100V to 80V. It is clear that dynamic response of the output voltage under TVCL scheme is slowest, with a very long settling time about 458ms. In traditional CSO scheme, the settling time is shortened significantly, close to 116ms. Contrastively, the MPC-CSO scheme can achieve fastest dynamic response, only 16ms. Thus, the proposed MPC-CSO scheme can realize the most excellent dynamic performance when the desired voltage steps up or down.



(a) TVCL scheme **(b) traditional CSO scheme** **(c) MPC-CSO scheme**

Fig.19 The transient experimental results when the desired voltage steps down from 100V to 80V. (U_o:25V/div; i_o:6A/div; i_L:7A/div; time:50ms/div).

Based on Fig. 14~Fig. 19, a comprehensive experimental comparison of TVCL scheme, traditional CSO scheme and MPC-CSO scheme can be summarized in Table II. It is obvious that the proposed MPC-CSO scheme can achieve the best dynamic performance among the three schemes.

TABLE II

AN EXPERIMENTAL PERFORMANCE COMPARISON OF THREE CONTROL SCHEMES

Control Schemes	Start-up	Load disturbance	Input voltage disturbance	The desired voltage step-change
TVCL	slow	slow	slow	slow
Traditional CSO	slow	slow	fast	fast
MPC-CSO	fast	fast (0ms)	fastest (0ms)	fastest

In fact, the proposed MPC-CSO scheme can also be extended to other phase-shift control such as EPS or TPS control. However, for the parallel DAB modules in PETT, the control scheme should be as simple as possible besides the comprehensive performance improvement. Thus, the MPC-CSO scheme in DPS control is the most suitable for cascaded DAB modules in PETT.

VII CONCLUSION

Aimed at the parallel DAB modules in PETT, a model predictive control with current-stress-optimized (MPC-CSO)

scheme based on dual-phase-shift (DPS) control is proposed to improve the dynamic performance and balance the transmission power. By combining the predictive control and CSO scheme, the dynamic response and the efficiency of DAB converters with transmission power self-balance can be improved at the same time when it faces with the following extreme conditions such as: start-up, load resistor step-change, input voltage step-change and the desired voltage step-change.

A comprehensive experimental comparison of TVCL, traditional CSO and the proposed MPC-CSO schemes is adopted to show the salient features of the proposed MPC-CSO scheme, which can be concluded as:

1) It can always achieve transmission power balancing in various operation conditions even if the power of DAB cells steps up or down.

2) It can boost the output voltage to the desired value directly with no overshoot during start-up process.

3) It can achieve excellent dynamic response of DAB dc-dc converters under the input voltage fluctuation or load disturbance conditions, and the settling time is approximately to zero.

4) It can further improve the efficiency of DAB converters even though the same phase-shift control is adopted, especially for high voltage transfer ratio or light-load operation condition.

5) It can be extended to other phase-shift controls if the computation speed of the adopted digital controller is allowed.

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