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DPWM techniques in digitally controlled, EMI compliant DC-DC converters

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Abstract

This paper aims to present a combined, DPWM based control method and spectrum flattening technique of a mid-power range DC-DC converter. The research goal was to obtain sustainable results in both switching control and EMI compliance, using one 8 or 16 bits RISC MCU as main control unit running a performance- and speed-optimized firmware. This approach describes a hybrid method preserving the good dynamic performances of an analog switching regulator controller and adding the flexibility of controlling the output voltage by adjusting the duty cycle value of a DPWM signal and thus controlling the average voltage value of the signal applied in the feedback circuit of a DC-DC converter. Beside the feedback control of the DC-DC converter an active EMI reduction technique applies on this design by taking advantage on the constant-frequency, forced-continuous current mode architecture of the switching regulator controller, which allows its frequency to be synchronized with an external control clock dithered by a software implemented pseudo-random sequence generator. All this efforts concludes in reducing the noise power considerably at the main peak and at the next peaks.

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Keywords: DPWM; EMI; PSRG; SFM; SMPS.

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1. Introduction

Applying digital control techniques to switching mode power supplies (SMPS) adds several advantages such as flexibility, precision, scalability with the use of software control. However, pure digital control has also disadvantages such as bandwidth, switching frequency, cost, etc. [1]. Our approach is to describe a hybrid method by using the good dynamic performances of an analog switching regulator controller (SRC) and adding the flexibility of controlling the output voltage with a microcontroller unit (MCU) and taking special care on flattening the electro-magnetic interference (EMI) of the converter by a software controlled, active method. One of the advantages of this hybrid method is the possibility of adding an external control loop with a narrower loop bandwidth in order to counteract temperature effect, offset and aging of a pure analog power supply. The external loop bandwidth depends on typical digital control parameters such as instruction cycle speed of the MCU, analog-to-digital conversion time, filtering. In the digital pulse width modulation (DPWM) method, this loop delay is considerably less, since it is dependent only by the instruction cycle speed of the MCU (duty value changed) and the delay introduced by the output filter dampening the AC component of the DPWM signal. The amplified PWM signals drive the gates of the main switches in the converter, which generates electromagnetic interferences, perturbing other electronic equipment. Beside passive EMI countermeasures (layout design, filtering), a good practice to mitigate the emission power level is to introduce a pseudo-random dithering of control clock timing of the SRC, which can be achieved by software and one available PWM peripheral of the same control MCU. Many papers discuss the EMI level mitigation; this work references a few of them [4], [5], [6].

The main experimental application (Figure 1) consists of a digitally controlled DC-DC converter based on a low power, high-performance USB capable, RISC MCU and on a high efficiency, synchronous, buck-boost controller with external reference, driving four external MOSFET switches. The MCU generates two independent PWM signals: PWM1 is used for controlling the SRC and PWM2 is used for synchronizing the switching logic inside the SRC.

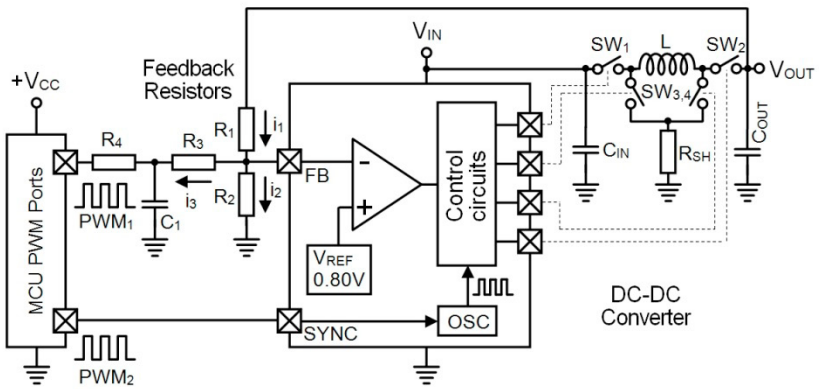


Fig. 1. Block schematic of the digitally controlled power supply unit pointing the key components of the system.

2. DPWM control method of a DC-DC converter

The component values and the ripple introduced in the feedback loop were determined by simulations. DPWM outputs are dependent on several parameters at a given moment in time:

$$V_{PWM} = f(\mathrm{V}_L, \mathrm{V}_H, \mathrm{f}_{PWM}, \mathrm{D}, \mathrm{t}) \tag{1}$$

where VL represents the minimum DC voltage generated by the DPWM output (Low logic level), VH is the maximum DC voltage generated by the DPWM output (High logic level), f_{PWM} is the frequency of the DPWM signal, D is the duty cycle of the DPWM signal and finally, t is the considered moment of time. The output voltage can be expressed with the formula:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + \left(V_{REF} - V_{PWM}\right) \cdot \frac{R_1}{R_3 + R_4} \tag{2}$$

where V_{REF} is a reference voltage and V_{PWM} is:

$$V_{PWM} = D \cdot V_H + (1 - D) \cdot V_L \tag{3}$$

The optimal resistor values and the PWM frequency are determined after performing the necessary calculations, demonstrated in [10], considering the use of standard resistor values, more suitable for practical implementation, the obtained values are as follows: R_1=30 kOhm, R_2=1.2 kOhm, R_3=3.6 kOhm, R_4=1.2 kOhm, $f_{PWM=}$46.875 kHz.

The ripple introduced in the feedback loop is filtered out with a simple low pass filter and its value is highest at 50% duty cycle value of the DPWM signal. We can express the capacitor charge and discharge equations during steady state conditions at *T/2*, where *T* is the PWM period, V_{p+} and V_{p-} are the maximum and minimum peak value of the ripple voltage as:

$$V_c = V_{p-} + (\mathrm{V_H} - \mathrm{V_L}) \cdot \left(1 - e^{-\frac{T}{2R_4C_1}}\right) \tag{4}$$

$$V_d = V_{p+} + \left(V_{p+} - V_{p-}\right) \cdot e^{-\frac{T}{2R_4C_1}} \tag{5}$$

The ripple voltage can be expressed as:

$$V_{ripple} = V_{p+} - V_{p-} \tag{6}$$

The capacitor charge and discharge voltages are equal at *T*/2 moment. Using (Eq.4), (Eq.5) and (Eq.6) and after rearranging the equation we can obtain the ripple voltage's equation:

$$V_{ripple} = \left(V_H - V_L\right) \cdot \frac{1 - e^{-\frac{T}{2R_4C_1}}}{1 + e^{-\frac{T}{2R_4C_1}}} \tag{7}$$

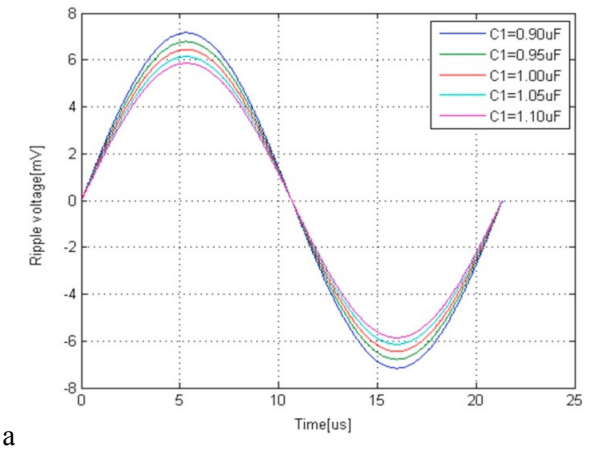
We optimize our system so that the ripple value is always lower or equal than 1LSB value of the realized DAC converter dependent on the desired resolution, thus we define the ripple voltage as:

$$V_{ripple} = \frac{\left(V_H - V_L\right)}{2^N} \tag{8}$$

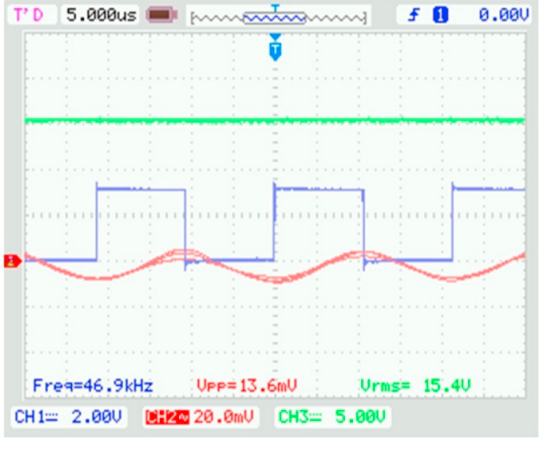
Using (Eq.7) and (Eq.8)and by rearranging we can obtain the time constant defined as:

$$R_4 \cdot C_1 = \frac{1}{2f\left[\ln\left(2^N+1\right)-\ln\left(2^N-1\right)\right]} \tag{9}$$

By choosing 8 bit DAC resolution, the value of C_1 results immediately by rearranging (Eq.9), which ensures that the ripple value does not exceeds 1LSB value of DAC converter. The simulation results (Figure 2a) of the experimental circuit (Figure 1) shows the effect of capacitor C_1 on the ripple value, the experimental measurements are presented in Figure 2b.



a



b

Fig. 2. (a) The ripple voltage on C1 depending its value (b) The measured ripple with 50% duty of DPWM.

3. Active EMI dampening of the DC-DC converter

Taking advantage of this particular design, where the buck-boost controllers have reference signal inputs, PWM signals can be applied to these inputs synchronizing the control of the switching elements (MOSFETs). Additionally this method allows an efficient EMI reduction technique by randomly spreading the frequency of the PWM signals, thus flattening the radiated switching noise amplitude on the specified switching frequency and upper harmonics.

For a generic, quad-pipelined, 8-bit RISC MCU the PWM period time can be determined as a relation between the values stored in a reference register (PR) and t_{OSC}, the period time of the MCU's main clock signal, multiplied by an optional prescale value. The particular formulas are listed in the referenced microcontroller manuals [2], [8], [9]. For a fixed main clock frequency (f_{OSC}) the PWM resolution decreases as the PWM frequency increases accordingly to the (Eq. 10). This relation determines the main criteria in microcontroller selection where the highest peripheral clock rates (driving the PWM generator) are preferred:

$$\mathrm{PWM_{RES}} = \log(f_{OSC} \bullet (f_{PWM})^{-1}) \bullet (\log(2))^{-1} \tag{10}$$

Having direct control over the PWM frequency, allows modulating the period register (SFR) content by randomly generated values. Depending on implementation the pseudo random generator algorithm could have only algorithmic implementation or supported by MCU hardware. Some MCU families [7] features random number generation by hardware, combining different on-board oscillator clock signals exploiting that the two clocks can vary independently from each other counting an unpredictable difference of pulses number [10]. Thus, the random generator call can return values very fast.

A category of particular pseudo-random sequence generators (PRSG) [11] uses simple and modular irreducible polynomials where the pointed member values are XOR-ed in adjacent sequences and then the result shifts back to LSB position of the initial value [3], generating a sequence of 16 bits that repeats every 65535 shifts [12],[13]. Pseudo-random dithering of control clock timing in DC-DC converter [5] is achieved by adding extra digital circuitry.

To improve algorithmic randomness in a simple manner implies an open-air analog-to-digital converter (ADC) input digitalization by periodically adding two or three LSB bit to the input value of the PRS. The noise captured by the ADC input is random by nature, thus mixing these randomly changing LSB bits with the input value of PRSG before the generator distribution cycle ends, could improve the overall randomness of the PRSG. Figure 6 sketches the entire workflow of the software and hardware mechanism, highlighting the relations between each software and hardware component.

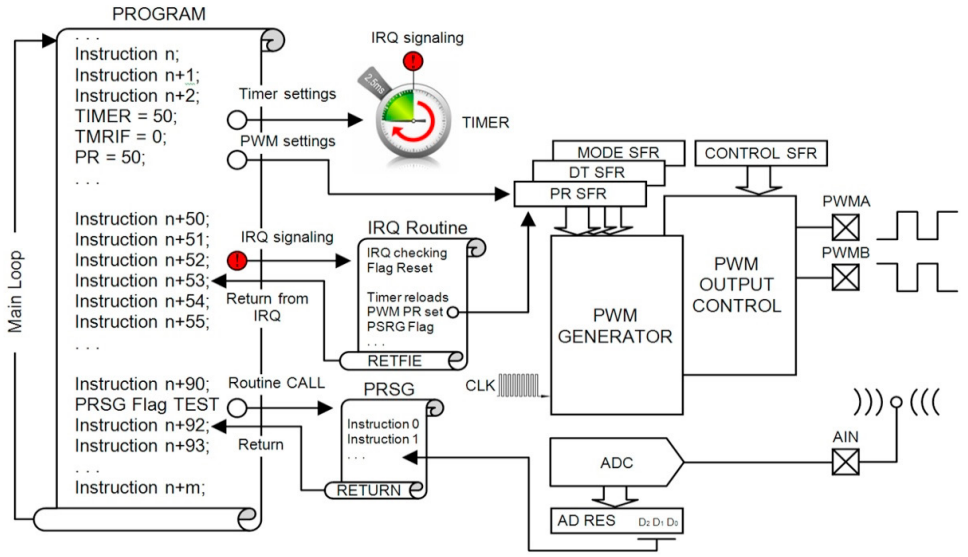


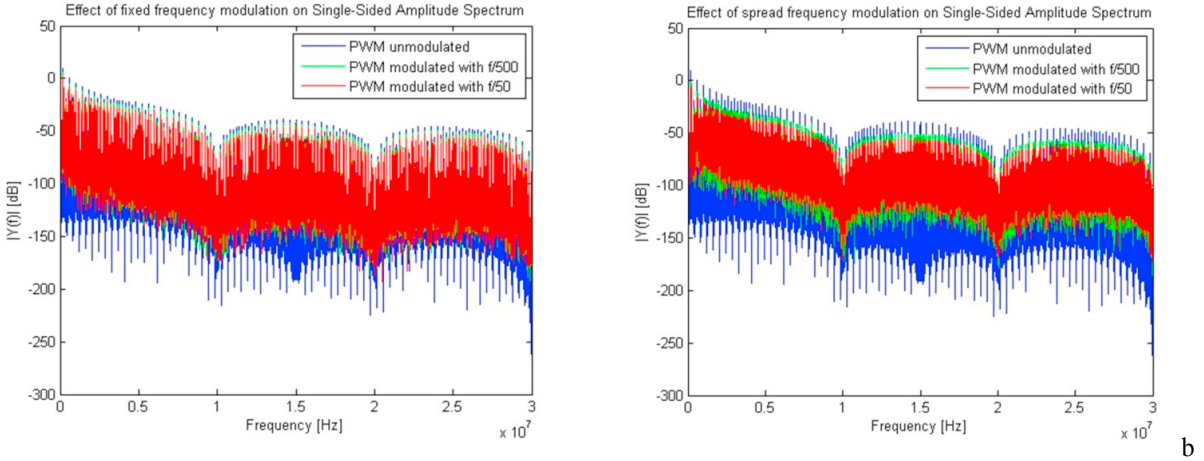
Fig. 3. Workflow of the DPWM control loop and pseudo randomly spread frequency generator.

A TIMER is responsible for the modulation frequency, the IRQ routine handles the TIMER overflow, reloads the TIMER and sets the PWM's period register content and finally enables the next random sequence generation. In the main loop, the PRSG Flag is periodically tested and when is active, a new random sequence runs out from the subroutine serving the next IRQ routine. The ADC module contributes to add more randomization to the PRSG value.

The application also needs a time-base for the modulation frequency of the PWM signal. Thus, a timer circuit periodically triggers the PSRG and sets the PWM frequency accordingly. The control algorithm slides the frequency gradually in every modulation period until it reaches the desired value then takes a new random value and the cycle repeats.

In accordance with the presented and referenced theory, a PWM signal generator was built in MATLAB environment that can produce a train of PWM signals with customizable amplitude, switching frequency, sampling frequency, on time, rise and fall time, duty and number of periods in the pulse train presented in [14]. The single sided amplitude spectrum simulation uses 300 samples per switching period, and a train of 2000 PWM periods represented on a 10 ms timeslice Figure 4a presents the effect of modulating the main 200 kHz switching frequency by a fixed amount either in positive or negative direction with an *f*/500 modulation frequency and a +/- 15% offset of the main frequency. One can observe that as the modulation frequency increases the frequency components magnitude are reduced.

The other single sided amplitude spectrum simulation (Figure 4b) presents the effect of spread frequency modulation using random frequency generation with different modulating frequencies scaled to the nominal 200 kHz frequency.



a b

Fig. 4. (a) Fixed frequency modulation (b) Randomly spread frequency modulation.

4. Results and Discussion

The first experimental results obtained with a spectrum analyzer and a H-field EMC probe placed over the inductor coil shows the spectral image of the switching noise at 300 kHz switching frequency without applying the spreading algorithm (Figure 5a). The next diagram shows the spectral image with spread-frequency modulation enabled by software (Figure 5b). PWM signals now suffer 20% spread of the PWM frequency and the resulted spectrum slides in positive direction. The magnitude of the frequency components decreases by spreading the signals energy over a wide frequency band. Choosing low resolution bandwidth (RBW) frequency increases the scanning resolution and reveals an attenuation of the integrated power of the signal components spreaded on randomly distributed frequency bands.

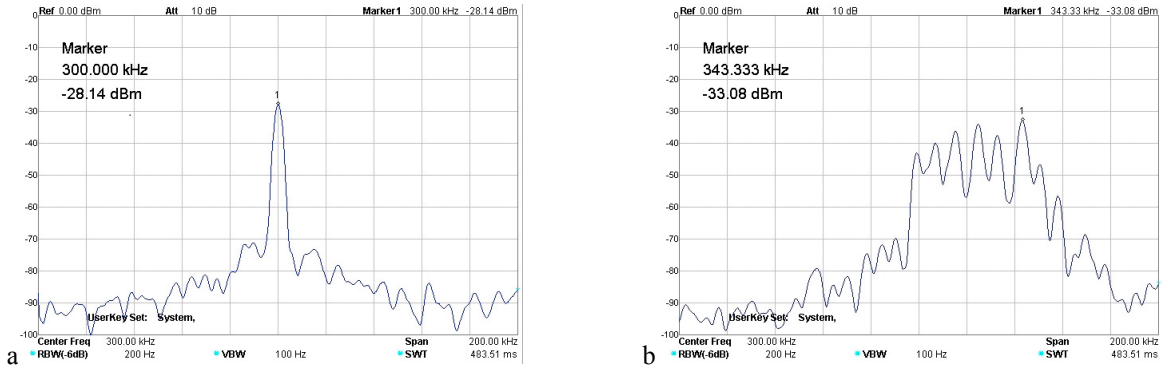


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Fig. 5. (a) Switching noise without spread modulation (b) Switching noise with spread modulation.

The next experimental step consists in a conformity verification of the conducted EMI limit of the DC-DC converter according to the CISPR22 standard, Class A. The DC-DC converter input voltage was set at 12 VDC, powered from a laboratory grade power supply unit, through a line attenuation network (LISN). During the test an electronic load consumes 1A at a fixed 12 VDC output voltage.

Figure 5a shows that without enabling the spreading, the switching noise has a strong presence at the main frequency component (66.21 dBµV at 300 kHz) and at the first couple of harmonics (64.30 dBµV at 600kHz, 56.05 dBµV at 900kHz), overriding the 60 dBµV average limit (horizontal green line).

Enabling the spreading algorithm, the magnitude of the frequency components are reduced, as can be shown on Figure 5b. Randomly changing the switching frequency over a +20% domain of the base frequency in every 1ms will reduce the noise power by 7.79dBµV at the main peak, by 6.2dBµV and 11.08dBµV at the second, respectively at the third peak.

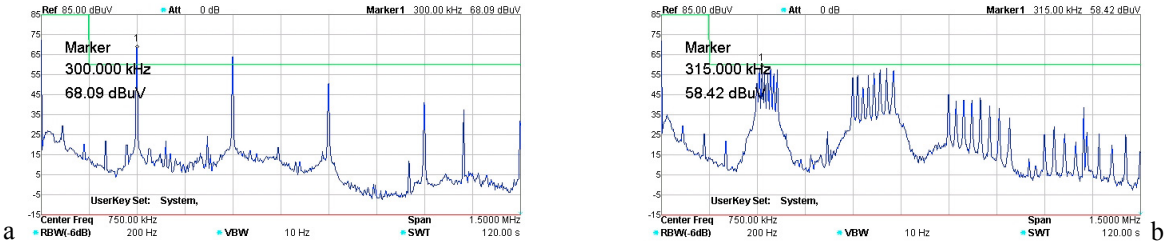

Fig. 6. (a) Switching noise without spread modulation (b) Switching noise with spread modulation.

Thus, the maximum peaks are set below the 60dBµV limit. For better understanding the below inserted diagrams show only a magnified portion from 0 Hz to 1.5MHz of the entire emission bandwidth set by the CISPR standard. A practical comparison was also performed (Table 1.) targeting three mainstream microcontroller family (Atmel XMEGA, Texas MSP430 and Microchip PIC18F) with special interest on the low-mid range, budgetary priced, RISC architecture MCUs, equipped with at least 16K program memory, multi-channel PWM generator and built-in USB communication interface. The key variables were the main clock source frequency (f_{OSC}), peripheral clock frequency (f_{PER}), execution cycle (t_{CYC}). These variables have direct influence on the PWM period resolution (PR) and the modulation period (in relation with the execution time of the PRSG function). Some MCU families use the CPU instruction cycle clocking all their peripherals while others allow routing the main oscillator output towards the peripheral clock inputs thus improving the PWM frequency resolution.

Table 1. Performance comparison between MCU families.

MCU Family	MCU Subtype	Clock Frequency	Max. Peripheral Clock Freq.	Execution Cycle Time	PRSG execution time (rand())	PWM Period Resolution	Modulation period	Value / performance
Atmel XMEGA	ATxmega16C4	32MHz	32MHz	31.25ns	370us (140us)	8-6bits		best
Texas MSP430	MSP430F5503	25MHz	25MHz	avg. 160ns	620us (8.2us)	7-6bits	1-100ms	better
Microchip PIC18F	PIC18F24K50	48MHz	12MHz	83.33ns	810us (107us)	6-5bits		good

5. Conclusions

A series of experimental measurements validates the previously presented mathematical models, resulting from computer-aided simulations offering practical advises about the linearity, resolution and code efficiency for real applications. Regarding the EMI mitigation technique there are many applications and articles addressing the same problem but few with immediate applicability in a mid-range MCU domain. This work intends to add some applicative details in that less covered domain. Practical measurements also prove that the DC-DC converter efficiency is not affected considerably, but the EMI reduction increases by this technique.

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