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An all-digital low ripples capacitive DC-DC converter with load tracking controller

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ABSTRACT

An all-digital Switched Capacitor (SC) DC-DC converter with a Switch Logic Controller and Optimizer (SLCO) is proposed in this paper. The SLCO achieves the maximum efficiency while keeping the output voltage ripples and load regulation at minimum values. Capacitance Modulation (CpM) and Pulse Frequency Modulation (PFM) are used to cover a wide dynamic range of load currents. Theoretical analysis and optimization algorithm are also presented to achieve the maximum efficiency. The SC converter is implemented in 0.13 μm CMOS technology using thick oxide I/O devices and achieves a maximum efficiency of 63% at power density of 0.095 W/mm^2. The SC converter delivers up to 100 mA load current for an output voltage of 1 V from a 3.6 V nominal input voltage. Output voltage ripples and load regulation are less than 16 mV and 0.02%/mA, respectively.

1. Introduction

Switched Capacitor (SC) DC-DC converters have received high attention over switching based DC-DC converters [1–3]. This is because SC converters use the integrated high-density capacitors with low series resistance in standard CMOS process providing high power efficiency, cost effective, and thus, being a fully integrated solution. However, there are technical challenges in the design of fully integrated SC converters. One of the most important challenges is to support a load current (I_{load}) with wide dynamic range (e.g. load currents up to 100 mA) while keeping the output voltage ripples ($V_{ripples}$) lower than 20 mV pp [4,5].

Many techniques have been introduced to lower the level of $V_{ripples}$ such as phase interleaving, Capacitance Modulation (CpM), and time modulation [4,6]. In Ref. [6], a VCO combined with a phase interleaving technique was used to lower the values of the load regulation and $V_{ripples}$ through changing the switching frequency (f_{sw}). This approach showed $V_{ripples}$ close to 50 mV pp for load currents up to 160 mA using 18-phase interleaving. The main limitation of this approach is the need for a VCO with wide frequency range to support a wide dynamic range of I_{load}. As an example to cover a load range from 0 to 160 mA, Le et al. showed that the VCO frequency has to change from 1 to 300 MHz [6]. Moreover, this approach is a mixed signal solution which is not an all-digital scalable solution.

In Ref. [4], the load regulation has been reduced through Pulse Frequency Modulation (PFM). In addition, capacitance and time modulation techniques have been used to further reduce $V_{ripples}$. This approach results in $V_{ripples}$ that scales with I_{load}, and thus, this approach reduces $V_{ripples}$ at light loads only. As an example, Kudva et al. shows $V_{ripples}$ of 27 mV pp for load current of 2 mA using a load capacitor of 5 nF [4].

Achieving $V_{ripples}$ lower than 20 mV for load currents up to 100 mA with integrated capacitors in an all-digital solution is still a challenging problem. Combining two or more of the already existing ripple reduction techniques may result in further reduction of $V_{ripples}$ for a load with wide dynamic range. Such an approach requires an optimum controller to achieve the targeted reduction. This controller should guarantee that controls of the power switches are leading to the maximum efficiency and smaller load regulation values while reducing $V_{ripples}$.

Moreover, most of mobile devices are powered by batteries with nominal supply voltage of 3.6 V while digital circuits need a supply of ~1 V. Such a high voltage difference between input and output voltage would stress the transistors of any advanced technology node, e.g. 0.13 μm and less. One possible solution is to use cascaded thin-oxide transistors and use level-shifters to avoid the breakdown\stress of the devices [6].

The work in Ref. [2] used an all-digital approach but with only a single 2:1 step-down topology. As a result, the efficiency is limited to

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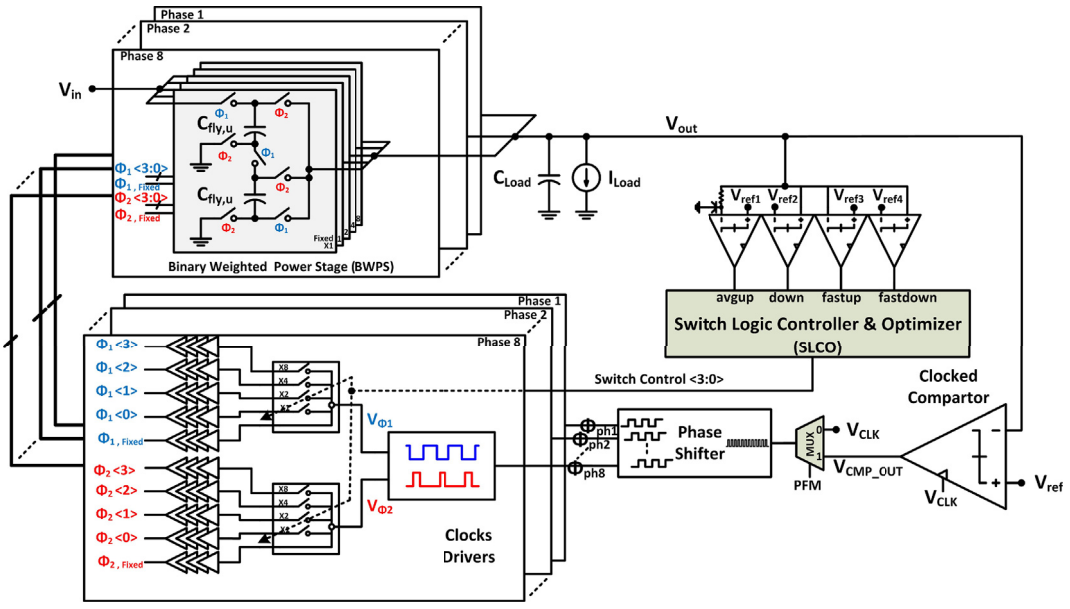

Fig. 1. System-level block diagram of the proposed SC converter.

(<55%) for a ~1 V output voltage.

Therefore, achieving high efficiency while having a high power density in an all-digital solution is still another challenging problem that is being addressed in this work.

Load step transient recovery time is also another challenging problem for switched capacitor converters [5]. Le et al. achieved a sub-nano second recovery time on the cost of having a clock frequency of 3.3 GHz [6]. Such high frequency oscillator reduces the overall efficiency. Therefore, reducing the recovery time without affecting the efficiency is also a problem that is being addressed in this paper.

This paper proposes a new fully integrated SC converter for load currents up to 100 mA. The proposed architecture is based on combining CpM [7], PFM [2], and phase interleaving techniques with an optimum controller to reduce $V_{ripples}$ while keeping lower values of load regulation over a wide load current range. In addition, a Fast Transient Recovery (FTR) technique to lower the recovery time is introduced.

The paper is organized as follows. In Section 2, the proposed architecture is introduced. Section 3 discussed the implementation of the controller. The circuit implementation of the proposed SC converter is shown in Section 4. Section 5 presents the simulation results. Finally, Section 6 concludes the paper.

2. Proposed architecture

Qualitative Description: A top-level block diagram of the proposed SC converter is shown in Fig. 1. The proposed architecture is based on a hybrid solution of CpM and PFM techniques to support a wide range of load currents.

The proposed architecture is mainly composed of the following main blocks: a phase interleaved Binary-Weighted Power Stage (BWPS), a Switch Logic Controller and Optimizer (SLCO), a clocked comparator, and a multi-phase clock driver. In this design, eight phases are used for each binary weighted power stage. A multiplexer (MUX) is used to switch between the CpM and PFM modes. The operation of the feedback loop starts with comparing the output voltage (V_{out}) with set of reference voltages $V_{ref(1-4)}$ through four clocked comparators. Outputs of clocked comparators are detected by the SLCO which determines the mode of operation (CpM or PFM mode) and the optimum Switch Control <3:0> word.

At light loads condition (PFM mode), the MUX bypasses the external clock and an internal clock ($V_{CMP,OUT}$) at the output of the clocked comparator is generated to control the BWPS. In this case, the SLCO selects the minimum number of power stages to minimize $V_{ripples}$ such that V_{out} equals the desired value. It is important to note that the number of power stages changes as I_{load} changes and the SLCO is responsible for finding this value as explained later throughout the paper. In addition, as I_{load} scales down, the number of phases controlling the power stages is reduced to further reduce $V_{ripples}$.

At heavy load conditions (CpM mode), the MUX bypasses the clocked comparator and a clock with fixed frequency is used to control the power stages. In this case, $V_{ripples}$ depends on the value of the switching frequency (f_{sw}), number of interleaving phases, and load capacitance (C_{load}). While the load regulation of V_{out} depends on flying capacitors (C_{fly}), f_{sw} and switches sizes. Several design parameters can lead to the desired level of the load regulation and $V_{ripples}$, however one specific set of the design parameters leads to the highest efficiency. The SLCO selects the optimum number of stages to increase the efficiency while reducing the load regulation and $V_{ripples}$ to the desired levels. Finally, at fast load transient steps, the fastup or the fastdown signals, shown in Fig. 1, are triggered forcing the SLCO to bypass the switch control word for fast step up\step down load current. This approach enables the converter to recover quickly and prevents large undershooting\overshooting.

Quantitative Analysis: The theory and the optimum design methodology for the proposed SC converter are presented in this subsection. This optimum methodology maximizes the efficiency for given values of load regulation and $V_{ripples}$.

The efficiency, η, of the SC converter, modeled in Fig. 2, is given by,

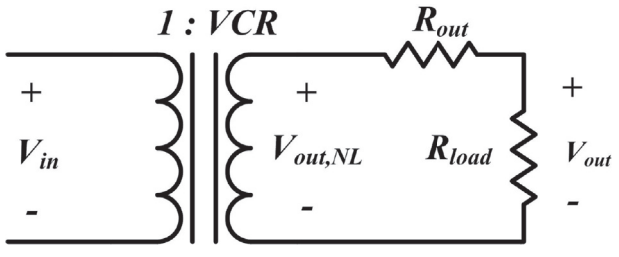

Fig. 2. SC converter model.

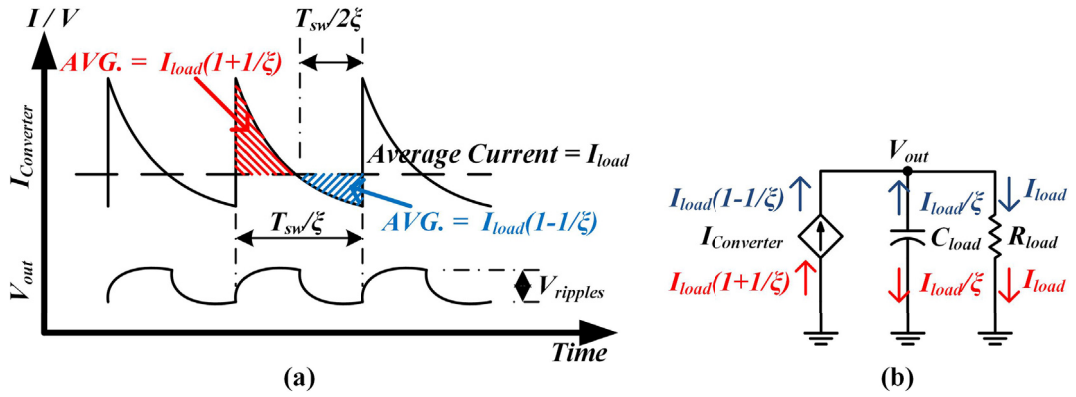

Fig. 3. (a) Output Current and voltage pulses of the converter when using interleaving. (b) Equivalent circuit of the converter showing the current pulses.

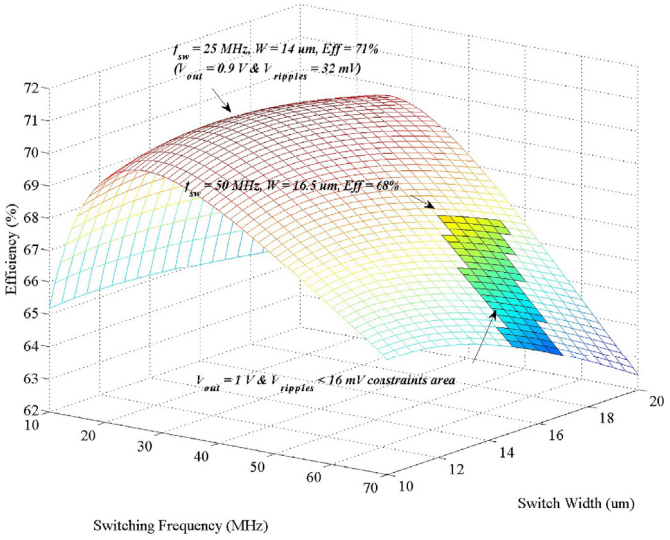

Fig. 4. Efficiency versus switching frequency and switch size. Solid area represents V_{out} = 1 V and $V_{ripples}$ < 16 mV.

$$\eta = \frac{P_{load}}{P_{load} + P_{loss}} = \frac{P_{load}}{P_{load} + P_{R_{out}} + P_{sw} + P_{control}} \tag{1}$$

where P_{load} is the output load power, P_{Rout} is the intrinsic loss due to the output impedance of the SC converter (R_{out}), P_{sw} is the gate switching losses of CMOS switches, $P_{control}$ is the loss of the control circuits. Analytical expressions for those parameters are given by Ref. [2],

$$P_{load} = I_{load} \times \gamma \times V_{out,NL} \tag{2}$$

$$P_{R_{out}} = \frac{(V_{out,NL} - \gamma \times V_{out,NL})^2}{R_{out}} \tag{3}$$

$$R_{out} = \sqrt{\left(\frac{K_C}{N \times C_{fly,u} \times f_{sw}}\right)^2 + \left(\frac{2 \times K_S}{N \times \xi \times \mu \times C_{ox} \times \frac{W}{L} \times V_{dsat}}\right)^2} \tag{4}$$

$$P_{sw} = V_{in}^2 \times C_{sw} \times f_{sw} \tag{5}$$

where I_{load} is the load current, γ is the ratio between loaded and unloaded output voltage, V_{out} and $V_{out,NL}$, respectively. K_C and K_S are constants that depend on the converter topology, $C_{fly,u}$ is the unit flying capacitance (= C_{fly}/N), N is the switch control word, and ξ is the number of phases used for interleaving. μ is the mobility, C_{ox} is the oxide capacitance, W/L is the aspect ratio, V_{dsat} is the saturation voltage of MOS device, V_{in} is the input voltage to the converter, C_{sw} is the total gate and parasitic switching capacitance ($C_{sw} \propto W$), and f_{sw} is the switching frequency.

The output impedance (R_{out}) given in equation (4) composes of two terms. The first term represents the slow switching resistance which represents the capacitive nature of the SC DC-DC converter when the resistance of the switches are negligible [8]. The second term represents the fast switching resistance which takes into account the resistance of the switches [8]. Therefore, the overall output impedance combines the capacitive and resistive losses of the SC converter.

Equations (1)–(5) show that there are optimum values for W, f_{sw}, and C_{fly} to maximize the efficiency. These optimum values depend on the given area, level of V_{out}, and the maximum allowable value of $V_{ripples}$. The value of V_{out} is given by Ref. [2],

$$V_{out} = V_{out,NL} \times \frac{R_{load}}{R_{load} + R_{out}} \tag{6}$$

where R_{load} is the load resistance.

Fig. 3 (a) shows a typical drawing of waveforms of $V_{ripples}$ and the output current pulses of the SC converter versus time. The main reason for $V_{ripples}$ is the shown current pulses. As depicted, the overall average current out from the converter is I_{load} while at charging and discharging phases of flying capacitors, the averages are $I_{load} \times (1 - 1/\xi)$ and $I_{load} \times (1 + 1/\xi)$, respectively, where ξ is the number of interleaving phases. Fig. 3 (b) presents the equivalent circuit model of the SC converter to model the waveforms shown in Fig. 3 (a). The average load current at R_{load} is always I_{load} during charging and discharging phases. Therefore, during the charging phase of flying capacitors, the load capacitor (C_{load}) gives I_{load}/ξ to R_{load}. Then, at the discharging phase of flying capacitors, the flying capacitors give the charges back to C_{load}. This charging-discharging operation on C_{load} is what causes the output voltage ripples.

It is important to note that the period (T_{sw}/ξ) depends on the number of used interleaving phases, ξ. With the aid of the model used in Fig. 3 (b), one can show that the value of $V_{ripples}$ is given by,

$$V_{ripples} = \frac{I_{load}}{2\xi^2 \times f_{sw} \times C_{load}} \tag{7}$$

Equations (1), (6) and (7) are used along with a constraint optimization algorithm to find the optimum values of W, f_{sw}, and C_{fly}. This optimization problem is defined as follows,

$$\begin{aligned} &Maximize: \ \eta(W, f_{sw}, C_{fly}) \\ &Given: \begin{cases} V_{out}(W, f_{sw}, C_{fly}) = h_1 \\ V_{ripples}(f_{sw}) \le h_2 \end{cases} \end{aligned} \tag{8}$$

where h_1 and h_2 are constants that determine the value of V_{out} and the maximum allowable value of $V_{ripples}$, respectively.

The constrained optimization problem in 8 is solved numerically using Lagrange multipliers, resulting in the optimum values for W, f_{sw},

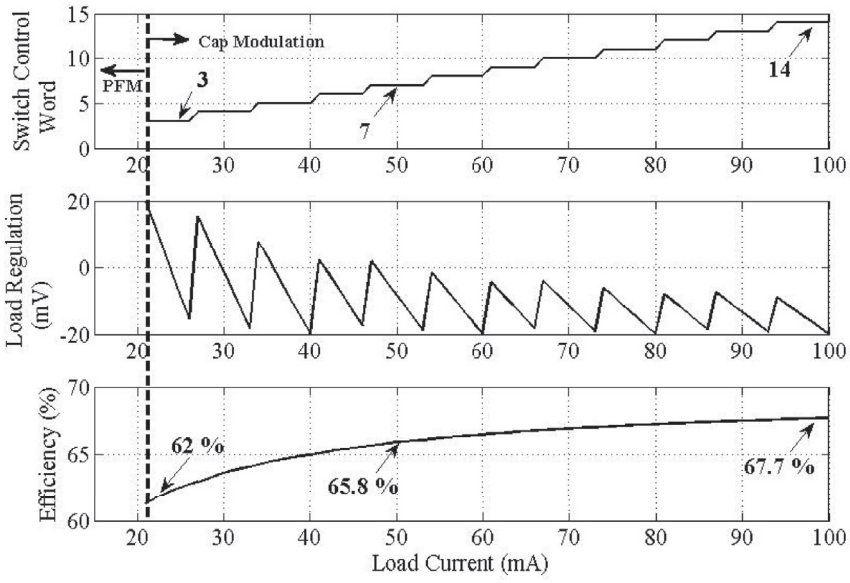

Fig. 5. Optimum switch control word, load regulation, and efficiency versus load current (CpM mode, V_{in} = 3.6 V and V_{out} = 1 V).

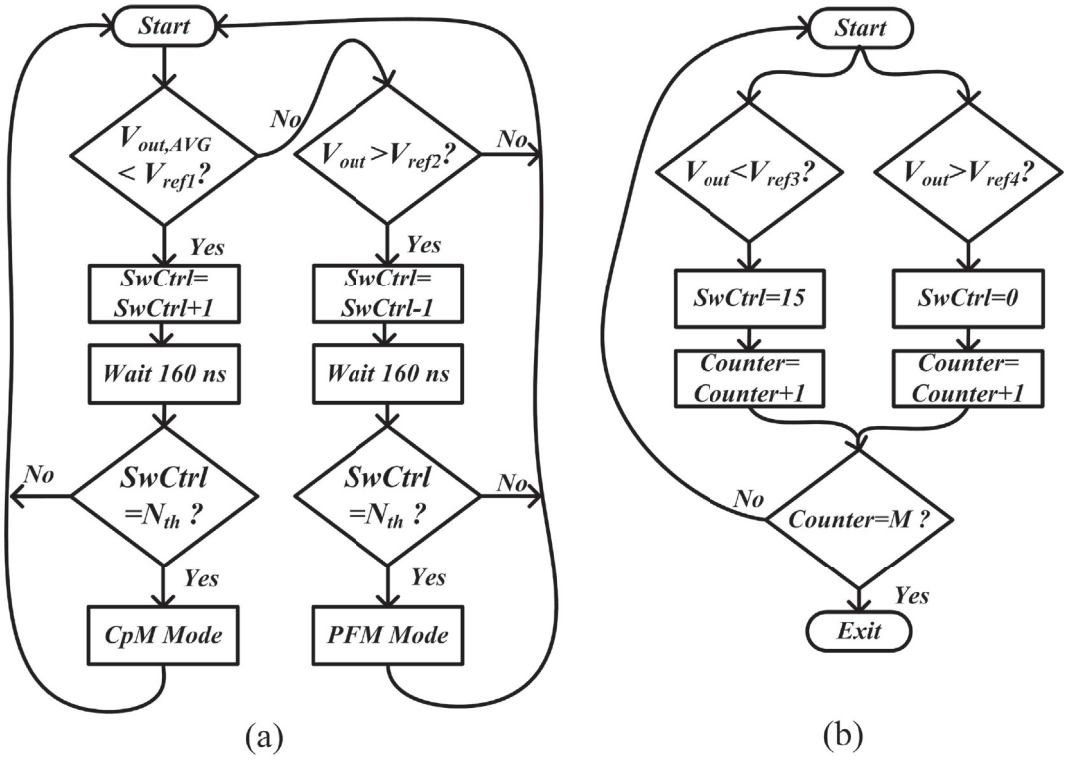

Fig. 6. SLCO flow chart diagram: (a) CpM\PFM modes (b) FTR.

and C_{fly}. Fig. 4 shows a plot for the efficiency for different values of f_{sw} and switch size (W) for a given I_{load} of 100 mA, C_{load} of 1 nF, V_{in} of 3.6 V, and C_{fly} of 3.84 nF. As indicated, the efficiency can be maximized if f_{sw} is set to 25 MHz with a switch size of 14 μm. However, at this maximum efficiency, values of V_{out} and $V_{ripples}$ are 0.9 V and 32 mV, respectively. Forcing V_{out} to 1 V and $V_{ripples}$ to 16 mV, the allowable region of solution is indicated by the solid area in Fig. 4. With the help of the constrained optimization problem given by equation (8), the maximum efficiency with the given values of V_{out} and $V_{ripples}$ is 68%. By keeping the same ratio between load resistance and output impedance in CpM mode, the value of the maximum efficiency is being tracked for any value of I_{load}. This is achieved through scaling the total switch size and flying capacitors by changing the switch control word. Fig. 5 shows the optimum control word for different load currents. As depicted, the load regulation is within 20 mV while the efficiency is degrading due to the $P_{control}$ losses. In PFM mode, f_{sw} is being scaled according to I_{load} to maintain the efficiency and V_{out}.

3. Switch Logic Controller

3.1. Capacitance modulation (CpM) mode

At heavy load conditions, CpM mode is being used for load regulation. As I_{load} decreases (increases), V_{out} starts to increase (decrease). Once V_{out} crosses a predetermined error (V_{ref1} and V_{ref2}), the switch control word is decreased (increased) according to the methodology

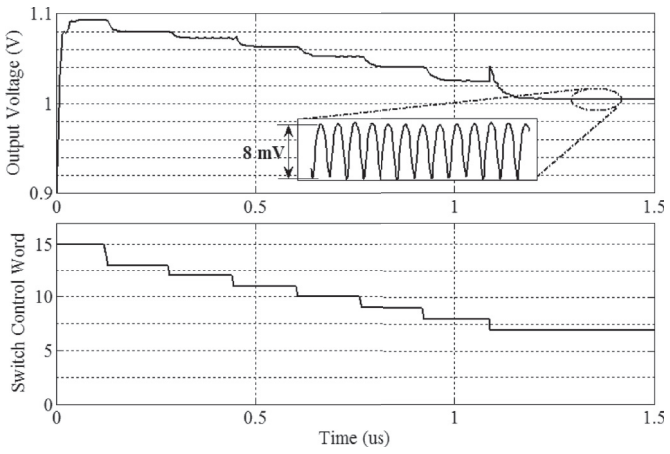

Fig. 7. Schematic-level simulated transient behavior for I_{load} = 50 mA and V_{in} = 3.6 V.

presented in Section 2 to maximize the efficiency and minimize load regulation value. Fig. 6 (a) shows the flow chart of the controller that implements the above mentioned operation. Values of V_{ref1} and V_{ref2} are set based on the maximum level of the load regulation. It is important to mention that the digital SLCO checks the level of V_{out} each 160 ns to guarantee that the output settles to the steady state value. In addition, phase interleaving is being used to further reduce $V_{ripples}$.

Fig. 7 shows the simulated settling behavior of the proposed SC converter using the SLCO for I_{load} of 50 mA. As indicated, the switch control word keeps changing until it settles to the optimum values within 1.2 μs. In this case, $V_{ripples}$ is less than 8 mV pp. Fig. 8 shows the simulated efficiency and load regulation value versus switch control word for I_{load} of 50 mA. As indicated, at a switch control word of 7, the minimum value of load regulation is achieved and efficiency reaches 65.8%.

Fig. 9 shows the simulated interleaving impact on ripples performance.

3.2. PFM mode

At light load current, PFM mode is used for load regulation combined with capacitance modulation to reduce the level of $V_{ripples}$ similar to the work done in Ref. [4]. While in the CpM mode, the SLCO detects I_{load} by monitoring the switch control word (N). When the value of N reaches a certain threshold value (N_{th}), the controller changes the operation from CpM to PFM to improve the efficiency and load regulation value. The value of N_{th} is selected such that the value of load regulation does not exceed a pre-specified value ($\Delta V_{out,th}$). The value of N_{th} is thus

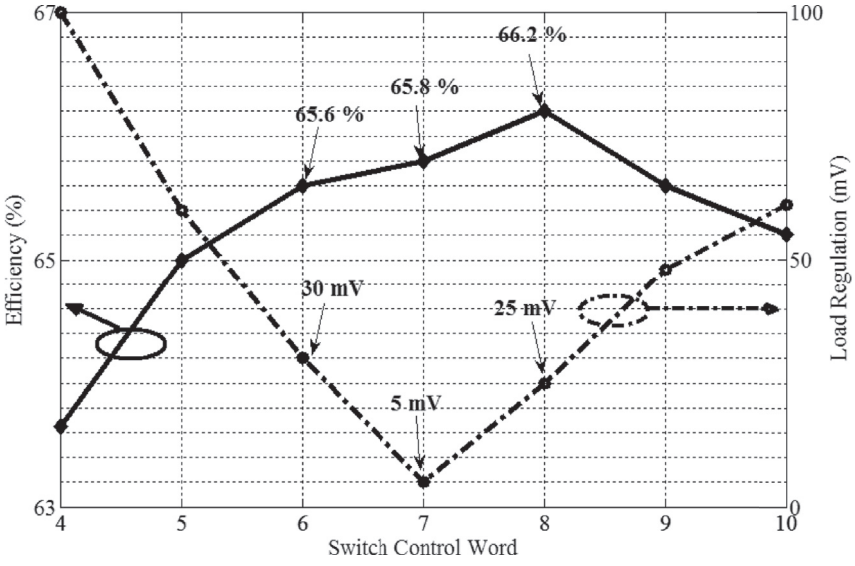

Fig. 8. Schematic-level simulated efficiency and load regulation versus switch control word for I_{load} = 50 mA and V_{in} = 3.6 V.

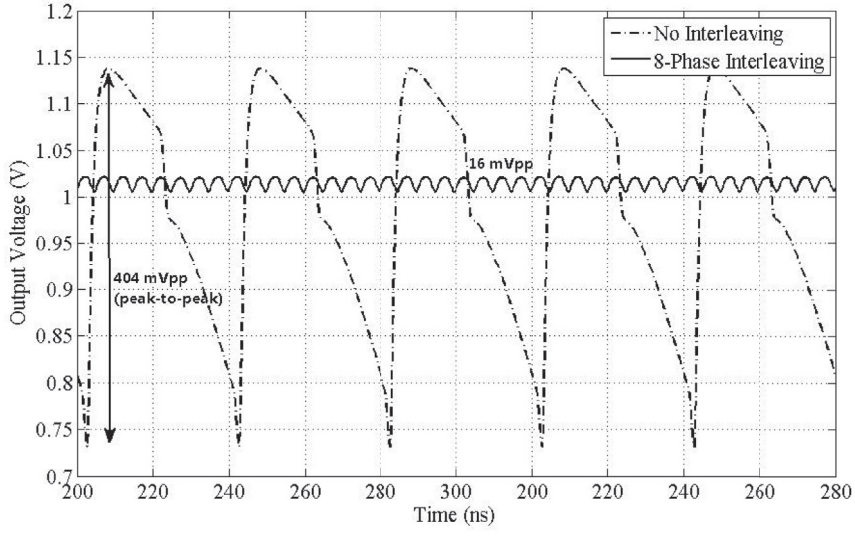

Fig. 9. Schematic-level simulated output voltage with and without interleaving for I_{load} = 100 mA and V_{in} = 3.6 V.

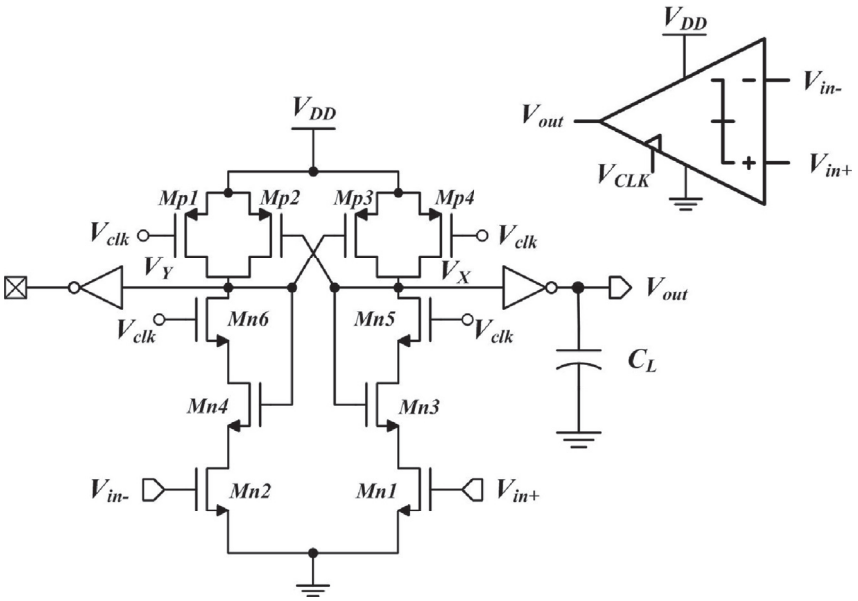

Fig. 10. Schematic-level diagram of the clocked comparator.

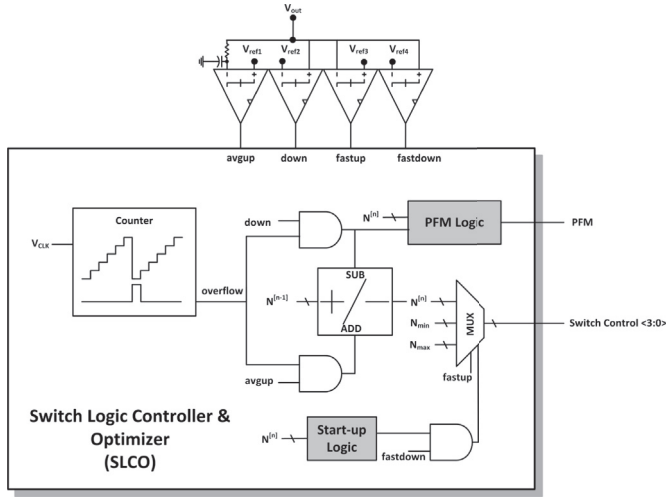

Fig. 11. Switch Logic Controller and Optimizer functionality block diagram.

given by,

$$\triangle V_{out,th} \leq V_{out,NL} \times \frac{R_{load,th}}{\frac{R_{out,unit}}{N_{th}+1} + R_{load,th}} - V_{out,NL} \times \frac{R_{load,th}}{\frac{R_{out,unit}}{N_{th}} + R_{load,th}} \quad (9)$$

where $R_{load,th}$ is the load resistance value at the boundary between PFM and CpM modes.

Fig. 6 (a) shows the flow chart for the digital SLCO to perform the required functionality.

3.3. Fast Transient Recovery technique

When a fast step in load current is applied to the SC converter, V_{out} drops or overshoots and the recovery time could be too high. To overcome this issue, V_{out} is sampled every 2.5 ns. When V_{out} drops (increases) below V_{ref3} (above V_{ref4}), the SLCO increases (decreases) the switch control word to its maximum (minimum) value. Hence, SC converter quickly charges (discharges) the output load capacitor to reduce the amount of undershoot (overshoot). Once V_{out} is above V_{ref3} (below V_{ref4}), the controller converges to the correct value of the switch control word according to the methodology discussed earlier in this section. Fig. 6 (b) shows the flow chart implemented within the controller to implement this functionality. A counter with maximum count of M has been added to prevent oscillation at start-up of the SC converter.

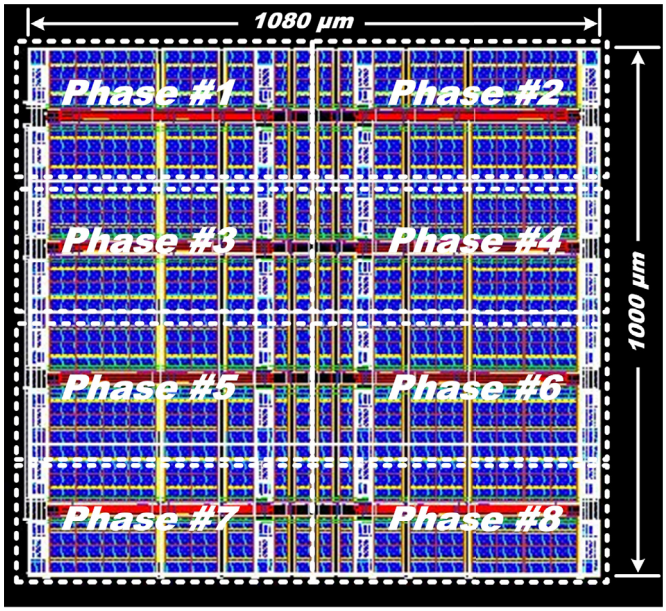

Fig. 12. Physical implementation of the proposed SC converter.

4. Circuit implementation

The proposed SC DC-DC converter has been implemented on 0.13 µm technology using thick oxide MOS devices. The power stage is implemented using a 3-to-1 series-parallel architecture (shown in Fig. 1) to convert the battery voltage 3.3 V – 4 V (~3.6 V nominal value) to ~1 V required for digital systems in sub-90 nm technology nodes. The usage of thick oxide MOS devices adds a challenge on the design because of its higher on resistance which requires increasing sizing of the power switches to decrease conduction loss. However, the larger the size of the MOS power switches, the larger the switching losses, which limits the maximum switching frequency. As a result, flying capacitors should be increased to compensate for the output resistance of converter. Using core devices for lower input supply levels

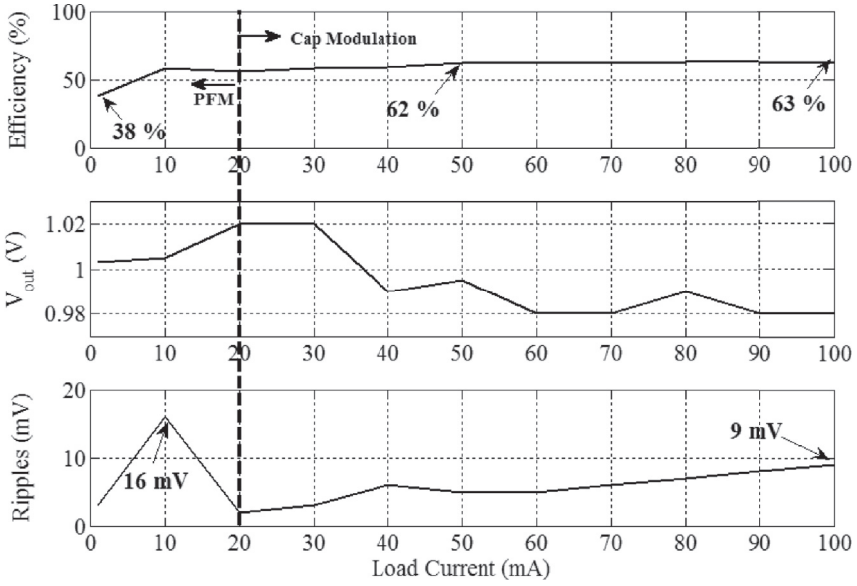

Fig. 13. Post-layout simulated efficiency, V_{out}, and output ripples versus load current for V_{in} = 3.6 V.

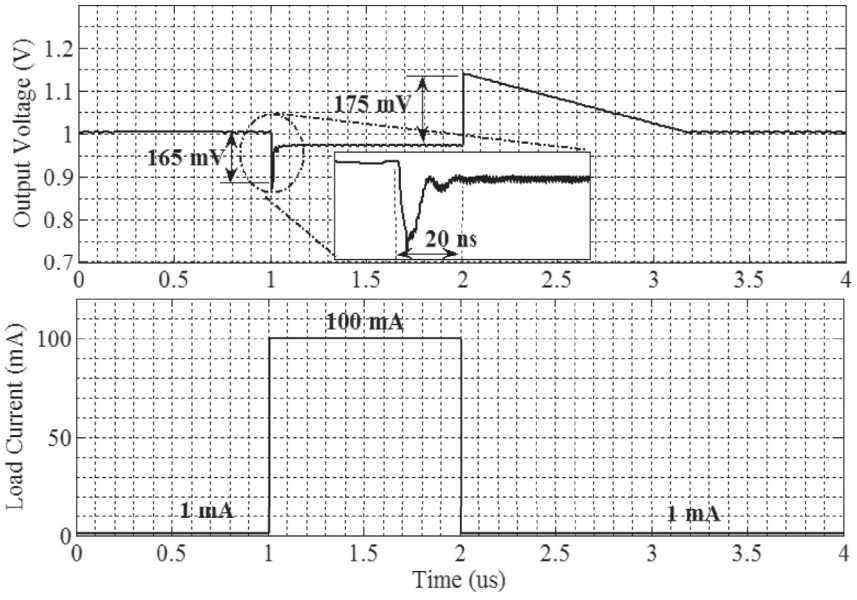

Fig. 14. Post-layout simulated I_{load} step from 1 mA to 100 mA with rise and fall time of 50 ps at V_{in} = 3.6 V.

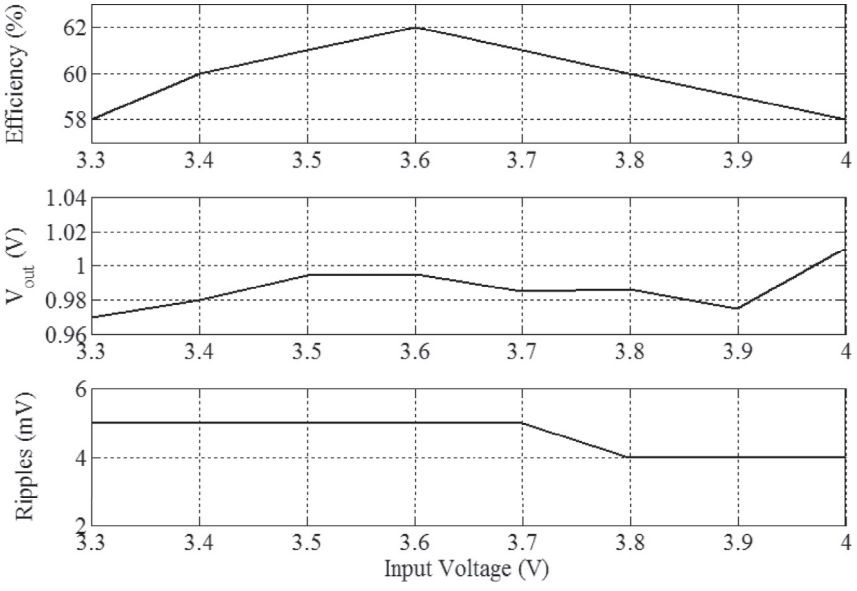

Fig. 15. Post-layout simulated efficiency, V_{out}, and output ripples versus input voltage for I_{load} = 50 mA.

Table 1
Comparison with prior work.

	[9]	[6]	[2]	[7]	[4]	[5]	This Work
Technology	130 nm Bulk	65 nm Bulk	90 nm Bulk	45 nm CMOS	130 nm CMOS	28-nm FDSOI	130 nm CMOS
Type of MOSFET	Thin Oxide	Thin Oxide	Thin Oxide	Thin Oxide	Thin Oxide	Thin Oxide	Thick Oxide
Approach	Mixed	Mixed	All-Digital	All-Digital	All-Digital	Mixed	All-Digital
Topology	3-level	1/3, 2/5 SC	1/2 SC	2/3 SC	1/3, 1/2 SC	1/3,1/2,2/3,4/3 SC	1/3 SC
$V_{in}(V)/V_{out}(V)$	2.4/(0.6–1.35)	(3–4)/1	3.6/1.5 3.0/1.3	1.8/(0.8–1)	1.2/(0.3–0.55)	1.8/(0.2–1.1)	(3.3–4)/1
Interleave/C_{fly}/C_{out}	4/18 nF/10 nF	18/3.88 nF/0	10/2 nF/3.2 nF	2/534 pF/700 pF	2/936 pF/5 nF	8/N.A./0	8/7.68 nF/1 nF (MOS)
Efficiency (η)/η_{peak}	63%/77%	73%/74.3%	74%/77%	N.A./69%	N.A./70%	*N.A.*/45.5% 72.5% 68.5 65%	62%/63%
Power Density (W/mm^2)@η	0.2	0.19	0.05	0.05 (incl. C_{load})	0.0245 (incl. C_{load})	0.146 *at* 0.34 V 0.31 *at* 0.72 V 0.386 *at* 0.9 V 0.412 *at* 0.96 V	0.095 (incl. C_{load})
Load Step (mA)@t_{rise}	220 mA → 370 mA @100 ps	0 → 162 mA @50 ps	42 mA → 72 mA @25 ns	270 μA → 7.6 mA *@N.A.*	N.A.	70 mA Step@ 1 ns	1 mA → 100 mA @50 ps
Droop	7.5% w/shunt reg.	7.6% w/3.3 GHz Sampling	2.1%	> 25%	N.A.	17%	17% w/400 MHz Sampling
Recovery Time	80 ns	< 1ns	N.A.	120 ns	N.A.	200 ns	20 ns
$I_{load,\max}$	~850 mA	~160 mA	~110 mA	8 mA	~50 mA (22 mW @ 0.4 V)	130 mA	100 mA
Load Regulation	N.A.	0.01%/mA (10–160 mA)	0.6%/mA	N.A.	0.2%/mA (2–32 mA)	N.A.	0.02%/mA (1–100 mA)
$V_{ripples}$	N.A.	< 50 mV	N.A.	< 50 mV	< 50 mV	100 mV	< 16 mV
f_{sw}	50 - 200 MHz	1 - 300 MHz	70 MHz (max)	30 MHz	< 200 MHz	N.A.	< 50 MHz

helps to increase the efficiency to values higher than 77%. Eight interleaving phases are used to drive the eight stages of the BWPS to reduce $V_{ripples}$. Each stage is 4-bits binary weighted 3-to-1 converters. Switches are driven with clock drivers that are implemented using scaled up inverters. Non-overlapping clocks are used to avoid shot-through currents. Clocked comparator, shown in Fig. 10, has the ability to detect an input voltage difference of 1 mV and is clocked with a 400 MHz clock. Then, 50 MHz eight phase clocks are generated using the phase shifter.

Fig. 11 shows the functionality block diagram of the SLCO. As depicted from the figure, the SLCO has four inputs which are "avgup", "down", "fastup", and "fastdown" signals and two outputs which are "PFM" and "Switch Control<3:0>". Those input signals are the outputs of the comparators, shown in Fig. 11, which are responsible for defining the output voltage level compared with reference voltages, as discussed earlier in Section 3.

The SLCO composes of an n-bit counter whose input is a reference clock and the output is the overflow signal. This overflow signal is used to determine the time instances at which the outputs of the comparators are checked to indicate a change in the state of the output voltage. The reference clock and the number of bits of the counter are chosen such that the output voltage settles before another comparison is performed. In this paper, the reference clock frequency is 50 MHz and the counter is a 3-bits one. At the end of each comparison, an avgup\down signal is generated to increase\decrease the Switch Control word in either the CpM or the PFM modes.

In case of a large step in the load current, the fastup or fastdown signal is triggered. In this case, the Switch Control word is set to its minimum ($N_{\min}$)\maximum ($N_{\max}$) when the load current decreases\increases.

Finally, a Start-up Logic is added to prevent any oscillations that may occur at start-up due to continuous triggering of the fastup and fastdown signals. In the start-up mode, the fastup and fastdown signals are masked until the output voltage settles to its steady-state value. This is achieved by monitoring the switch control word and ensuring that there is no change across two consecutive comparison cycles.

The SLCO consumes quiescent current of ~225 μA while the clocked comparator, MUX, and phase shifter consume 15, 60, and 120 μA, respectively, at CpM mode. At PFM mode the current consumption of the MUX and phase shifter scales according to f_{sw}.

The physical implementation of the proposed SC DC-DC converter is shown in Fig. 12. Each unit out of the eight units composes of the power stage switches, flying capacitors, clocks drivers, non-overlapping clock generator, and load capacitor of one phase segment. As shown from the figure, the proposed SC DC-DC converter covers an area of 1.08 mm^2 including the 1 nF load capacitor.

5. Simulation results

The SC converter is implemented and simulated using 0.13 μm CMOS technology. As mentioned earlier, thick oxide devices are used to design and implement the proposed SC converter. Main performance parameters simulations including efficiency, V_{out}, and $V_{ripples}$ across different values of I_{load} at an input voltage of 3.6 V are shown in Fig. 13. As depicted, at 20 mA the SC converter switches from PFM to CpM mode. In addition, efficiency higher than 56% is achieved in CpM mode. The peak efficiency reaches 63% at maximum load current. In the PFM mode, the efficiency degrades to 38% at load current of 1 mA. In all cases, the ripples are below 16 mV.

As depicted from the post-layout simulation results, the efficiency values has degraded ~5% due to parasitic capacitance and resistance of the interconnect metals in the physical implementation.

Fig. 14 shows the simulated step response of the converter when I_{load} changes from 1 mA to 100 mA in 50 ps and vice versa. As depicted, the SLCO responds to I_{load} step with an overshoot\undershoot less than 175 mV. In addition, the recovery time in the case of undershoot is less than 20 ns.

The main performance parameters simulations at I_{load} of 50 mA are shown across different values of input voltage in Fig. 15. As depicted, the peak efficiency occurs at V_{in} = 3.6 V, at which design optimization has been done. Moreover, the output voltage change across the whole input voltage range does not exceed 30 mV.

A performance summary of the proposed SC converter and other existing architectures are summarized in Table 1. As indicated, the proposed architecture achieves the lowest value of $V_{ripples}$ with a peak efficiency of 63% using thick oxide devices. The work in Ref. [6] achieved a higher efficiency, for the same voltage conversion ratio, but on the expense of being not a scalable all-digital solution.

In addition, in spite of being an all-digital solution, the load regulation is less than 0.02%/mA, the power density is 0.095 W/mm^2, the droop voltage and recovery time for 1 mA to 100 mA load current step in 50 ps are 17% and 20 ns, respectively. To our knowledge, these are the best reported values when compared to other all-digital solutions.

6. Conclusion

An all-digital Switched-Capacitor (SC) DC-DC converter with a Switch Logic Controller and Optimizer (SLCO) was presented in this paper. The SLCO achieved the maximum efficiency while keeping output voltage ripples and load regulation at minimum values. Capacitance modulation (CpM) and Pulse Frequency Modulation (PFM) are used to cover a wide dynamic range of load currents. Theoretical analysis and optimization algorithm were presented to achieve the maximum efficiency. The SC converter was implemented in 0.13 μm CMOS technology using thick oxide I/O devices and achieves a maximum efficiency of 63% at power density of 0.095 W/mm^2. The SC converter delivers up to 100 mA load current for an output voltage of 1 V from a 3.6 V nominal input voltage. Output voltage ripples and load regulation are less than 16 mV and 0.02%/mA, respectively.

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