Regular paper

A Unified Modeling Approach for DC-DC Converters Based on The Three-State Switching Cell

Wesley H. Maciel, José Augusto R. Carvalho, Fernando L. Tofoli

PII: S1434-8411(17)32355-5
DOI: https://doi.org/10.1016/j.aeue.2018.03.009
Reference: AEUE 52262

To appear in: *International Journal of Electronics and Communications*

Received Date: 4 October 2017
Accepted Date: 2 March 2018

Please cite this article as: W.H. Maciel, J.A.R. Carvalho, F.L. Tofoli, A Unified Modeling Approach for DC-DC Converters Based on The Three-State Switching Cell, *International Journal of Electronics and Communications* (2018), doi: https://doi.org/10.1016/j.aeue.2018.03.009

A Unified Modeling Approach for DC-DC Converters Based on The Three-State Switching Cell

Wesley H. Maciel, José Augusto R. Carvalho, and Fernando L. Tofoli
Department of Electrical Engineering
Federal University of São João del-Rei (UFSJ)
São João del-Rei-MG, Brazil
whmaciel@yahoo.com.br, jaugusto@outlook.com, fernandolessa@ufsj.edu.br

Abstract—This paper proposes a general small-signal model for the representation of dc-dc converters based on the three-state switching cell (3SSC) operating in continuous conduction mode (CCM). Even though such power electronic converters present distinct behaviors depending on the duty cycle range i.e. $0<D<0.5$ and $0.5<D<1$, the developed analysis effectively shows that the derived model is valid in either case. An approach similar to the PWM (pulse width modulation) switch is employed, being this a fair, simple, and straightforward technique if compared with other similar ones e.g. average state-space modeling. Dc and ac small-signal models can then be obtained in order to provide relevant expressions associated to the converters e.g. the static gain and several transfer functions used in the implementation of closed-loop control. A dc-dc buck converter is also investigated, whose model is properly represented by mathematical expressions that are validated by simulation tests for both operating conditions of the 3SSC.

Keywords—3SSC-based converters, dc-dc converter modeling, PWM switch model.

I. INTRODUCTION

Small-signal modeling of dc-dc converters is a well-known topic in literature, especially considering the application of linearized state-space models to obtain transfer functions that allow closed-loop operation [1]. However, this technique depends on a considerable amount of mathematical manipulations. For example, in the classical Ćuk, SEPIC (single-ended primary inductance converter), and Zeta converters, which are fourth-order systems, the inversion of 4×4 matrices is necessary. Besides, the analysis becomes quite complex as more parasitic elements are taken into account [2].

Other alternative solutions dedicated to small-signal modeling have also been introduced e.g. complementarity framework, even though it presents significant complexity [3]. Fourier series decomposition can also be used to model power converters, which are based on the Fourier series analysis of the PWM (pulse width modulation) signal within the mathematical representation of the model, thus minimizing the possibility of applying different or sophisticated control laws [4].

Among several distinct solutions, circuit averaging has proven to be effective for modeling purposes [5-7]. The PWM switch model proposed by Vorpérian for the analysis of dc-dc converters operating in CCM [8] and DCM (discontinuous conduction mode) [9] consists in a simple and direct approach from the point of view of electric circuits, analogously to that used in the

small-signal modeling of amplifiers using bipolar junction transistors (BJTs) [10, 11]. This technique has been widely applied to classical dc-dc converters, but it can be extended to other topologies with higher component count [12-14].

The classical nonisolated dc-dc converters i.e. buck, boost, buck-boost, Ćuk, SEPIC, and Zeta are widely employed in distinct applications [15]. However, operation at high power levels is typically not possible in practice since the load power is processed by a single semiconductor element in each operating stage. The 3SSC and a family of nonisolated dc-dc converters were proposed in [16] as an interesting alternative for this purpose, since the filter elements are designed for twice the switching frequency, with consequent reduction of overall dimension. Besides, the current stresses through the semiconductor elements are reduced and current sharing is maintained due to the autotransformer.

3SSC-based converters are able to operate in two distinct conditions depending on the value assumed by the duty cycle: nonoverlapping mode (NOM – D<0.5) and overlapping mode (OM – D>0.5). The 3SSC dc-dc buck converter operating in CCM was thoroughly analyzed in [17], as it is demonstrated that the mathematical analysis is not the same for each aforementioned mode, resulting in distinct design procedures for the power stage elements of a same topology. However, the small-signal modeling of converters employing the 3SSC has not yet been investigated in literature.

Within this context, this paper proposes a unified small-signal model that can be used in the representation of dc-dc converters derived from the 3SSC when operating in CCM. Firstly, the analysis focuses on the constitution of the 3SSC and respective operating modes i.e. NOM and OM. Thus the respective main theoretical waveforms can be determined in order to obtain both dc and ac models. The general model is then applied to a dc-dc buck converter, while the main transfer functions are presented. Considering both NOM and OM, such expressions are validated by means of simulation using ac sweep in PSIM® software.

II. Small-Signal Modeling of Dc-Dc Converters Based on The 3SSC in CCM

The 3SSC can be obtained from the dc-dc push-pull converter [16], being composed of two active switches S_1 and S_2; two diodes D_1 and D_2; and one autotransformer with unity turns ratio. The detailed analysis of Fig. 1 shows that it in fact comprises two PWM switches, which is due to the existence of two two-state switching cells (2SSCs), also referred to as canonical switching ones [18, 19].

According to [8], the PWM switch is a three-port element [20] whose terminals are: active (a), which is directly connected to the main switch; passive (p), which is directly connected to the diode; and common (c), which is connected to both semiconductors. A similar representation can then be adopted for the 3SSC. However, it is worth to mention that distinct operating conditions regarding the switching states of the semiconductors exist in NOM and OM, which are analyzed in detail as follows.

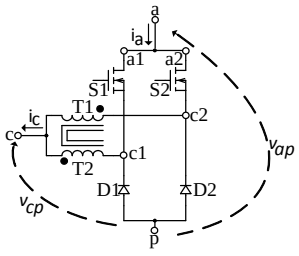


Fig. 1. Representation of the 3SSC.

A. Operation in NOM

If D<0.5, the 3SSC presents the complementary operation of semiconductors S_2-D_1 and S_1-D_2 in the first and third operating stages as shown in Fig. 2 (a) and Fig. 2 (c), respectively, while S_1 and S_2 are not turned on simultaneously during the switching period T_s. On the other hand, the active switches remain off during the second and fourth stages.

In order to model 3SSC-based dc-dc converters, the waveforms of the instantaneous current through the active terminal $i_a(t)$ and the instantaneous voltage across the common and passive terminals $v_{cp}(t)$ must be analyzed. Fig. 3 shows that the behavior of the aforementioned quantities is not the same as that observed in the PWM switch that exists in the conventional dc-dc topologies. In fact, current $i_a(t)$ flows through a single active switch in the first and third stages, corresponding to $i_{a1}(t)$ and $i_{a2}(t)$, respectively. On the other hand, it is null during the second and fourth stages. Similarly, it can be seen that $v_{cp}(t)$ is equal to half of the diode reverse voltage in the first and second stages, but null during the second and fourth ones, where both diodes are forward biased. Then the following conditions result for one switching period:

$$i_a(t)=\begin{cases} i_{a2}(t), & 0<t<D\cdot T_s \\ 0, & D\cdot T_s<t<\dfrac{T_s}{2} \\ i_{a1}(t), & \dfrac{T_s}{2}<t<\dfrac{(2\cdot D+1)}{2}\cdot T_s \\ 0, & \dfrac{(2\cdot D+1)}{2}\cdot T_s<t<T_s \end{cases} \tag{1}$$

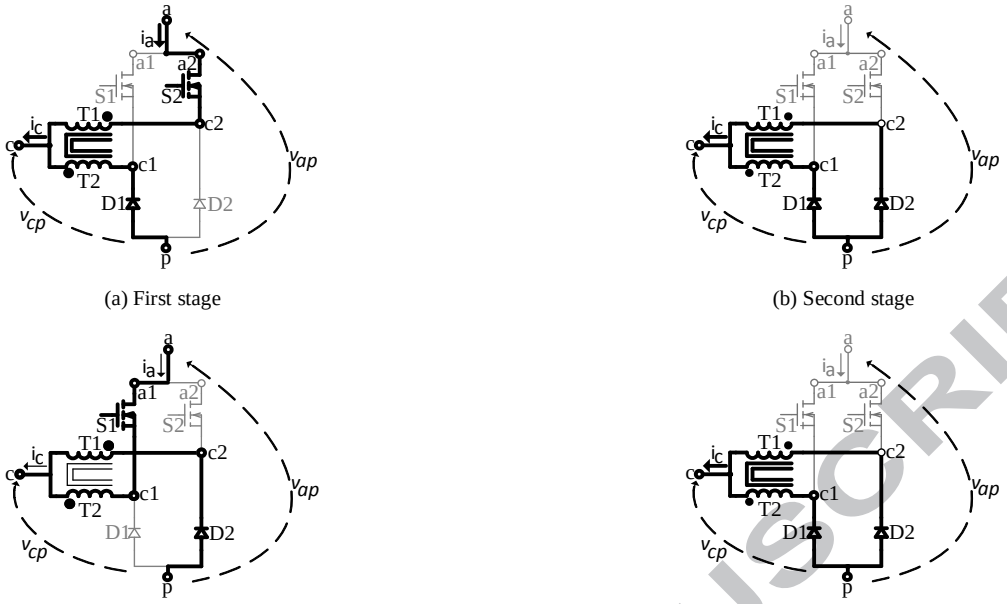
$$v_{cp}(t)=\begin{cases} \dfrac{v_{cp2}(t)}{2}, & 0<t<D\cdot T_s \\ 0, & D\cdot T_s<t<\dfrac{T_s}{2} \\ \dfrac{v_{cp1}(t)}{2}, & \dfrac{T_s}{2}<t<\dfrac{(2\cdot D+1)}{2}\cdot T_s \\ 0, & \dfrac{(2\cdot D+1)}{2}\cdot T_s<t<T_s \end{cases} \tag{2}$$

Considering that the autotransformer has unity turns ratio, the following statement is also valid:

$$i_a(t)=\begin{cases} \dfrac{i_c(t)}{2}, & 0<t<D\cdot T_s \\ 0, & D\cdot T_s<t<\dfrac{T_s}{2} \end{cases} \tag{3}$$

$$v_{cp}(t)=\begin{cases} \dfrac{v_{ap}(t)}{2}, & 0<t<D\cdot T_s \\ 0, & D\cdot T_s<t<\dfrac{T_s}{2} \end{cases} \tag{4}$$

where $i_c(t)$ is the instantaneous current through the common terminal and $v_{ap}(t)$ is the instantaneous voltage across the active and passive terminals.



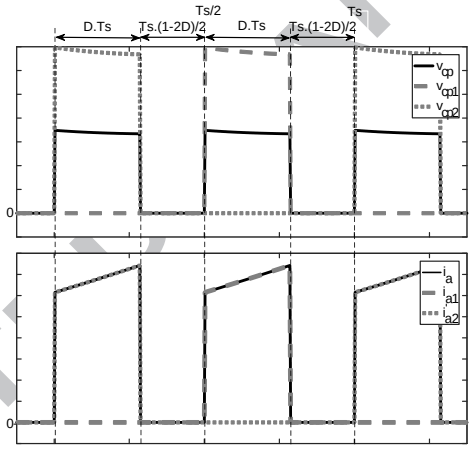
(a) First stage

(b) Second stage

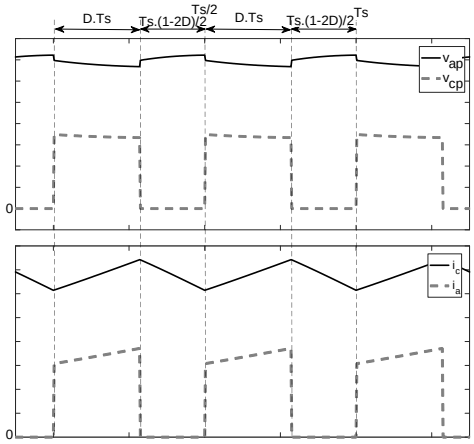
(c) Third stage

(d) Fourth stage

Fig. 2. Operating stages in NOM.



(a)



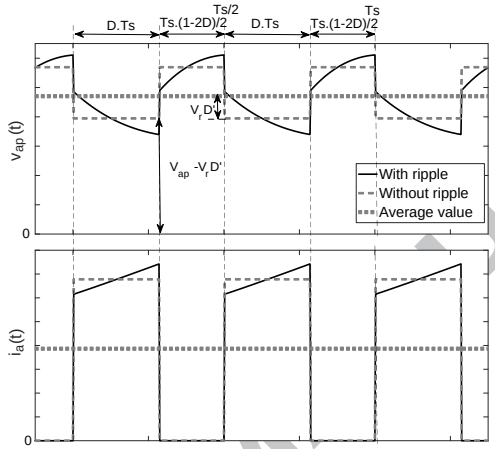
(b)

Fig. 3. Waveforms representing the operation in NOM.

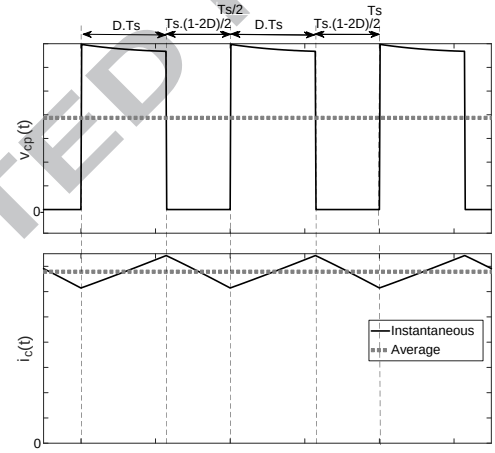
In this case, the average values of voltages and currents are of major interest rather than their respective instantaneous ones. Therefore it is important to determine them in order to assess the dc and ac small-signal models properly. According to Fig. 4, the behavior of $v_{ap}(t)$ is peculiar since terminals *a* and *p* are generally connected to a voltage source or a filter capacitor, which typically present an intrinsic series resistance. Therefore voltage $v_{ap}(t)$ is oscillatory as such series resistance draws a pulsating current, whose peak-to-peak amplitude is equal to the maximum value of $i_c(t)$. If the current ripple regarding $i_c(t)$ is neglected while only its respective average value I_c is considered, the ripple associated to $v_{ap}(t)$ can then be determined as:

$$V_r = R_e \cdot I_c \tag{5}$$

where the value of R_e depends on the path through which $i_c(t)$ flows and, consequently, on the converter topology under analysis.



(a)



(b)

Fig. 4. Average values of voltages and currents associated to the small-signal model in NOM.

Besides, if the high-frequency ripple associated to the instantaneous waveforms is neglected, it is possible to represent $i_a(t)$ and $v_{cp}(t)$ as a function of $i_c(t)$ and $v_{ap}(t)$ i.e.:

$$i_a(t) = \begin{cases} \dfrac{I_c}{2}, & 0 < t < D \cdot T_s \\ 0, & D \cdot T < t < \dfrac{T_s}{2} \end{cases} \tag{6}$$

$$v_{cp}(t)=\begin{cases}\dfrac{V_{ap}-V_r\cdot(1-D)}{2}, & 0<t<D\cdot T_s\\ 0, & D\cdot T_s<t<\dfrac{T_s}{2}\end{cases} \tag{7}$$

where V_{ap} is the average value of $v_{ap}(t)$.

Therefore the average values of $i_a(t)$ and $v_{cp}(t)$ i.e. I_a and V_{cp} can be determined from (6) and (7), respectively.

$$I_a=\frac{1}{(T_s/2)}\cdot\int_0^{T_s/2} i_a(t)\cdot dt \Rightarrow I_a=D\cdot I_c \tag{8}$$

$$V_{cp}=\frac{1}{(T_s/2)}\cdot\int_0^{T_s/2} v_{cp}(t)\cdot dt \Rightarrow V_{cp}=\left[V_{ap}-V_r\cdot(1-D)\right]\cdot D \tag{9}$$

It is worth to mention that (8) and (9) are invariant properties of the model independently on the dc-dc converter topology operating in NOM.

B. Operation in OM

Fig. 5 shows that switches S_1 and S_2 are on simultaneously during the first and third stages when D>0.5. Besides, at least one active switch is on during any operating stage. It is then expected that the voltage and current waveforms associated to terminals *a*, *p*, and *c* are not the same as those valid for NOM. Analyzing Fig. 6, it is possible to write the following expressions:

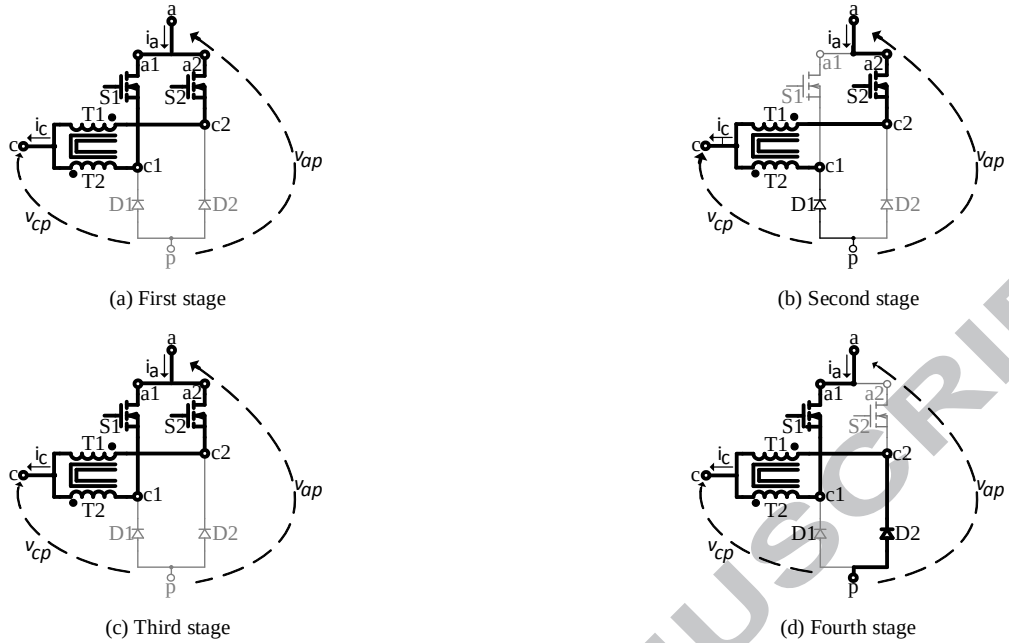
$$i_a(t)=\begin{cases}i_{a1}(t)+i_{a2}(t), & 0<t<\dfrac{(2\cdot D-1)\cdot T_s}{2}\\ i_{a2}(t), & \dfrac{(2\cdot D-1)\cdot T_s}{2}<t<\dfrac{T_s}{2}\\ i_{a1}(t)+i_{a2}(t), & \dfrac{T_s}{2}<t<D\cdot T_s\\ i_{a1}(t), & D\cdot T_s<t<T_s\end{cases} \tag{10}$$

$$v_{cp}(t)=\begin{cases}v_{cp2}(t), & 0<t<\dfrac{(2\cdot D-1)\cdot T_s}{2}\\ \dfrac{v_{cp2}(t)}{2}, & \dfrac{(2\cdot D-1)\cdot T_s}{2}<t<\dfrac{T_s}{2}\\ v_{cp1}(t), & \dfrac{T_s}{2}<t<D\cdot T_s\\ \dfrac{v_{cp1}(t)}{2}, & D\cdot T_s<t<T_s\end{cases} \tag{11}$$

Since the autotransformer presents unity turns ratio, current $i_c(t)$ and voltage $v_{cp}(t)$ can be represented as:

$$i_a(t)=\begin{cases}i_c(t), & 0<t<\dfrac{(2\cdot D-1)\cdot T_s}{2}\\ \dfrac{i_c(t)}{2}, & \dfrac{(2\cdot D-1)\cdot T_s}{2}<t<\dfrac{T_s}{2}\end{cases} \tag{12}$$

$$v_{cp}(t)=\begin{cases}v_{ap}(t), & 0<t<\dfrac{(2\cdot D-1)\cdot T_s}{2}\\ \dfrac{v_{ap}(t)}{2}, & \dfrac{(2\cdot D-1)\cdot T}{2}<t<\dfrac{T_s}{2}\end{cases} \tag{13}$$



(a) First stage

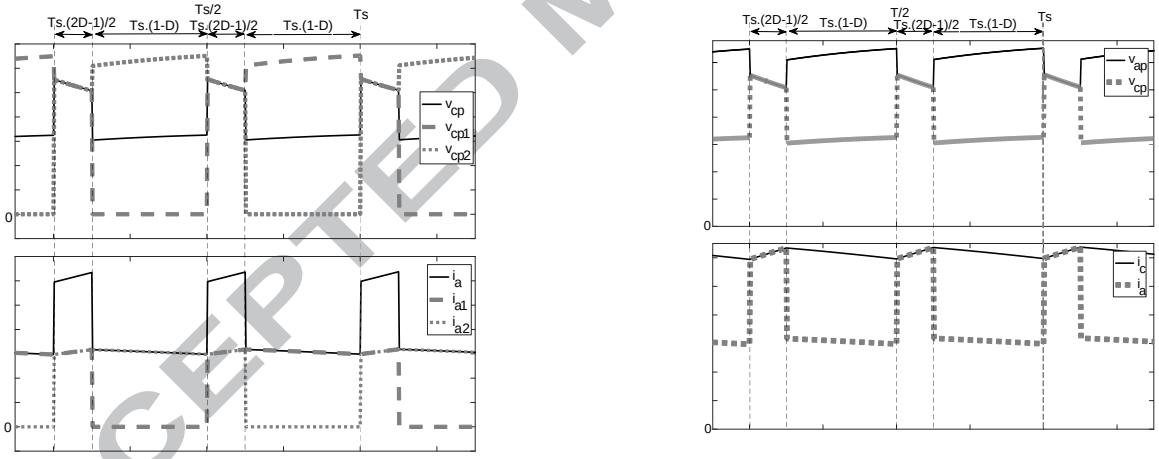
(b) Second stage

(c) Third stage

(d) Fourth stage

Fig. 5. Operating stages in OM.

Analogously to NOM, voltage $v_{ap}(t)$ presents oscillatory behavior in Fig. 7 due to the existence of resistance R_e in the path of current $i_c(t)$ as discussed before. If the high-frequency ripple associated to the instantaneous waveforms is neglected, expressions (14) and (15) result, which can be used to calculate I_a and V_{cp} in (16) and (17), respectively.



(a)

(b)

Fig. 6. Waveforms representing the operation in OM.

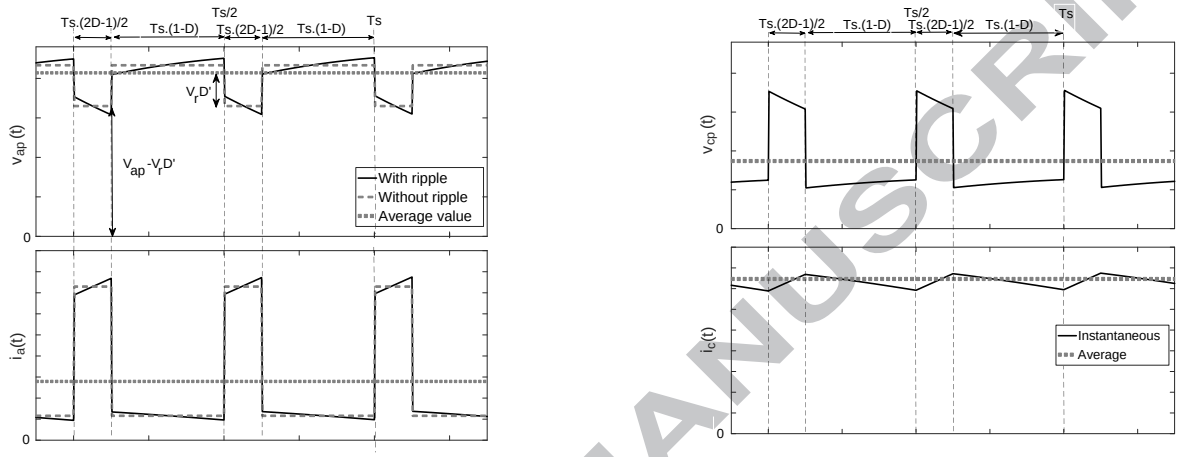
$$i_a(t) = \begin{cases} I_c, & 0 < t < \dfrac{(2\cdot D-1)\cdot T_s}{2} \\ \dfrac{I_c}{2}, & \dfrac{(2\cdot D-1)\cdot T_s}{2} < t < \dfrac{T_s}{2} \end{cases} \tag{14}$$

$$v_{cp}(t) = \begin{cases} V_{ap} - V_r\cdot(1-D), & 0 < t < \dfrac{(2\cdot D-1)\cdot T_s}{2} \\ \dfrac{V_{ap} - V_r\cdot(1-D)}{2}, & \dfrac{(2\cdot D-1)\cdot T_s}{2} < t < \dfrac{T_s}{2} \end{cases} \tag{15}$$

$$I_a = \frac{1}{(T_s/2)} \cdot \int_0^{T_s/2} i_a(t) \cdot dt \Rightarrow I_a = D \cdot I_c \tag{16}$$

$$V_{cp} = \frac{1}{(T_s/2)} \cdot \int_0^{T_s/2} v_{cp}(t) \cdot dt \Rightarrow V_{cp} = \left[V_{ap} - V_r \cdot (1-D) \right] \cdot D \tag{17}$$

It can be seen that the invariant properties given by (16) and (17) are identical to the ones obtained in (8) and (9) for the operation in NOM. Therefore it can be stated that a unified small-signal model can be used to represent 3SSC-based dc-dc converter over the entire range of the duty cycle.



(a) (b)

Fig. 7. Average values of voltages and currents associated to the small-signal model in OM.

C. DC and AC Models

Analyzing (16) and (17) or (8) and (9), it is possible to define the following ratio:

$$\frac{I_c}{I_a} = \frac{1}{D} = \frac{V_{ap}}{V_{c1p}} \tag{18}$$

$$V_{cp} = V_{c1p} - D \cdot D' \cdot V_r = D \cdot \left(V_{ap} - R_e \cdot I_c \cdot D' \right) \tag{19}$$

where $D'=1-D$ is the complementary duty cycle, and V_{c1p} is the average value of the voltage across terminals *c1* and *p* as shown in Fig. 8.

It is then possible to establish an analogy between expression (19) and a transformer, whose turns ratio depends on the duty cycle. The dc model shown in Fig. 8 can then be used, which is similar to the representation valid for dc-dc converters based on the canonical cell.

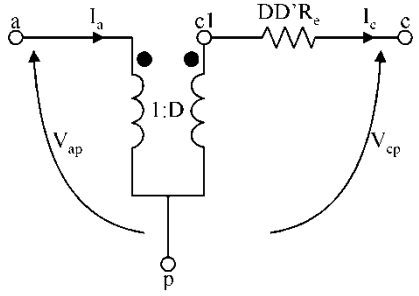


Fig. 8. Dc model used to represent 3SSC-based dc-dc converters in CCM.

Now, in order to derive the ac model, one must consider that the average values of the previously defined parameters (D, I_a, I_c, V_{ap}, V_{cp}) are influenced by their respective small-signal perturbations ($\hat{d}$, i_a, $\hat{i}_c$, v_{ap}, v_{cp}). Therefore, expressions (16) and (17) become (20) and (21), respectively.

$$I_a + \hat{i}_a = \left(D + \hat{d}\right) \cdot \left(I_c + \hat{i}_c\right) \tag{20}$$

$$V_{cp} + \hat{v}_{cp} = \left(D + \hat{d}\right) \cdot \left\{\left(V_{ap} + \hat{v}_{ap}\right) - \left(I_c + \hat{i}_c\right) \cdot R_e \cdot \left[1 - \left(D + \hat{d}\right)\right]\right\} \tag{21}$$

Differentiating both sides of (20) and (21), and also neglecting the terms where the product of two perturbations exists, it is possible to write:

$$i_a = D \cdot i_c + I_c \cdot d \tag{22}$$

$$v_{cp} = D \cdot v_{ap} - D \cdot R_e \cdot (1 - D) \cdot i_c + d \cdot V_D \tag{23}$$

where:

$$V_D = V_{ap} + I_c \cdot R_e \cdot (D - D') \tag{24}$$

and i_a, i_c, d, v_{ap}, v_{cp} correspond to the derivatives of $\hat{d}$, i_a, $\hat{i}_c$, v_{ap}, v_{cp}, respectively.

Considering that terms $I_c \cdot d$ and $d \cdot V_D$ in (22) and (23) can be treated as a current source and a voltage source, respectively, both perturbed by the duty cycle, the ac model shown in Fig. 9 can finally be obtained. If all perturbations are neglected, it is worth to mention that the same representation in Fig. 8 results.

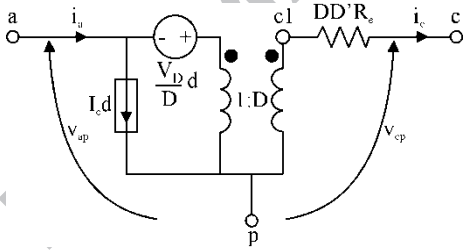


Fig. 9. Ac model used to represent 3SSC-based dc-dc converters in CCM.

III. Small-Signal Analysis of The Buck Converter Employing the 3SSC

The 3SSC buck converter using the cell type B is shown in Fig. 10 (a), where all semiconductor elements are considered ideal. However, the intrinsic series resistance of the filter inductor R_L and the equivalent series resistance of the output filter capacitor R_{SE} are represented in the circuit. By using the ac model represented in Fig. 9, it can be seen that it is quite simple to include parasitic elements as desired.

The static gain of the converter can be determined from Fig. 10 (b) considering the following assumptions: the duty cycle is constant and equal to D; the output filter capacitor is open; the inductor is represented only by its respective resistance R_L; the average input voltage is equal to V_i. The circuit analysis leads to:

$$\frac{V_o}{V_i} = \frac{D \cdot R_o}{R_L + R_o} \tag{25}$$

where V_o is the average output voltage.

If R_L=0 in (25), it can be seen that the static gain is the same as that regarding a conventional buck converter operating in CCM.

Besides, analyzing Fig. 10 (b) and using distinct techniques and properties associated to electric circuits, it is possible to derive distinct transfer functions involving several variables e.g. the input voltage $v_i(s)$, input current $i_i(s)$, output voltage $v_o(s)$, output current $i_o(s)$, duty cycle $d(s)$, and inductor current $i_L(s)$.

For instance, in order to determine the input-to-output transfer function $v_o(s)/v_i(s)$, the duty cycle is assumed constant and equal to D, while the input voltage is perturbed. After simplifying the resulting circuit and some mathematical manipulation, the following expressions results:

$$\frac{v_o(s)}{v_i(s)} = \frac{D \cdot R_o \cdot (C \cdot R_{SE} \cdot s + 1)}{\left[C \cdot L \cdot (R_o + R_{SE})\right] \cdot s^2 + \left[C \cdot (R_L \cdot R_o + R_L \cdot R_{SE} + R_o \cdot R_{SE}) + L\right] \cdot s + (R_L + R_o)} \tag{26}$$

Analogously, it is possible to obtain the control-to-output transfer function $v_o(s)/d(s)$ if the input voltage is constant and equal to V_i, while the duty cycle is perturbed, resulting in:

$$\frac{v_o(s)}{d(s)} = \frac{V_i \cdot R_o \cdot (C \cdot R_{SE} \cdot s + 1)}{\left[C \cdot L \cdot (R_o + R_{SE})\right] \cdot s^2 + \left[C \cdot (R_L \cdot R_o + R_L \cdot R_{SE} + R_o \cdot R_{SE}) + L\right] \cdot s + (R_L + R_o)} \tag{27}$$

Other relevant transfer functions can also be obtained from the analysis of the ac model as follows:

$$Z_i(s) = \frac{v_i(s)}{i_i(s)} = \frac{(R_o + R_{SE}) \cdot L \cdot C \cdot s^2 + \left[(R_L \cdot R_o + R_L \cdot R_{SE} + R_{SE} \cdot R_o) \cdot C + L\right] \cdot s + (R_o + R_L)}{D^2 \cdot \left[(R_o + R_{SE}) C \cdot s + 1\right]} \tag{28}$$

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} = \frac{R_o \cdot \left[R_{SE} \cdot L \cdot C \cdot s^2 + (R_L \cdot R_{SE} \cdot C + L) \cdot s + R_L\right]}{(R_o + R_{SE}) L \cdot C \cdot s^2 + \left[(R_L \cdot R_o + R_L \cdot R_{SE} + R_{SE} \cdot R_o) \cdot C + L\right] \cdot s + (R_o + R_L)} \tag{29}$$

$$\frac{v_o(s)}{i_L(s)} = \frac{R_o \cdot (R_{SE} \cdot C \cdot s + 1)}{(R_o + R_{SE}) \cdot C \cdot s + 1} \tag{30}$$

$$\frac{i_L(s)}{d(s)} = \frac{V_i \cdot \left[(R_o + R_{SE}) \cdot C \cdot s + 1\right]}{(R_o + R_{SE}) \cdot L \cdot C \cdot s^2 + \left[(R_L \cdot R_o + R_L \cdot R_{SE} + R_{SE} \cdot R_o) \cdot C + L\right] \cdot s + (R_L + R_o)} \tag{31}$$

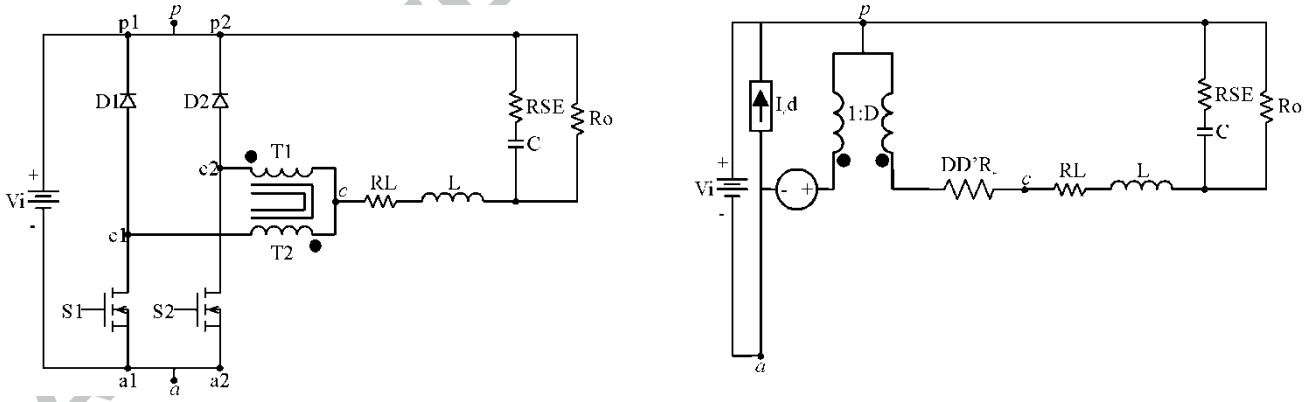


Fig. 10. 3SSC buck converter employing cell B: (a) power stage and (b) ac model.

The careful analysis of expressions (25) to (31) shows that the static gain and the aforementioned transfer functions are exactly identical to the ones valid for the conventional dc-dc buck converter in CCM. It is also expected that the proposed model applied to the family of converters described in [16] provides the very same results as those regarding other classical dc-dc converter topologies.

Finally, it is worth to mention that expression (27) is necessary for the implementation of voltage mode control, as the output voltage remains constant if the load comes to vary. Similarly, expressions (30) and (31) are required by average current mode control, where two control loops exist.

IV. MODEL VALIDATION

It is possible to validate the small-signal model by using two approaches: (a) performing ac sweep with dedicated simulation software and (b) analyzing the dynamic response of the output when a disturbance is applied to the input [21]. The gain and phase Bode plots associated to expressions (26) to (31) can be obtained using ac sweep in PSIM® software and considering the 3SSC dc-dc buck converter shown in Fig. 10 (a). An arbitrary operating point has been chosen according to the specifications given in Table I, which corresponds to OM.

According to the plots in Fig. 11 to Fig. 16, the theoretical curves that represent the model and the ones obtained by simulation corresponding to the converter operation are nearly identical. Since the model is valid for the entire range of the duty cycle, it is able to represent the converter adequately.

Table I. Design specifications of the 3SSC buck converter in OM (D>0.5).

Parameter	**Value**
Input voltage	V_i=200 V
Output voltage	V_o=150 V
Output power	P_o=1 kW
Load resistance	R_o=22.5 Ω
Switching frequency	f_s=30 kHz
Duty cycle	D=0.75
Output filter capacitance	C=2.40 µF
Filter inductance	L=312 µH
Equivalent series resistance of the output filter capacitor	R_{SE}=10 mΩ
Series resistance of the filter inductor	R_L=1 mΩ
Inductor current ripple	ΔI_L=1.33 A
Output voltage ripple	ΔV=1.5 V

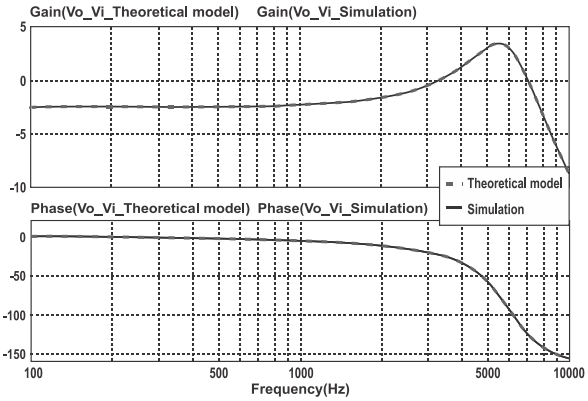


Fig. 11. Bode plots for $v_o(s)/v_i(s)$ and D=0.75.

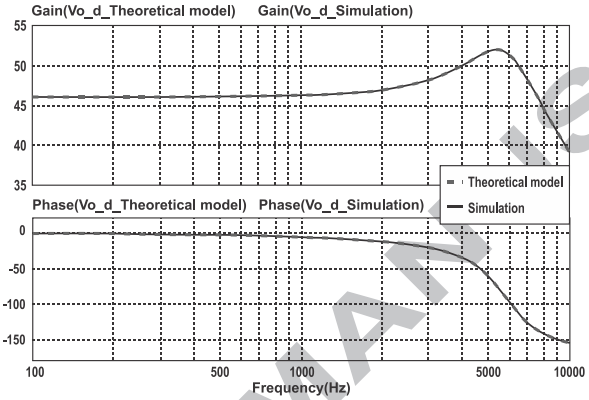


Fig. 12. Bode plots for $v_o(s)/d(s)$ and D=0.75.

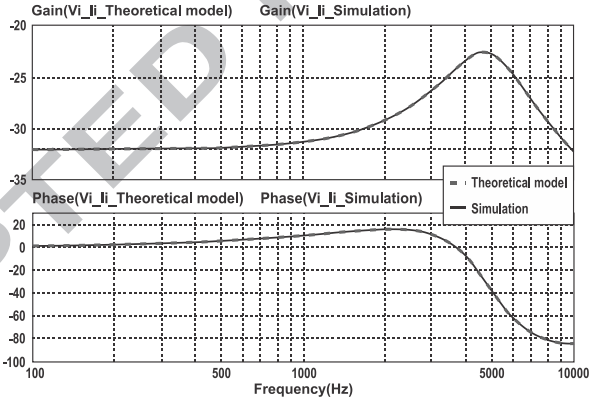


Fig. 13. Bode plots for $Z_i(s)=v_i(s)/i_i(s)$ and D=0.75.

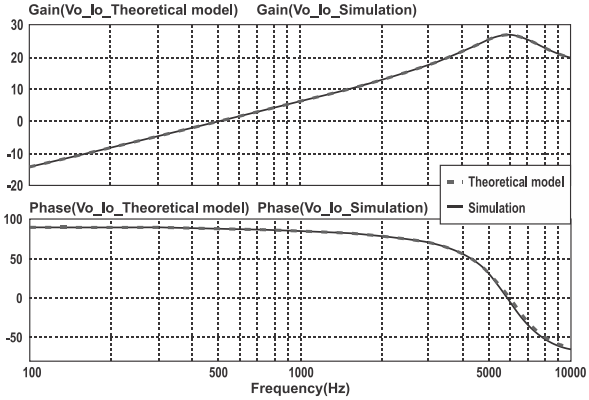


Fig. 14. Bode plots for $Z_o(s)=v_o(s)/i_o(s)$ and D=0.75.

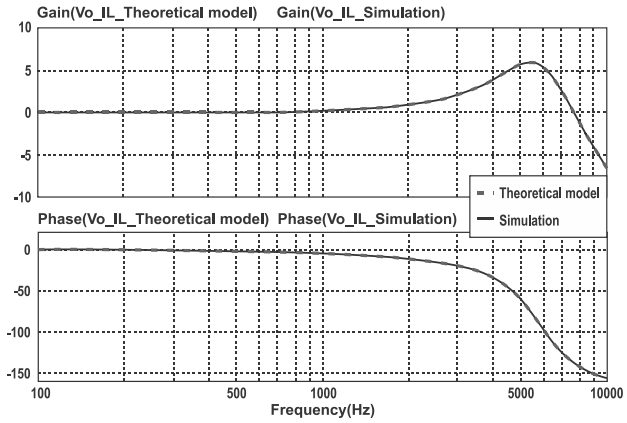


Fig. 15. Bode plots for $v_o(s)/i_L(s)$ and D=0.75.

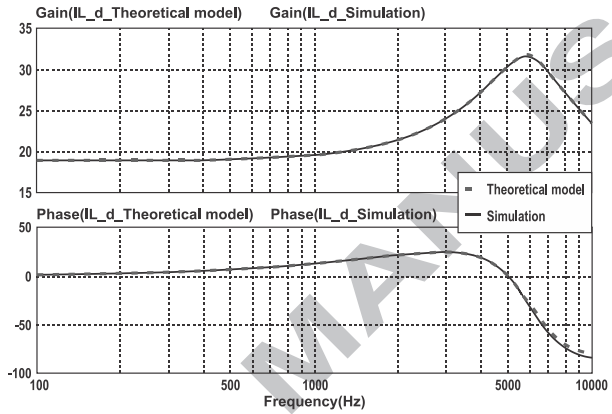


Fig. 16. Bode plots for $i_L(s)/d(s)$ and D=0.75.

Now, let us analyze the dynamic behavior of the model compared with the converter performance considering the input-to-output and control-to-output transfer functions and the specifications given in Table I. Fig. 17 shows that the average model is able to represent the converter start-up from t=0 properly, where there are no initial conditions for the filter inductor and filter capacitor. The duty cycle remains constant at 0.75 during 30 ms, although the input voltage decreases from 200 V to 150 V at t=10 ms, thus causing the output voltage to be reduced from 150 V to 112.5 V as defined by the static gain in (25). Once again, the input voltage varies from 150 V to 250 V at t=20 ms, as the output voltage increases from 112.5 V to 187.5 V in both the converter and the model.

Analogously, the model is evaluated regarding the behavior of $v_o(s)/d(s)$, where the input voltage remains constant at V_i=200 V. The duty cycle is reduced from 0.75 to 0.25 at t=10 ms, and increased from 0.25 to 0.5 at t=20 ms, where it can be seen that the output voltage varies as expected in both cases. Therefore it is reasonable to state that the proposed approach is able to represent the converter in both NOM and OM.

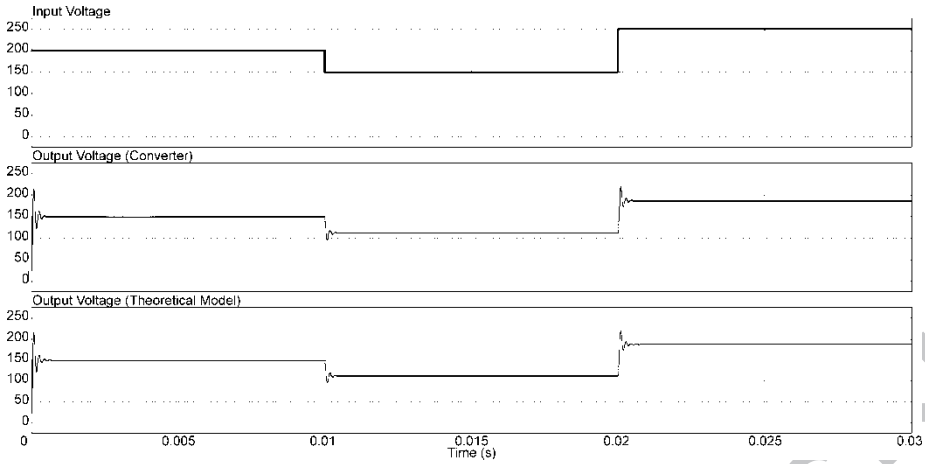


Fig. 17. Dynamic behavior of the converter and small-signal model for $v_o(s)/v_i(s)$ when the input voltage is perturbed.

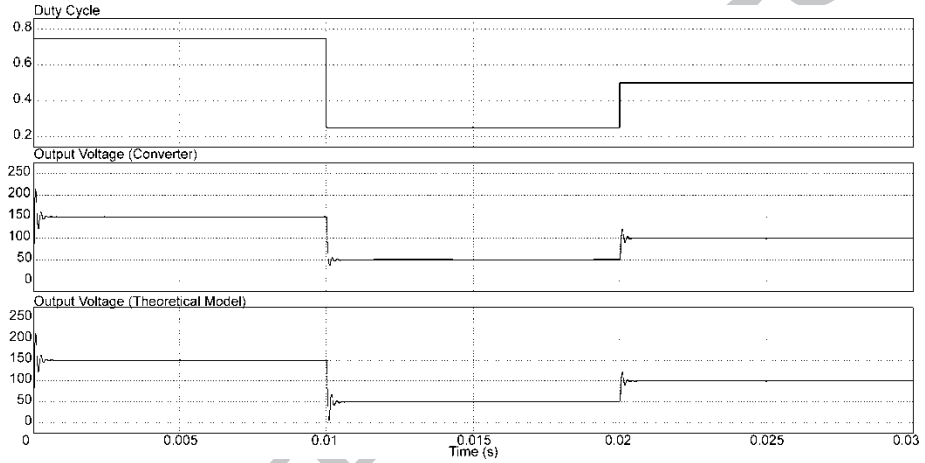


Fig. 18. Dynamic behavior of the converter and small-signal model for $v_o(s)/d(s)$ when the duty cycle is perturbed.

V. Conclusion

The small-signal modeling approach proposed for dc-dc converters based on the 3SSC in CCM has proven to be a simple and straightforward technique, considering that the analysis is strictly carried out from the point of view of electric circuits. It has been show that it is able to represent the topologies operating in both operating modes i.e. NOM and OM, which can be typically found in 3SSC-based structures.

A 3SSC dc-dc buck converter has been analyzed in detail, whose model has been properly validated comparing the Bode plots of the theoretical model with the ones obtained by simulation. It is worth to mention that the derived transfer functions are strictly important for the closed-loop operation of the converters. Besides, it has been proven that the resulting expressions are exactly the same ones valid for the conventional buck converter operating in CCM.

Finally, it can be stated that the aforementioned modeling technique can easily be extended to other 3SSC converters, thus allowing the development of their respective small-signal models with few mathematical manipulations if compared to the average state-space technique.

VI. Acknowledgment

The authors are thankful to overall support provided by CAPES, CNPq, FAPEMIG, and INERGE.

References

[1] S. C. Smithson and S. S. Williamson, "A unified state-space model of constant-frequency current-mode-controlled power converters in continuous conduction mode," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 4514-4524, 2015.
[2] Deepak, R. K. Pachauri, and Y. K. Chauhan, "Modeling and simulation analysis of PV fed Cuk, Sepic, Zeta and Luo DC-DC converter," in *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, 2016, pp. 1-6.
[3] F. Vasca, L. Iannelli, M. K. Camlibel, and R. Frasca, "A new perspective for modeling power electronics converters: complementarity framework," *IEEE Transactions on Power Electronics*, vol. 24, pp. 456-468, 2009.
[4] A. Jaafar, P. Lefranc, E. Godoy, X. L. Shi, A. Fayaz, and N. Li, "Experimental validation with a control point of view analysis of the SEPIC converter," in *2009 35th Annual Conference of IEEE Industrial Electronics*, 2009, pp. 462-497.
[5] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Transactions on Power Electronics*, vol. 6, pp. 251-259, 1991.
[6] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and control of the isolated DC-DC modular multilevel converter for electric ship medium voltage direct current power system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, pp. 124-139, 2017.
[7] A. Villarruel-Parra and A. J. Forsyth, "Enhanced average-value modeling of interleaved DC-DC converters using sampler decomposition," *IEEE Transactions on Power Electronics*, vol. 32, pp. 2290-2299, 2017.
[8] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, pp. 490-496, 1990.
[9] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, pp. 497-505, 1990.
[10] L. Safari and S. Minaei, "A novel COA-based electronically adjustable current-mode instrumentation amplifier topology," *AEU - International Journal of Electronics and Communications*, vol. 82, pp. 285-293, 2017/12/01/ 2017.
[11] U. Bansal and M. Gupta, "Two stage class AB-AB amplifier using FGMOS for low voltage operation and SSF for frequency compensation," *AEU - International Journal of Electronics and Communications*, vol. 73, pp. 59-67, 2017/03/01/ 2017.
[12] K. D. T. Ngo, "Alternate forms of the PWM switch models," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 35, pp. 1283-1292, 1999.
[13] V. Vorperian and W. T. McLyman, "Analysis of a PWM-resonant converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 33, pp. 163-170, 1997.
[14] C. Y. Chang, W. S. Liu, J. F. Chen, R. L. Li, N. T. J. Liang, and M. H. Chen, "Modified PWM switch model for continuous conduction mode DC-DC converters with coupled inductors," *IET Power Electronics*, vol. 3, pp. 629-636, 2010.
[15] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed.: Wiley & Sons, 2002.
[16] G. V. T. Bascope and I. Barbi, "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cells," in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, 2000, pp. 858-863 vol.2.
[17] J. P. R. Balestero, F. L. Tofoli, C. M. d. Seixas, G. V. T. Bascopé, and F. J. M. d. Seixas, "Comparative analysis between overlapping and non-overlapping operation modes for the PWM buck converter using the three-state switching cell," *International Journal of Electronics*, vol. 101, pp. 553-568, 2014/04/03 2014.
[18] B. Singh and A. Anand, "A PFC based SRM motor drive using a canonical switching cell converter," in *2016 IEEE 6th International Conference on Power Systems (ICPS)*, 2016, pp. 1-6.
[19] S. Singh, V. Bist, B. Singh, and G. Bhuvaneswari, "Power factor correction in switched mode power supply for computers using canonical switching cell converter," *IET Power Electronics*, vol. 8, pp. 234-244, 2015.
[20] A. Soltan, A. M. Soliman, and A. G. Radwan, "Fractional-order impedance transformation based on three port mutators," *AEU - International Journal of Electronics and Communications*, vol. 81, pp. 12-22, 2017/11/01/ 2017.
[21] F. Mohammad, J. Sampe, S. Shireen, and S. Hamid Md Ali, "Minimum passive components based lossy and lossless inductor simulators employing a new active block," *AEU - International Journal of Electronics and Communications*, vol. 82, pp. 226-240, 2017/12/01/ 2017.