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High-Voltage 12.5-V Backside-Illuminated CMOS Photovoltaic Mini-Modules

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ABSTRACT In this paper, we employed a one-step localized substrate removal (LSR) process to fabricate a backside-illuminated CMOS photovoltaic (PV) mini-module suitable for high-voltage and low-power applications. LSR can be considered an upgrade of multichip module technology, by providing a 50-μm physical gap between on-chip PV cells for electrical isolation, while avoiding the need for time-consuming pick-and-place steps. A proof-of-concept PV module achieved open-circuit voltage of 12.5-V and μA-scale short-circuit current within a small form factor (3.13 V/mm^2). The fabrication of this PV mini-module is based on standard microelectronics manufacturing/packaging processes, thereby ensuring easy integration with other microelectronics for self-powered systems.

INDEX TERMS Complementary metal-oxide-semiconductor (CMOS), backside-illuminated photovoltaic device, localized substrate removal, micro-electromechanical systems (MEMS) process.

I. INTRODUCTION

Recent advances in circuit design and complementary metal-oxide-semiconductor (CMOS) technology have greatly reduced the size and power consumption of autonomous sensor nodes and implantable medical devices [1]–[3], thereby opening the door to the development of self-powered systems. The production of electricity from light using silicon-based photovoltaic devices (PVs) is viewed as a promising alternative to batteries, but only 0.5 V output voltage generated by a silicon PV is not sufficient to drive transistors, which typically require a driving voltage of 1.2V or higher. In addition, driving the micro-electro-mechanical system (MEMS) electrostatic actuators implemented by a foundry CMOS process typically requires a high-voltage power supply (>10V) and low activation current (>1μA) [4], [5]. This issue has been overcome by implementing a CMOS PV connected to a dc/dc voltage booster circuit to increase the dc voltage of the PV to a desired level by inserting as many voltage doublers as required [6]. Unfortunately, the efficiency of voltage booster circuits depends largely on the intensity of illumination reaching the PV cells [3], [6]. In contrast, a miniature PV array can function as a dc/dc step-up converter without the need for a conventional charge pump or switching converters, thereby avoiding the use of switched-capacitor high frequency circuits or bulk inductors. The fact that PVs are connected serially allows for the scaling up of array voltage to levels suitable for low-power MEMS actuation [7], [8]. Unfortunately, stacking on-chip CMOS PVs in series is not a straightforward solution, due to the common ground associated with the sharing of the same bulk substrate [9]–[11]. Multichip module (MCM) technology can be one solution to serially connecting a large number of individual CMOS PVs via microelectronic packaging [12]; however, this approach is time-consuming and highly inefficient, particular in the fabrication of very-high-voltage PV mini-arrays that require the assembly of tens or even hundreds of PV dies. We recently presented a proof-of-concept of a localized substrate removal (LSR) process to enable the electrical isolation and serial connection of four on-chip PV cells generating output voltage of 2.05V [13]. In this study, we developed a high-voltage (up to 12.5V) backside-illuminated (BSI) CMOS PV mini-module by cascading 25 on-chip BSI-PV cells in series via one-step LSR. This made it possible to avoid the time-consuming pick-and-place steps required for MCM. Fabrication of the proposed CMOS PV module is compatible with standard microelectronics manufacturing and packaging processes, which means

that it could easily be integrated with other microelectronic components for the manufacture of self-powered systems.

II. DESIGN AND EXPERIMENTS

The design of the CMOS BSI-PV chip is based on the standard TSMC 0.18-μm bulk CMOS configuration, whereas the design of integrated passive device (IPD) submount is based on standard AFSC TIPD passive-only technology. The bulk CMOS process was developed for logic and mixed signal circuits, whereas the low-cost IPD platform was developed for wireless communication systems and RF applications. Nonetheless, we adopted bulk CMOS processing for the fabrication of BSI-PV chips and the IPD platform for the serial connection of on-chip PV cells to enable the generation of higher voltages. During chip layout, we employed interdigitated doping patterns to create "electrically-uniform" n-well/p-sub diodes in order to enlarge the total junction area used to generate photocurrent from the substrate. Single PV cells were formed by connecting multiple unit p-n cells in parallel. The upper metal layers of each unit cell are cross-connected to the lower metal layers of adjacent unit p-n cells using multiple vias to achieve uniform series resistance independent of PV size. The anode and cathode of the PV cells are routed to the opposite sides of the chip to simplify packaging and device characterization. The final chip layout comprises 25 PV cells monolithically implemented on the same bulk substrate.

Fig. 1 illustrates the post-CMOS processing used in the fabrication of the proposed CMOS PV mini-module. The LSR method includes post-MEMS etching, flip-chip bonding, and substrate thinning to ensure on-chip electrical isolation. Following fabrication in a CMOS foundry, the PV chips underwent post-micromachining treatment, which involved anisotropic dielectric dry etching followed by isotropic silicon dry etching. Our aim was to create localized air cavities beneath the field oxide. The processed PV chip was then flip-chip bonded to an IPD submount using Au stub bumps as a bonding material. Finally, the CMOS chips were thinned via mechanical grinding and polished until the air trenches were exposed. The resulting CMOS PV mini-modules were sent to a four-point probe station to measure the light current-voltage (I-V) characteristics under exposure to a 980-nm laser source. The Gaussian laser beam profile was converted to a 5×5 mm^2 top-hat beam spot with equal energy distribution (intensity variation of less than 10%) using a beam shaping lens set. The size of the CMOS PV mini-module is 3.9×3.9 mm^2, with the PV chip occupying an area of 2×2 mm^2. The PV chip comprises 25 PV cells, each of which occupies an area of 0.3×0.3 mm^2, in which the active PV p-n junction covers an area of only 0.1×0.1 mm^2. Thus, the ratio of PV active area to the total chip area is 6.25%. Figs. 2(a), 2(b), and 2(c) respectively present microscopic views of the as-realized CMOS PV chip, IPD submount, and the resulting CMOS PV mini-module. The close-up scanning emission microscopic (SEM) image of the PV mini-module

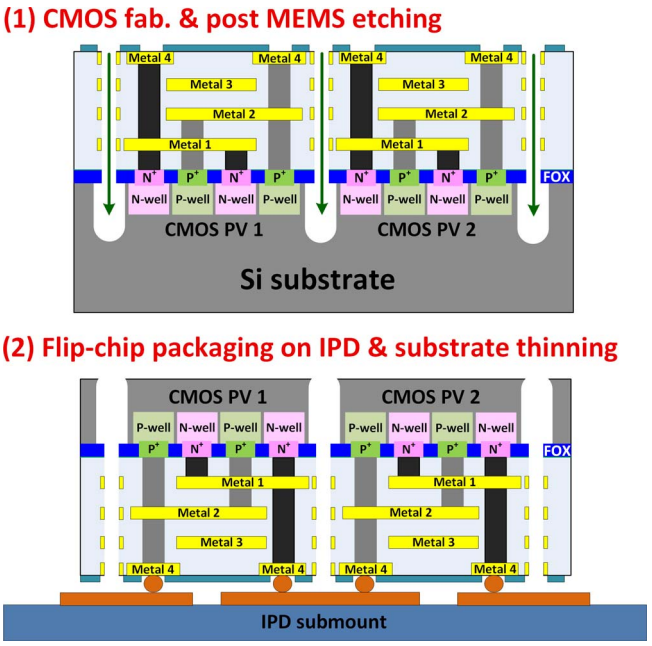

FIGURE 1. Localized substrate removal procedure to electrically isolate on-chip PV cells with one-step LSR process.

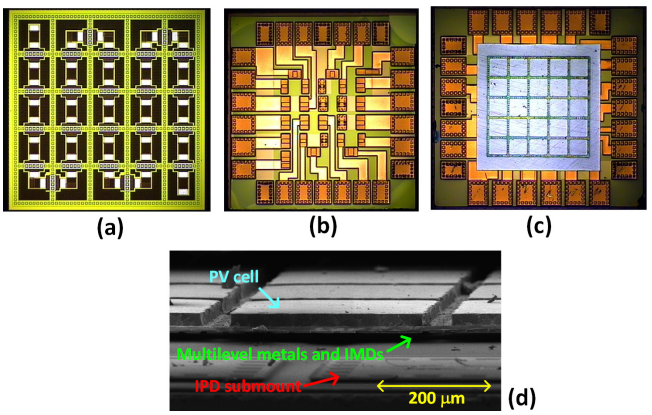

FIGURE 2. Top microscopic views of (a) CMOS PV chip, (b) IPD submount, and (c) assembled high-voltage CMOS PV mini-module. (d) Cross-sectional SEM view of CMOS PV mini-module with electrically isolated PV cells after LSR.

in Fig. 2(d) shows that all of the PV cells are separated physically by the air trenches. Nonetheless, the PV cells remain connected to each other through the multilevel metals and intermediate dielectrics (IMDs). The depth of the LSR-produced air trenches (approximately 30 μm) determines the substrate thickness in the resulting PV cells.

III. RESULTS AND DISCUSSION

Fig. 3(a) presents the current-voltage characteristics of the CMOS PV mini-module under 6 mW/mm^2 illumination. This PV mini-module allows an adjustable open-circuit voltage from 0.5 to 12.5 V by probing different electrode pads on the IPD to select the number of PV cells to be serially connected, while maintaining the short-circuit current at a nearly constant level (11∼12 μA under 6 mW/mm^2 illumination).

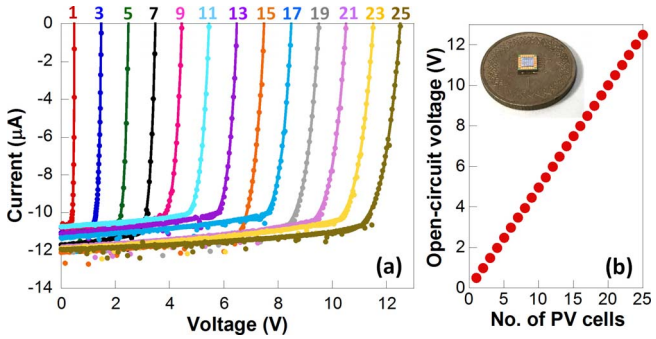

FIGURE 3. Characteristics of the CMOS PV mini-module in which PV cells are serially-connected: (a) Measured current-voltage characteristics of CMOS PV mini- module under 6 mW/mm^2 illumination. The inset values indicate the number of PV cells to be serially connected during the measurements. (b) Measured open-circuit voltage versus the number of serially-connected PV cells.

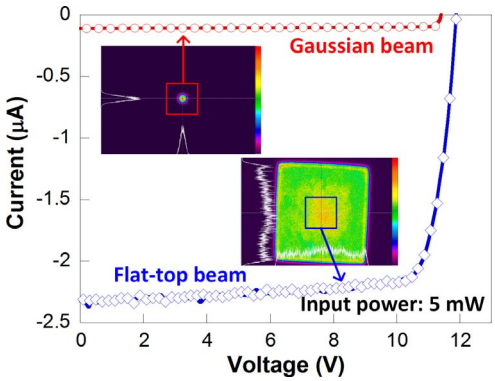

FIGURE 5. Measured current-voltage characteristics of CMOS PV mini-module illuminated by a laser beam with Gaussian and flat-top intensity distribution, respectively.

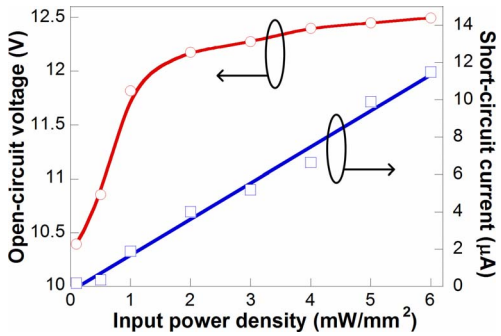

FIGURE 4. Measured (a) open-circuit voltage and (b) short-circuit current of CMOS PV mini-module (25 PV cells cascaded) under various input power densities.

The fill factors of 25 isolated PV cells range from 78% to 86% while the fill factor of the resulting PV mini-module is about 80%. This is slightly lower than the fill factor we had achieved in previous study [13]. Such a fill factor degradation may be attributed to the in-foundry diode performance variation and/or the surface defects produced during silicon etching and substrate thinning in LSR to enable electrical isolation. Fig. 3(b) shows a linear trend (~0.5V/cell) between the open-circuit voltage and the number of serially-connected PV cells, demonstrating the efficacy of using LSR for voltage boosting in CMOS on-chip PV cells. The inset of Fig. 3(b) illustrates the compactness of the as-realized CMOS PV mini-module. As shown in Fig. 4, the PV mini-module is able to provide > 10V open-circuit voltage even in a low-light environment (0.1 mW/mm^2), with a linear increase in μA-scale short-circuit current with illumination intensity.

The practical implementation of high-voltage PV mini-modules requires uniformity in the illumination intensity distribution, due to the fact that the amount of photocurrent generated by the PV cell is limited by the smallest current on any one of the PV cells linked in series. This would not be a critical issue in cases where the PV module is exposed to sunlight; however, it could impose difficulties in dealing with the Gaussian intensity distribution of laser beams. This issue limits the applications of the proposed CMOS PV mini-modules using laser as the energy source [2]. As shown in Fig. 5, a focused Gaussian laser beam with a beam size of 2.25 mm^2 (smaller than the size of CMOS PV chip) degrades the photocurrent generated by the PV array, resulting in a decrease in the short-circuit current from 2.32 μA to only 0.1 μA under 5-mW illumination. This was accompanied by a corresponding drop in open-circuit voltage drop from 11.89 V to 11.43V. One solution to the issue of partial-shading would be to employ a bypass diode running in reverse parallel to the PV cell. In this arrangement, the bypass diode is block when all PV cells were illuminated, and conducts when one or several cells are shadowed. Table 1 presents a performance comparison of high-voltage PV modules reported in the literature. Here, we define the specific open-circuit voltage $<V_{oc}>$ as the ratio of V_{oc} to the area of the PV chip. Despite the success in using the μ-cell pattern/assembly in high-voltage PV modules ($<V_{oc}>$ of approximately 2.5 V/mm^2), this approach tends to be highly complex, expensive, and incompatible with low-cost bulk CMOS processes. The MCM approach adopted from IC pick-and-place packaging is compatible with low-cost bulk CMOS processes; however, this approach is restricted by its ~300 μm PV cell separation requirement, which limits the $<V_{oc}>$ to only 0.64 V/mm^2. The proposed bulk-CMOS compatible LSR approach releases this constraint by leveraging the CMOS back-end process to define air trenches for on-chip electrical isolation, thereby reducing PV cell separation to only 50 μm. This greatly increases the density of PV cells in the module, resulting in a $<V_{oc}>$ of 3.13 V/mm^2. The ultimate efficiency of the PV mini-module is only 0.5%, because the PV active area covers only a small portion of the overall chip area (~6.25%). The intrinsic efficiency (in which only the PV active area is taken into account) is approximately 8.1%. Further improvements in the efficiency of the PV module could be achieved by increasing the active area on the PV cell. This could be achieved by reducing

TABLE 1. Comparison of high-voltage photovoltaic modules.

Reference	[7]	[8]	[12]	[13]	This work
Process	μ-cell pattern/assembly		MCM	bulk CMOS & post LSR	
Substrate	SOI	c-Si	c-Si	c-Si	c-Si
Interconnect Scheme	On-chip metal patterns		External submount	Multilevel metals External IPD submount	
Stacking	169	512	9	4	25
PV Chip area (mm^2)	42.25	59.85	7.84	8.91	4
V_{oc} (V)	103	155	5.05	2.05	12.5
$<V_{oc}>$ (V/mm^2)	2.44	2.59	0.64	0.23	3.13

the separation among PV cells, and/or employing a thicker PV (from 30 to 150 μm). The combination of light trapping structures in such a thin PV array will also help in improving its photocurrent generation.

IV. CONCLUSION

This paper presents a high-voltage CMOS PV mini-module fabricated using a one-step LSR process. The proposed PV mini-module features adjustable (0.5 to 12.5V) open-circuit voltage and μA-scale short-circuit current in a small form factor with a specific open-circuit voltage $<V_{oc}>$ of 3.13 V/mm^2. Only 25 on-chip PV cells were serially connected in our proof-of-concept demonstration; however, the proposed LSR approach could be used to connect a large number of PV cells on a single chip in order to boost the output voltage without the need for additional processing steps or sacrificing device performance.

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