A Fully Integrated CMOS Low Noise Amplifier for IEEE 802.11a Standard Applications

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Abstract: *In this paper, a fully integrated CMOS low noise amplifier (LNA) with on-chip spiral inductors in 0.18µm CMOS technology for IEEE 802.11a applications is presented. Using cascode topology and modified input impedance network as well as inductor neutralization technique, the LNA power dissipation is lowered to 15.8mW while having power gain of 17.82dB and reverse isolation factor of -58.37dB at centre frequency of 5.5GHz. S_{11} and S_{22} are equal to -16.1dB and -32dB, respectively. Designed LNA has IIP3 of +3dBm and less than 2.9dB noise figure (NF) in working band width, as resulted from transistor level simulation using TSMC RF CMOS 0.18 µm design kit.*

Keywords: RF CMOS LNA, Low noise amplifier, RF front-end, Ultra Wide Band (UWB), inductive neutralization.

1. Introduction

The ascending demand for high performance, low cost and integrated wideband radio frequency (RF) receivers for portable wireless communication systems like Cellular phones, Mobile TV, Blue-tooth, Wireless Local Area Network (WLAN), Wireless Personal Area Network (WPAN) and devices like Pagers, RF identification systems and Cordless phones has considerably increased investments and researches in RF micro-electronics industries. The most important standards for Ultra Wide Band (UWB) wireless systems are IEEE standards like 802.11 for WLAN, 802.15 for WPAN, 802.18 for radio regulatory technical advisory group and etc. Each has different revisions for distinctive purpose such as IEEE 802.11a/b/g and n. There are two different technologies for UWB systems implementation: 1) DS-UWB 2) Multi-band OFDM. MB-OFDM UWB is consist of 5 major band groups, each subdivided into 3, 528MHz bands except last band group which has 2, 528MHz bands. Fig.1 shows the band groups of OFDM based on FCC definition.[1-4]

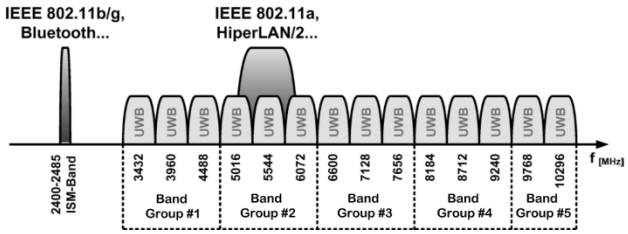

Fig.1: Frequency allocation of MB-OFDM UWB channels [4].

The second band group is consist of, the bands #4, #5 and #6, which extends from 4.752 ~ 5.280 GHz, 5.280 ~ 5.808 GHz, and 5.808 GHz ~ 6.366 GHz respectively, which covers frequency ranges from 4.75 to 6.36 GHz with related centre frequency as depicted in Fig.1[2].

IEEE 802.11 was the first WLAN standard with data transmission rate of 2Mbps. To increase the data transmission rate, the new generations of WLAN standards 802.11a WLAN and HiperLAN/2 are defined which evolved from 2.4GHz to 5GHz spectrum using OFDM technology. The advantages of these standards are higher data rate, greater system capacity, low interference and less congestion [5-6]. Fig.2 demonstrates set of valid operating channels for WLAN 802.11a [6].

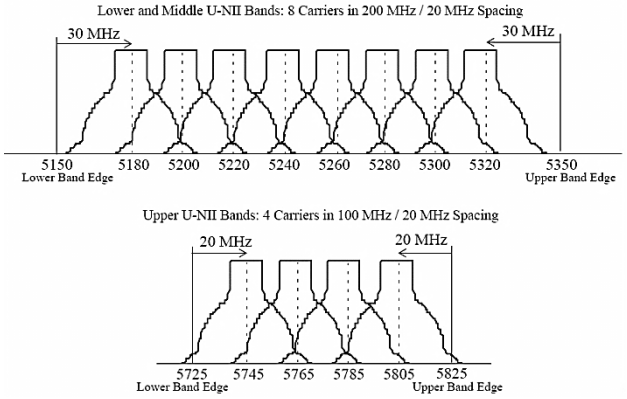

Fig.2: OFDM PHY frequency channel plan for the US [6].

In the RF receiver front-end circuits, noise performance is mainly determined by the first gain stage amplifier (LNA), so that its noise figure has direct effect on whole system noise sensitivity [1,3]. This paper describes a CMOS low noise amplifier, designed for IEEE 802.11a standard, from 5GHz to 6GHz, which is simulated in ADS by TSMC RF CMOS 0.18µm design kit with 1.8v power supply. Inductor neutralization technique is used to increase stability and reverse isolation of LNA. Also, a modified input matching network is represented which has better performance compared to reference [7].

2. Designing Process

Table I illustrates acceptable values for the performance parameters of LNAs which are used in heterodyne receivers. Balancing between the parameters mentioned on the table, in one hand and power consumption and supply voltage on the other hand is a major challenging on an optimal LNA design procedure [3]. The first step in LNA design practice, based on application, is topology selection and suitable transistors' dimensions determination. Fig.3 shows the chosen LNA topology. A cascode circuit is chosen due to its suitable reverse isolation and bandwidth to respond our requirements and application.

The circuit uses a bias current of 8.68mA for main core and 95.1uA for bias transistors to provide sufficient voltage for M_1. Therefore, Total power consumption is 15.8mW with power supply of 1.8v. M_1 and M_2 have 3 µm width with length of 0.18 µm and 64 fingers.

TABLE I: Typical LNA characteristics in hetero-dyne systems. [3]

NF	2dB
IIP3	> -10dBm
Gain	> 15dB
Input and output impedance	50 Ohm
Input and output return loss	< -15dB
Reverse isolation	> 20dB
Stability Factor	> 1

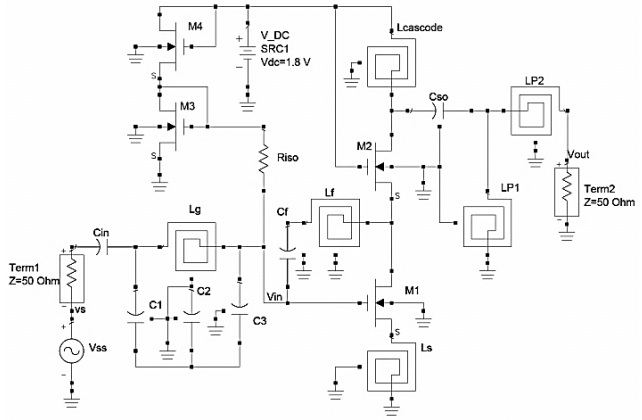

Fig.3: Designed and simulated LNA structure.

R_{iso} is used to reduce the effect of C_{gs} of M_3 and supply gate of M_1 while isolating M_3 from input signal. R_{iso} set to 16Kohm by P+ poly silicide because lower resistance causes to noise figure increment, meanwhile it provides other above considerations.

2.1. Input / Output Resonance

The second step is L_g designing from "Equation (1)" to adjust input resonance frequency. Because a high voltage gain is needed, source inductor of M1, L_s , is not used.

Afterwards, in the third step, output resonance circuit must be designed in the presence of load without related matching network. It is calculated using "Equation (2)".

$$\omega_o = \sqrt{\frac{1}{L_g C_{gs1}}} \tag{1}$$

$$\omega_o = \sqrt{\frac{1}{L_{cascode}(C_{gd2} + C_L)}} \tag{2}$$

where C_L indicates parasitic capacitances in output.

2.2. L_f Effect in Stability and Reverse Isolation (S_{12})

An LNA design that is nominally stable may oscillate at the extremes of manufacturing variations and perhaps at unexpectedly high or low frequencies. The stability of circuits is distinguished by "Stern stability factor" proposed in reference [3]:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2S_{12}S_{21}} \tag{3}$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$, If $K > 1$ and $\Delta < 1$, then the circuit is unconditionally stable [3].

As the effect of gate-drain overlap capacitance (C_{gd}) is comparable with the gate-source capacitance (C_{gs}) in submicron CMOS technologies, it cannot be neglected in Designing RF CMOS amplifiers. It is greatly responsible for the reduction of forward gain, isolation, and the operating frequency of the LNA [8]. Reference [1] proposed different techniques for reducing the effect of this capacitor, and in this work inductor neutralization is used.

Here, at the forth step, a suitable L_f is designed to increase circuit stability and reverse isolation by cancelling effect of C_{gd1}. Presence of L_f will affect input resonance frequency, Z_{11} and Z_{22}, so it needs re-optimizing. Fig.4 and Fig.5 shows the effect of L_f on circuit stability and reverse isolation, respectively, with output and input impedance matching. Presence of L_f has very little effect on NF as it can be neglected. C_f and L_f are obtained 951.9fF and 3.603nH, respectively.

2.3. Output Impedance Matching

The fifth step is output impedance matching circuit for achieving suitable Z_{22} and S_{22}. Smith chart method is used to design the relative matching network at desire frequency. The designed values of the Lp1 and Lp2 inductors are 14.4nH and 4.9nH, respectively, but on the transistor level optimization, Lp1 and Lp2 are 4.517nH and 1.581nH, respectively, which are differ from ideal values.

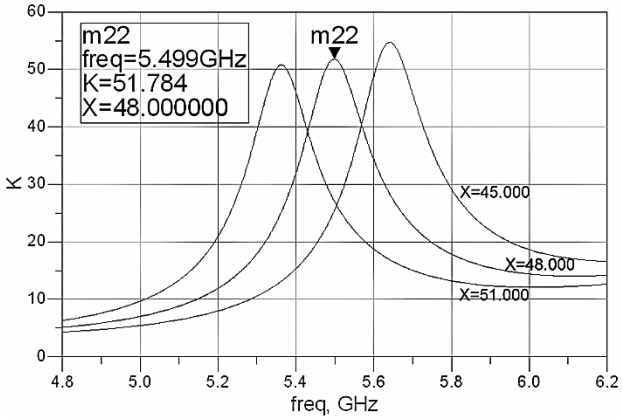

Fig.4:L_f effect on LNA stability factor (K).

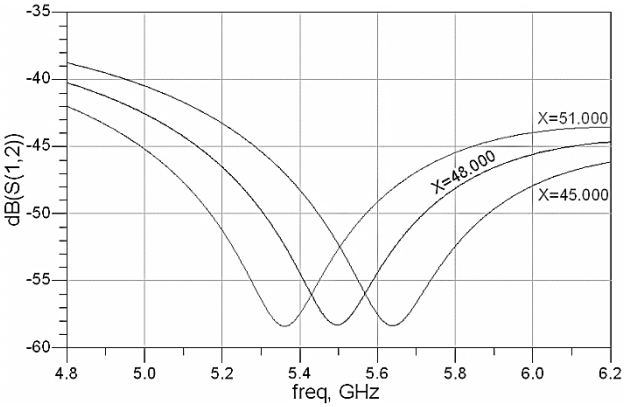

Fig.5:L_f effect on Reverse isolation of the LNA (S12).

2.4. Input Impedance Matching

Because any designing mistake causes to degrade NF and gain, input matching designing is very sensitive. In this design there is no difference between output and input matching network designing priority because, presence of L_f approximately isolate any affection of cascade inductor on input impedance. There are several methods to adjust the input impedance of the amplifier [7,9]. Reference [7] proposed a modified input matching for improving input matching. In this paper, that method is used with further modification. A "T capacitive network" is used in parallel with L_g, as depicted in Fig.6. In the restricted range, C_1 impress both $Im(Z_{11})$ and $Re(Z_{11})$, and C_3 controls $Im(Z_{11})$ and a bit $Re(Z_{11})$ in such a way, decreasing C_1 will decrease Z_{11} and decreasing C_3 will decrease $Im(Z_{11})$.

Presence of Ls will increase $Re(Z_{11})$, IIP3, and linearity, and will decrease noise figure of amplifier, input resonance frequency, and circuit gain. Nevertheless, it does not effect on $Im(Z_{11})$, especially when we use L_f due to neutralization of C_{gd} [??2]. The advantage of this technique is lower NF and, independent control for $Im(Z_{11})$ by C_3 and $Re(Z_{11})$ by L_s. Thus, after using these techniques it needs re-optimizing for achieving our final circuit. Determination of the exact elements values need trial and error method due to correlations between different parameters and parasitic effects that changes values calculated before. Both output and input impedance matching networks are designed in such a way for obtaining maximum power amplification, not for maximum voltage gain or minimum noise figure.

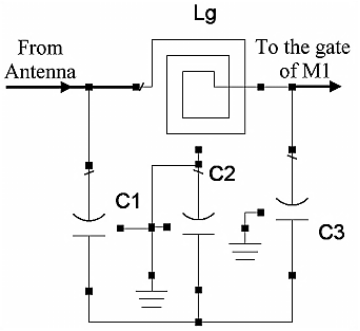

Fig.6: Modified input matching network.

2.5. Noise Figure

The NF of the presented LNA is 2.3dB, 2.475dB and 2.9dB at frequency of 5GHz, 5.5GHz and 6GHz, respectively, as presented in Fig.7. The degeneration inductor loss resistance in the transistor M1 source can affect NF, [10]. NF is reduced in presence of L_s.

2.6. Linearity

Input 1-dB compression point (1dB-CP) in this work is -15.12dBm achieved by "gain compression test" which is presented in Fig.8. Output and input third order interception points (OIP3 and IIP3) of current LNA are 14.805dBm and 3.04dBm, respectively, which achieved by "two-tone test" and are illustrated in Fig.9.

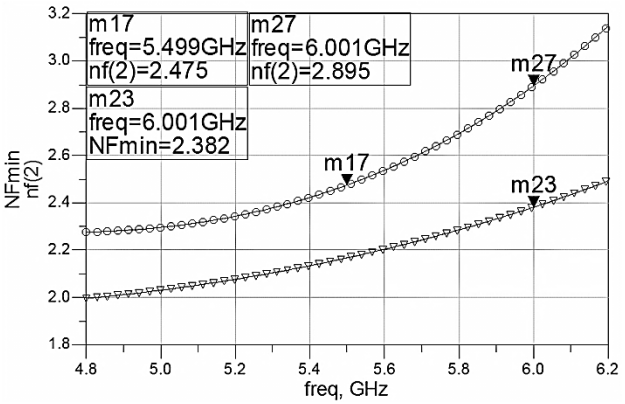

Fig.7: Noise figure.

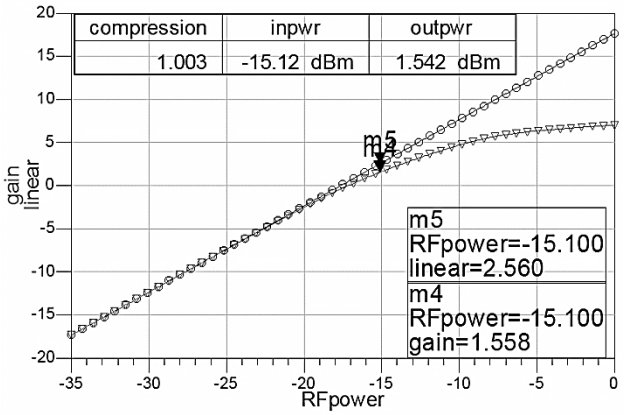

Fig.8: 1dB-compression point of the LNA.

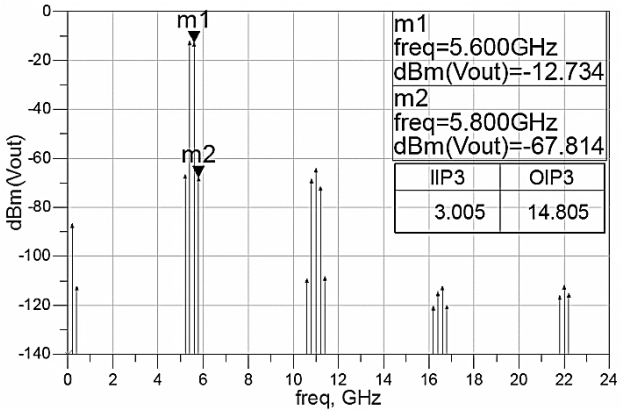

Fig.9: Third order interception point of the LNA.

TABLE II: Simulation results of designed LNA and other published works.

Ref.	S11 (dB)	S12 (dB)	S21 (dB)	S22 (dB)	Vdd (V)	Pdc (mW)	NF (dB)	Fc (GHz)	3dB-BW (MHz)	IIP3 (dBm)	Tech. CMOS(µm)	Year
[11]	-11.7	-30	13	-14	1.2	9.7	2.7	5.5	1000	-	0.09	2004
[12]	-28	-33	11.2	-14	0.6	2.1	3.2	5.5	1000	-8.6	0.09	2004
[7]	-18.5	< -48	20.5	-21.3	1.8	2	1.8~2.6	5.5	1000	-6.2	0.18	2008
[13]	-20	-30	20	-20	1.5	15	3.5	5	-	-9	0.18	2004
[14]	-14 -10	- -	11.6 13.1	-17 -22	1.8 1.8	3.96 3.96	3.4 4.1	5.7 5.7	900 700	- -	0.18 0.18	2007 2007
[15]	-11.5 -12.3	-25.5 -26.4	14.4 16	-12.3 -11.9	3 3	24 48	2.8 2.5	5.25 5.25	840 840	-1.5 -1.5	0.25 0.25	2001 2001
[16]	-23.5	-30	8	-10.3	2	10	4.8	5.5	1000	-1.5	0.25	2002
[5], K=0.7	-17.3	-140	24.6	-5.3	0.7	6.125	5.48	5.745	130	-	0.25	2010
This design	-16.13	-42~-58.37	17.8	-32	1.8	15.8	2.3~2.9	5.5	1000	+3	0.18	

2.7. S-parameters and simulation results

The designed circuit is simulated with ADS in 0.18µm standard. S parameters and voltage gain are shown in Fig.10 and Fig.11, respectively. NF and stability factor are discussed before and are demonstrated before, in Fig.7 and Fig.4, respectively.

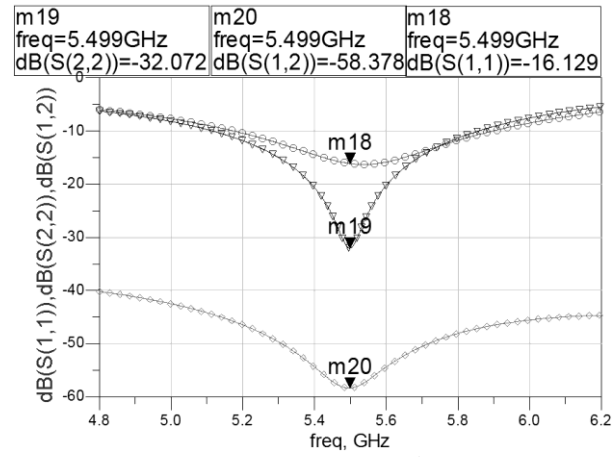

Fig.10: Simulated S-parameters of LNA.

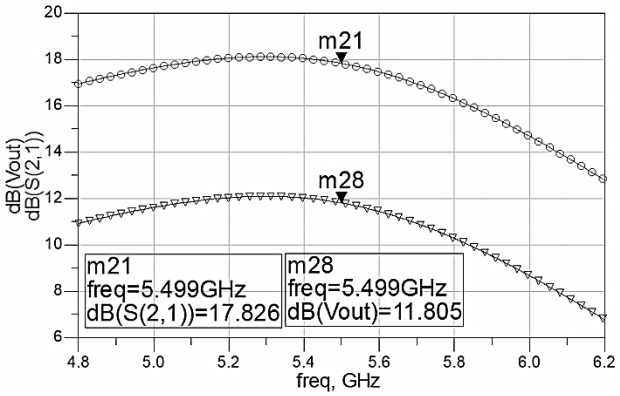

Fig.11: Voltage and power gain of LNA

3. Conclusion

A fully integrated CMOS LNA for IEEE 802.11a WLAN application is presented and simulated in standard 0.18µm by CMOS technology. Cited LNA has better balance and trade-off among all parameters such as S11, S22, S12, S21, K, NF. Stability and reverse isolation are improved while NF is kept low. For providing our requirements, input impedance matching network is also improved. This network has more degree of freedom, so designers can control real and image part of Z_{11} independently. The presented LNA is compared with other published works, and results are represented in Table II.

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