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Modified quadrant-based routing algorithm for 3D Torus Network-on-Chip architecture☆

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Summary Due to high performance demands of the consumer electronics and processing systems, like servers, the number of cores is increasing on System-on-Chip (SoC). Network-on-Chip (NoC) is suitable approach for reducing the communication bottleneck of multicore System-on-Chip. With the integration of 3D IC technology, the 3D Network-on-Chip design enhances the execution rate and decreases power utilisation by replacing long flat interconnects with short vertical ones. New compact architectures are possible by arranging the cores in three-dimensions. Optimised routing algorithms can provide higher execution speed along with reduced energy consumption. In this paper an efficient routing algorithm for 3D Torus topology architecture is proposed. A modified quadrant-based routing algorithm for 3D torus NoC architecture is proposed which is primarily based on division of space into different quadrants and also adopting a path which encounters least hops to connect to the destination node. The proposed algorithm is compared with other 3D routing algorithms like XYZ dimension order routing and the simulated results shows that the proposed algorithm has least latency.

Introduction

As the number of cores is increasing to meet the high performance requirement of the Multiprocessor System-on-Chip (SoC), the Network-on-Chip (NoC) offered a scalable and alternative method for communication in place of bus based system which had limitation of the bandwidth and more power consuming (Dally and Towles, 2004). However, as number of cores increases on the chip, three-dimensional (3D) Network-on-Chip provides an attractive option to reduce the long flat interconnect with the short vertical one with the advantage of high throughput, low latency and low power consumption. With the 3D integration many heterogeneous circuits can be stacked vertically and can

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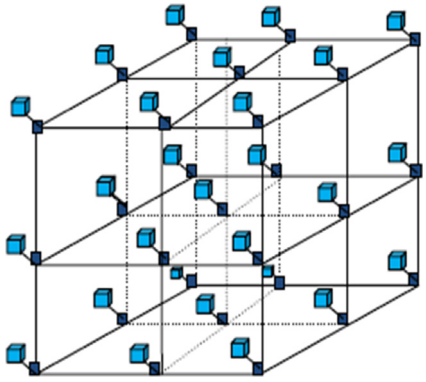

Figure 1 3D Mesh topology.

be connected by using through-silicon-vias (TSVs) (Cilardo and Fusella, 2016). TSVs provide the communication links between different layers. Because of very short and fine links they provide low delay, low power and high bandwidth communication channel. The cost of designing TSV is high and also very complex process with poor yields and defects. Instead of using TSV for all inter layer nodes, which causes significant area overhead and cost, a combination of 2D and 3D router with few TSV can be utilised (Chen et al., 2015).

The topology decides the physical architecture of the interconnection network. The most common topologies are mesh, torus, ring etc. for both 2D and 3D NoCs (Ansari et al., 2015a). 3D Mesh topology is shown in Fig. 1.

The performance of the 3D NoC can be significantly affected by the routing algorithm (Chen et al., 2015). Therefore, it is always challenging to design optimum routing algorithm for the given topology. Routing algorithms should be designed to give low latency and high throughput with

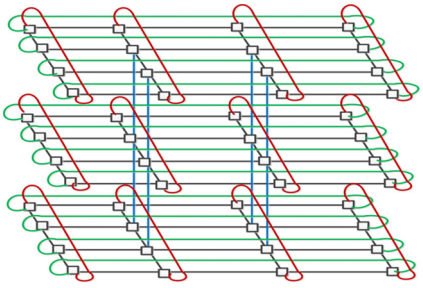

Figure 2 3D Torus topology (proposed).

no congestion and deadlock along with fault tolerant ability (Ansari et al., 2015b). Various routing algorithms were proposed for the 3D NoCs like Ebrahimi et al. (2014) given algorithm for 3-D mesh based NoCs to distribute the unicast and multicast traffic. Khan and Ansari (2011a) presented an efficient routing algorithm Quadrant-based XYZ DOR for 3D Asymmetric Torus. Khan and Ansari (2011b) presented a routing algorithm based on binary search tree (BST) for the topology based on modified binary tree.

The contribution of present work consists of proposing an algorithm for the 3D Asymmetric torus with reduced vertical links. A modified quadrant-based routing algorithm for 3D torus NoC architecture is based on first dividing the space into different quadrants and then adopting the path which gives least hops to connect to the destination node. Topology for the proposed algorithm is shown in Fig. 2.

Proposed 3D NoC routing algorithm

Most important thing in the NoC design is its topology and routing algorithm. Sending packets from Source node (S) to

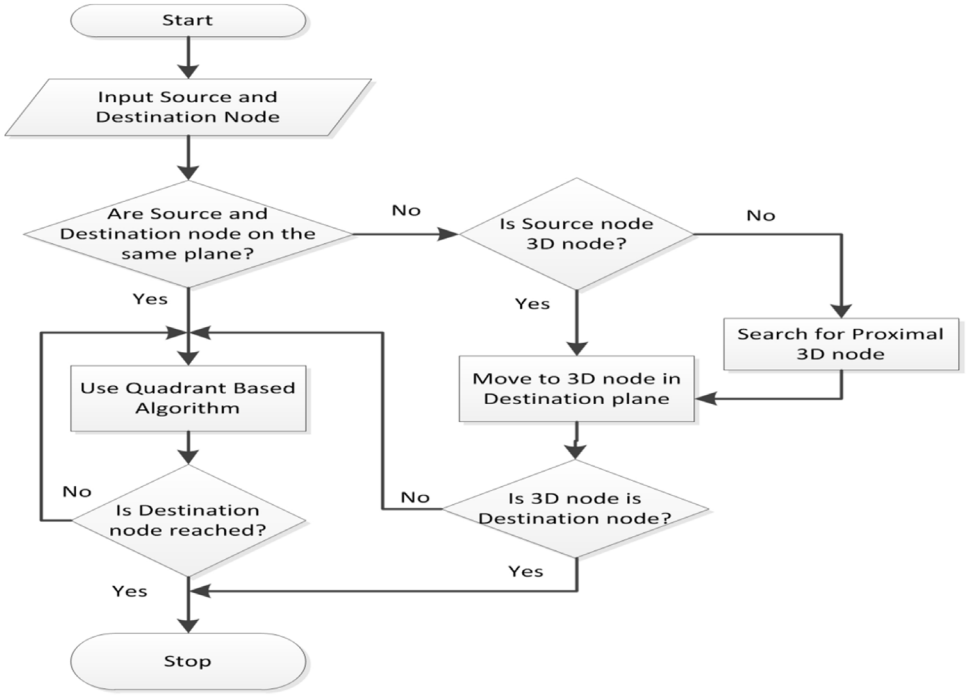

Figure 3 Proposed routing algorithm.

the Destination node (D) efficiently from various available paths without any congestion or fault with low cost is the main goal of the routing algorithm.

Quadrant-based algorithm

In this algorithm the whole node plane is divided into four quadrants and then checks the two basic queries:

(a) Are quadrants of S and D are different?
(b) Is the difference between S and D node are greater than the centre of the plane?

If the both (a) and (b) are correct then the nearest wrap around edge to S is used by applying quadrant based algorithm.

Proposed algorithm

The above algorithm considers each layers node are vertically connected with the node below or above layer by link using the 3D routers via TSVs. But this is not the actual case, because of the high cost and area overheads only few vertical links are available. In the proposed algorithm the packet is sent to the destination layer first and then the quadrant-based algorithm is implemented. The flow chart for the proposed algorithm is shown in Fig. 3.

Modified Quadrant-based Algorithm

// Input destination node $D(x_d , y_d, z_d)$ and source node $S(x_s , y_s, z_s)$
If $S(x_s , y_s , z_s)$ has TSV then
{ If $x_s = x_d$ and $y_s = y_d$ then
Start routing to upper or lower layer
Else use quadrant based algorithm}
Else
Find the nearest TSV or 3D node and use quadrant based algorithm
// quadrant based algorithm in x and y plane
Min = 0; Max = n – 1 //No. of nodes in plane is n
$\Delta x = x_d - x_s$ //difference in S and D in x-plane
$\Delta y = y_d - y_s$ //difference in S and D in y-plane
$X_0 = [nx/2]$, $Y_0 = [ny/2]$ //centre of the plane
x_n and y_n // next node to hop
//first route packets in X-plane
while ($\Delta x! = 0$) //routing in X-plane
{// observe the closest wrap-around edge in X-plane as destination is in the subsequently quadrant
If (($\Delta x \in X_0$, Max] || $\Delta x \in [-Max, -X_0)$)
If ($\Delta x > 0$)
$x_n = x_s - 1$ //move to next node along in the West(W) direction
Else
$x_n = x_s + 1$ // move to next node along in East(E) direction
Else //do X-routing
If ($\Delta x > 0$)
$x_n = x_s + 1$ // move to next node along in E direction
Else
$x_n = x_s - 1$ // move to next node in W direction
$x_s = x_n$ //change next node as current node
$\Delta x = x_d - x_s$ //re-compute Δx from new Source
}
//Similarly do the routing in y-plane till destination is reached

Table 1 Performance comparison of the proposed algorithm.

Parameters/algorithm	Proposed	XYZ DOR	Quad-based
Average delay	0.60 ns	0.80 ns	0.65 ns
No. of hops	7	11	8

Implementation

The proposed algorithm is written in Verilog Register Transfer Logic (RTL). The circuit designed for the algorithm takes input as the network size, input node and destination node give results as the path to be taken for the packet to reach destination. The synthesis of the proposed algorithm is achieved on the Xilinx Virtex-5 XC5VLX110 T FPGA kit, manufactured by DIGILENT. It is found that the proposed algorithm for $4 \times 4 \times 3$ Torus architecture produce better performance as compared to XYZ algorithm and quadrant-based algorithm as shown in Table 1.

Conclusion and future work

In the present work a modified quadrant-based routing algorithm for 3D torus NoC architecture is proposed. With the proposed algorithm packet is sent from the source to destination with less latency. With the less number of vertical links or TSVs the hardware requirement is reduced in this case with better performance. As extension to current work in future, it is planned to accommodate the faults and congestion in routing algorithm and also explore the power analysis.

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