*Research Article*

# A New CMOS Controllable Impedance Multiplier with Large Multiplication Factor

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This paper presents a new compact controllable impedance multiplier using CMOS technology. The design is based on the use of the translinear principle using MOSFETs in subthreshold region. The value of the impedance will be controlled using the bias currents only. The impedance can be scaled up and down as required. The functionality of the proposed design was confirmed by simulation using BSIM3V3 MOS model in Tanner Tspice 0.18 $\mu$m TSMC CMOS process technology. Simulation results indicate that the proposed design is functioning properly with a tunable multiplication factor from 0.1- to 100-fold. Applications of the proposed multiplier in the design of low pass and high pass filters are also included.

## 1. Introduction

A capacitance multiplier circuit is a useful building block in many very large-scale integration (VLSI) analog circuits, especially for active RC filter and oscillator designs and for cancellation of parasitic elements. Signal processing for biomedical applications is one of the areas where very low frequency filters are used [1–11]. In such a filter, a large time constant is required, which means large values capacitors and/or resistors are required. However, in integrated circuit design, implementing such a large time constant will not be acceptable due to a required large area on the chip and large power consumption. A more viable solution is to use small physical capacitor or resistor and it is scaled up using a simple circuit. There are many impedance-scaling circuits published in the open literature [2–9]. In [2, 3], an operational transconductance amplifier (OTA) based tunable $C$-multiplier is developed. The design is for capacitor scaling-up only and it uses three OTAs in which the multiplication factor is tuned using the OTAs' bias currents. An impedance scaler is presented in [4, 5] using MOSFETs. This would require a small area on the chip. However, the scaling factor is controlled by the aspect ratios of the transistors used. This means that, once fabricated, the scaling factor cannot be controlled. The design reported in [6] used three current-controlled current amplifiers in addition to an external

resistor. A universal immittance function simulator using a current conveyor is reported in [7]. In this design three CCIIs are used. Moreover, external resistors are used to control the multiplication factor. In [8] current conveyor based $R$- and $C$ multiplier circuits are developed. The values of $R$ and $C$ are controlled by two other resistors. In [9] an enhanced grounded capacitor multiplier is presented. The design is based on using the differential amplifier with exponential current scaling. In [10, 11] current conveyors and dual-$x$ current conveyors are used.

In this paper, a new impedance scaler is proposed. The design can scale up and down the capacitance and the resistance.

## 2. Proposed Impedance Multiplier

The block diagram of the proposed design is shown in Figure 1. It consists of a current amplifier, a voltage buffer, and the impedance to be scaled $Z$. With reference to Figure 1, the equivalent impedance seen by the voltage source $V_x$ is given by

$$Z_{\text{eq}} = \frac{V_x}{I_x} = \frac{V_x}{i_o}. \tag{1}$$
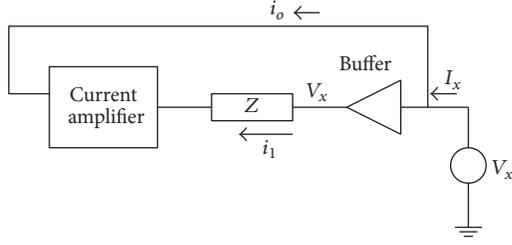
FIGURE 1: Block diagram of the proposed design.
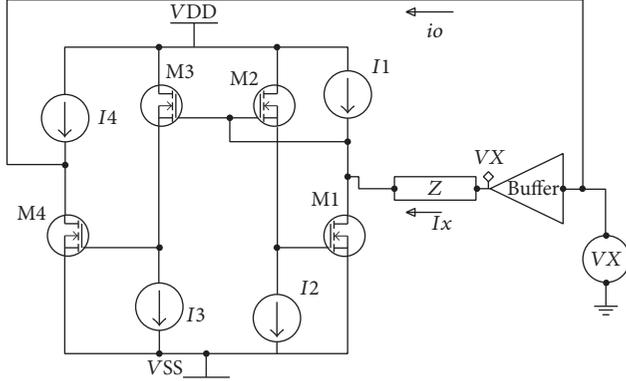


FIGURE 2: Circuit diagram of the proposed design.

The amplifier output is given by

$$i_0 = G \times i_1,\qquad(2)$$

where $G$ is the gain of the amplifier. If the input impedance of the current amplifier is small compared with $Z$, then the current $i_1$ passing through the impedance $Z$ can be approximated by

$$i_1 = \frac{V_x}{Z}.\qquad(3)$$

Combining (1), (2), and (3), the equivalent impedance is given by

$$Z_{\text{eq}} = \frac{Z}{G}.\qquad(4)$$

The circuit diagram of the proposed design is shown in Figure 2. Four MOSFETs M1–M4 form a translinear loop with regulated cascade input to lower the input impedance in series with $Z$. The MOSFETs are biased in the subthreshold region and this will provide high output impedance and hence enhance the lower corner frequency. All biased currents are designed using simple current mirrors. The buffer used is a two-MOSFET buffer and is shown in Figure 3.

With reference to Figure 2, applying KVL to the translinear loop yields

$$V_{\text{GS1}} + V_{\text{GS2}} = V_{\text{GS3}} + V_{\text{GS4}}.\qquad(5)$$
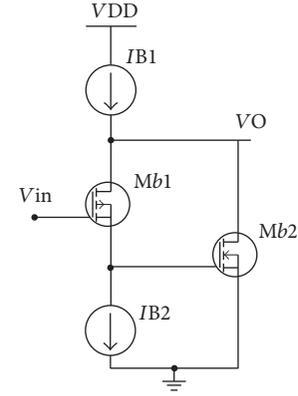


FIGURE 3: Circuit diagram for the buffer.

The drain current of an NMOS operating subthreshold is given by

$$I_D = I_{D0}e^{((V_{\text{GS}}-V_{\text{Th}})/nV_T)},\qquad(6)$$

where $I_{D0}$ is the saturation current, $n$ is the slop factor, and $V_T$ is the thermal voltage.

For the MOSFET to operate in subthreshold mode, the following condition must be satisfied:

$$\frac{I_{D0}}{I_D} \ll 1,$$

$$V_{\text{DS}} > 4V_T.\qquad(7)$$

From (6), the gate-to-source voltage is given by

$$V_{\text{GS}} = nV_T \ln\left(\frac{I_D}{I_{D0}}\right) - V_{\text{Th}}.\qquad(8)$$

Combining (5) and (8), it is easy to write

$$I_{D1}I_{D2} = I_{D3}I_{D4}.\qquad(9)$$

The equivalent impedance $Z_{\text{eq}}$ seen at terminal $x$ can be obtained if an AC voltage source is applied and the AC currents $i_1$ and $i_o$ are included in the analysis. Thus, (9) can be rewritten as

$$(i_{o+}I_4) * I_3 = I_2 * (I_1 + i_1)\qquad(10)$$

or

$$(i_{o+}I_4) = G * (I_1 + i_1),\qquad(11)$$

where $G = I_2/I_3$.

If $I_4 = G * I_1$, then $i_o = G * i_1$.

With reference to Figure 2, the impedance at node $x$ is given by

$$Z_{\text{eq}} = \frac{v_x}{i_x} = \frac{v_x}{i_o} = \frac{v_x}{Gi_1} = \frac{v_x}{i_1}\frac{1}{G}.\qquad(12)$$

Since $Z$ is much greater than the impedance at the drain of M1, then $v_x/i_1 \approx Z$, and (12) can be written as

$$Z_{\text{eq}} = Z\frac{1}{G}.\qquad(13)$$

TABLE 1: Performance comparison.

| | Technology ($\mu$m) | Multiplication factor | Power consumption | Area (mm$^2$) | Frequency range | Experimental/simulation |
|---|---|---|---|---|---|---|
| Ref [3] | 0.35 | 10 | NA | — | 400 Hz–70 KHz | Simulation |
| Ref [4] | | 10 | 10.8 mW | 0.0297 | NA | Simulation |
| Ref [9] | 0.50 | 28 | 1.32 mW | 0.07 | NA | Simulation & experimental |
| Ref [11] | 0.35 | 50 | 0.2 mW | NA | NA | Simulation |
| This work | 0.18 | Controllable 0.1–200 | 20 $\mu$W | 0.0030 | 10 Hz–7 KHz | Simulation |

It is evident from (13) that the circuit implements a tunable impedance scaler, which is tuned using the control parameter $G = I_2/I_3$. If $Z$ is replaced by a capacitor, then

$$Z_{eq} = \frac{1}{sC}\frac{1}{G}. \tag{14}$$

It is clear from (14) that a capacitance multiplier is achieved.

If $Z$ is replaced by a resistor, then

$$Z_{eq} = R\frac{1}{G}. \tag{15}$$

Equation (15) implements a tunable resistor that can be tuned by the control variable $G$. The resistor can be scaled up or down as required.

## 3. Simulation Results

The proposed circuit was simulated using Tanner Tspice in 0.18 $\mu$m TSMC CMOS technology and BSIM3v3 MOSFET model. To prove the concept, the circuit is configured as low pass filter with $R = 10\,\text{M}\Omega$ and the capacitance that can be scaled up and down is 5 pF. The transistors aspect ratio is 7/2 and the bias currents for the buffer are set to $I_{B1} = 1\,\mu\text{A}$ and $I_{B2} = 0.2\,\mu\text{A}$. The circuit is operated from $\pm0.75$ V. The bias currents $I_1 = I_3 = 5$ nA, the current $I_2 = I_4 = G * I_1$, and $G$ are swept from 0.1 to 100. Plots of the simulated result of the proposed design and the theory are shown in Figure 4.

It is evident from the plots that the proposed $c$-multiplier is working well. The 5 pF capacitor is scaled up to 500 pF and down to 0.5 pF.

As it appears from Figure 4 there is a deviation between ideal case and the proposed design. This deviation is due to the approximation made in (12) where we assume the input impedance at the node of M1 is much smaller than $Z$, in addition to the output impedance of the buffer circuit.

The proposed design can be used in the frequency range from 10 Hz to 7 KHz as shown in Figure 5.

The proposed circuit was simulated for transient analysis. An input signal of 100 mv amplitude and 5 KHz frequency was applied to the input of an ideal and simulated circuit. The output voltage for the ideal and simulated design is shown in Figure 6. It is clear that the proposed circuit is functioning properly.

The performance of the proposed design is compared with previously published works and is summarized in Table 1. It can be seen from the table the proposed design is superior to all in terms of controllability, area on chip, and frequency range, where the lower limit is 10 Hz, which make it attractive in very low frequency applications such as very low frequency filters.

## 4. Nonideal Analysis

The error shown in Figure 4 was investigated through the small signal analysis. The small signal equivalent circuit for Figure 1 is shown in Figure 7. The parasitic capacitance is not included because this design is suitable for low frequency applications.

Using routine analysis, the equivalent impedance seen at the node $V_X$ is given by

$$Z_{eq} = \frac{V_X}{i_X} = \frac{V_{d4}}{i_X}$$

$$= \frac{Z}{Zg_{ds4} + Zg_{m4}g_{m3}\left(2g_{m2b} + g_{m1b}g_{m2b}/g_{ds2b}\right)/\left(g_{ds3} + g_{m3}\right)/\left(Zg_{ds1} + 1 + Zg_{m1}g_{m2}/\left(g_{ds2} + g_{m2}\right)\right)\left(g_{ds1b} + 2g_{m2b} - g_{m1b} + g_{m1b}g_{m2b}/g_{ds2b}\right)}. \tag{16}$$

Comparing (16) with (13), the control variable $G$ is given by

$$G = Zg_{ds4} + \frac{Zg_{m4}g_{m3}\left(2g_{m2b} - g_{m1b}g_{m2b}/g_{ds2b}\right)/\left(g_{ds3} + g_{m3}\right)}{\left(Zg_{ds1} + 1 + Zg_{m1}g_{m2}/\left(g_{ds2} + g_{m2}\right)\right)\left(g_{ds1b} + 2g_{m2b} + g_{m1b} - g_{m1b}g_{m2b}/g_{ds2b}\right)}. \tag{17}$$
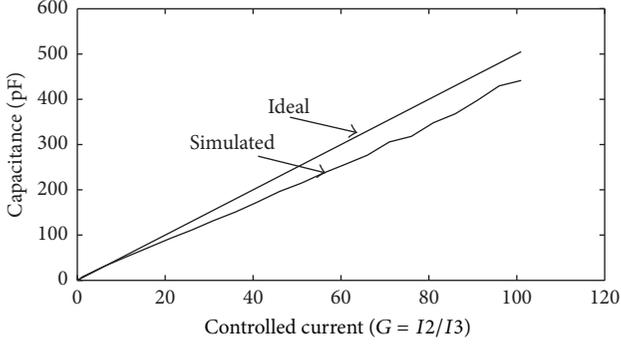
FIGURE 4: Plot of simulated capacitance and ideal case.
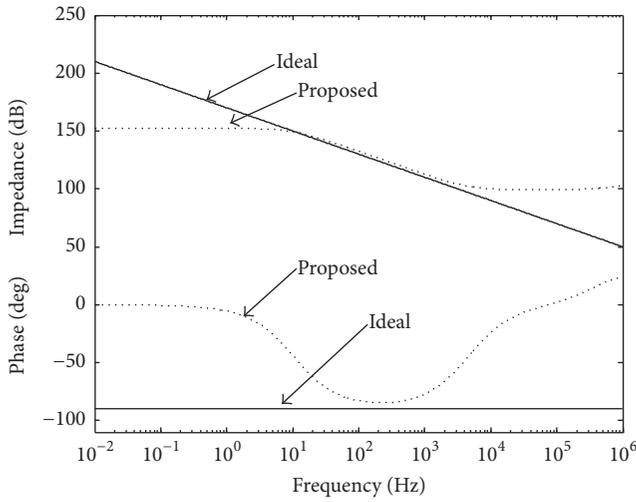


FIGURE 5: Compared impedance and phase for ideal and the proposed design.



FIGURE 6: Simulation for the transient response.

Equation (16) was simulated using MATLAB and the simulation results coincide with Tanner simulation. This confirms the correctness of the analysis.

To make it easy for designers to make use of (16), simplification was carried out as follows:

The transconductance and the output admittance of the MOSFET operating in subthreshold are given by the following: $g_m = I_D/nV_T$, $g_{ds} = \lambda I_D$; then using routine analysis, (17) can be reduced to

$$Z_{eq} = \frac{Z}{G} + \frac{nV_T}{GI_1}. \tag{18}$$

It is clear from (18) that the second term is the source of the error and it will be a function of the bias current $I_1$. The error can be minimized if the bias current $I_1$ is increased.

*4.1. Stability Analysis.* The proposed circuit was designed for low frequency applications using MOSFETs operating in the subthreshold mode. Therefore, the parasitic capacitances will

not affect the stability of the circuit. Using (16) and replacing $Z$ with the capacitance, there is only one pole:

$$w_p = \frac{g_{m1} + 1/r_{o1}}{g_{m4}r_{o4}} \approx \frac{g_{m1}}{g_{m4}r_{o4}}. \tag{19}$$

But $g_{m4} = Gg_{m1}$.

Equation (19) can be written as

$$w_p = \frac{1}{G \times r_{o4}}. \tag{20}$$

It is clear from (19), the pole depends on multiplication factor $G$ and $r_{o4}$.

## 5. Applications

The proposed design was used in the design of an RC low pass filter with cutoff frequency of 31.8 Hz. The parameters used in the proposed design are $C = 5$ pF, $R = 10$ Meg resistor, bias current $I_1 = I_3 = 2.5$ nA, and the multiplication factor $G = 100$. It is evident from the simulation results shown in Figure 8 that the filter designed using the proposed $c$-multiplier is in a close agreement in the frequency response with passive RC low pass filter. It is also obvious that the proposed design will work properly in the low frequency applications such as biomedical circuits and systems.

The proposed design was used as a resistance multiplier in the design of RC high pass filter with controllable cutoff frequency. The capacitance used was 5 pf, the resistor to be scaled was 10 Meg, and the bias current is $I_1 = 100$ nA. The control parameters are $G = 0.1$, 0.5, and 0.9. The simulation results shown in Figure 9 indicate that the proposed design is in close agreement with passive RC high pass filter in both the gain and the phase shift.
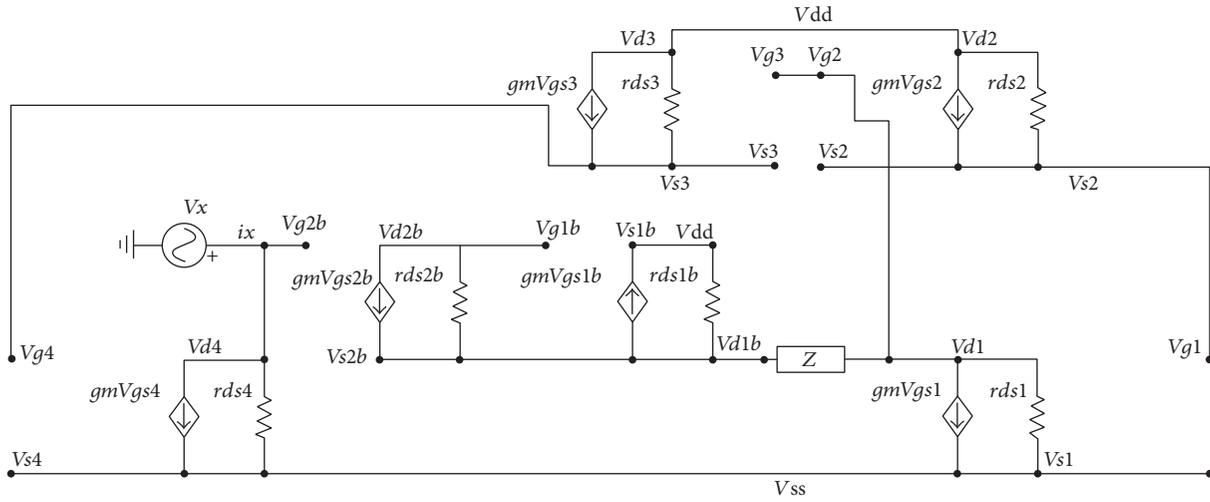
FIGURE 7: Small signal equivalent circuit of the proposed $C$-multiplier.
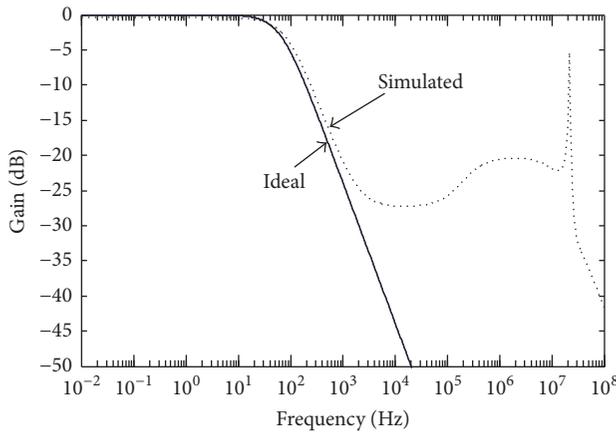


(a)
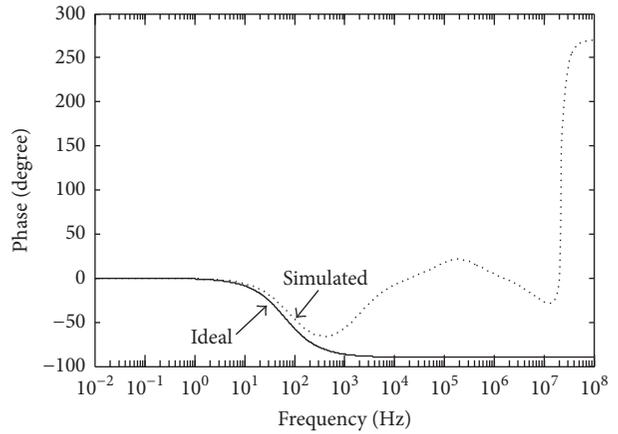
(b)

FIGURE 8: Frequency response for the low pass filter: (a) gain and (b) phase shift.
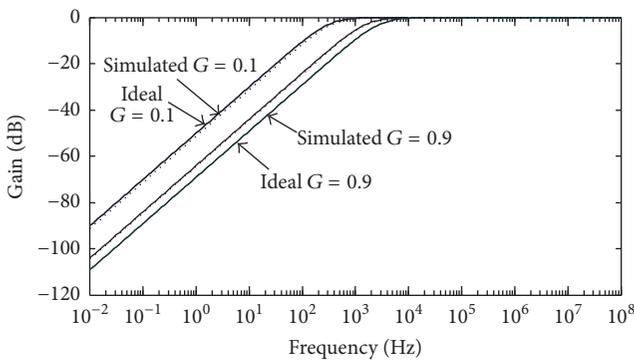


(a)
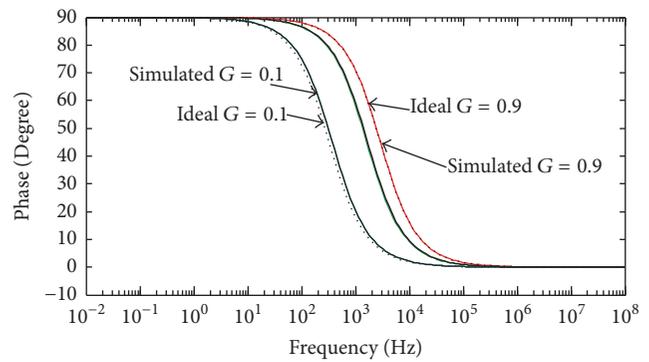
(b)

FIGURE 9: Frequency response for high pass filter: (a) gain and (b) phase shift.

## 6. Conclusion

A new simple and compact impedance multiplier was developed. The design is free of passive elements. The multiplication factor is controllable in the range from 0.1 to 100, which is large compared with previously reported designs. The proposed circuit can be used to scale either the capacitance or the resistance. We believe the developed design will be an excellent building block in integrated circuit design for applications where large time constant is required.

## Conflicts of Interest

The author declares that he has no conflicts of interest.

## Acknowledgments

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