MMI-Based Simultaneous All-Optical XOR–NAND–OR and XNOR–NOT Multilogic Gate for Phase-Based Signals

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***Abstract*— We propose a novel design to simultaneously access various optical logic functions from different output ports. Logical values of inputs and outputs are defined in phase and intensity area of light, respectively. The proposed structure is composed of one multimode interference waveguide with the ultrasmall size of 2.5 μm x 21 μm. Three output ports of proposed structure offer XOR, NAND, and OR logic functions. In addition, XNOR and NOT logic gates are realized by considering some changes in the conditions. Beam propagation method has been utilized to accomplish the simulations of light propagation. Simulation results of structure in whole *C*-band show that the maximum insertion loss is −0.14 dB and the least contrast ratio achieved for XOR, NAND, OR, XNOR, and NOT logic functions are 26, 24.7, 25.9, 26, and 25 dB, respectively.**

***Index Terms*— Beam propagation method, semi binary-phase-shift-keyed, optical logic gate, multimode interference.**

I. Introduction

OPTICAL devices have been providing the groundwork for the emergence of ultra-fast systems and networks. However, general-purpose all-optical elements are still a long way off. Among such optical components, optical logic gates play a vital role in signal processing missions like packet switching or decision making. A variety of techniques identified for conventional information conversions has led to remarkable progress in design of logic gates. In on-off keyed (OOK) signals, data is carried on light intensity. As these format signals can be directly launched into devices, they have attracted much attention from researchers and have been demonstrated in optical logic gates through highly nonlinear fibers (HNLF) [1], microring resonators [2], photonic crystals [3] and multi-mode interference (MMI) waveguides [4]. Nonetheless, phase-based formats like differential and binary phase-shift-keyed (PSK) formats have the advantage of designing the devices which benefit from better optical signal-to-noise ratio (OSNR) and nonlinearity tolerance as compared to OOK form and have been successfully demonstrated in semiconductor optical amplifiers (SOAs) [5], [6], photonic crystals [7], and MMI-based structures [8], [9]. Although there are some valuable reports on the implementation of simultaneous logic gates, however the achieved simultaneities are mostly limited to intensity-based structures all of which realize two complementary logic functions (NOT and XOR/XNOR [10], OR/NOR and AND/NAND [11]).

In this paper, for the first time, we propose a simultaneous three-function optical logic gate without any idle output port. The phase-based format signal is employed in order to avoid nonlinearity-involved process required for simultaneous operations. In order to cover three different logic functions, the phase difference in inputs is $2\pi/3$. The device contains one silicon-silica MMI-based waveguide which supports large bandwidth and data transfer rate. The structure simultaneously provides XOR, NAND, and OR logic functions in different output ports. Also, by some replacements in the input conditions, the other simultaneous logic functions XNOR and NOT are achievable. This is a promising method not only for preventing power loss occurring in idle output ports, but also for compact integration with low power consumption.

In Section 2 we explain a background of MMI principle and present the proposed structure. In section 3 we approach into the design of simultaneous logic functions. Then in section 4, performance of structure is verified by BPM. In section 5, we conclude prospective features of the proposed design.

II. Proposed MMI Structure

Multi-mode interference mechanism leads to the production of multiple images repeated at certain distances along propagation direction referred to as self-imaging phenomena. Based on general interference, first N-fold images of input light with the same amplitudes of $1/N^{1/2}$ are formed at a distance of [12]:

$$L = \frac{3L_\pi}{N}, \quad N \geq 1 \tag{1}$$

The beat length L_π, coupling length of two first order modes, is defined as $L_\pi = 4n_r W_e^2/(3\lambda_0)$, where n_r, W_e and λ_0 are the core refractive index, MMI effective width and free-space wavelength, respectively. W_e is defined as $W_e = W_{MMI} + (\lambda_0/\pi)\left(n_r^2 - n_c^2\right)^{-1/2}$ for TE mode, where W_{MMI} is the width of multimode region. In an N × N MMI-waveguide, the phases of optical output signals are given by [12]:

$$\varphi_{ij} = \pi + \frac{\pi}{4N}(j-i)(2N-j+i) \quad for\ i+j\ even \tag{2}$$

$$\varphi_{ij} = \frac{\pi}{4N}(j+i-1)(2N-j-i+1) \quad for\ i+j\ odd \tag{3}$$

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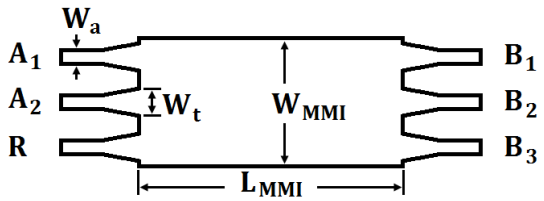

Fig. 1. Schematic of MMI-based simultaneous multi-logic gate structure.

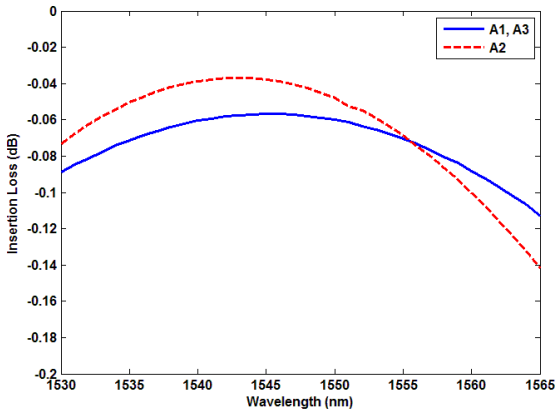

Fig. 2. Insertion loss spectrum in C-band.

where $i = 1, 2, \ldots, N$ and $j = 1, 2, \ldots, N$ are bottom-up numbered input and top-down numbered output access waveguides, respectively.

The proposed structure of MMI-based all-optical multi-logic gate is presented in Figure 1. The structure is composed of one MMI waveguide. There are two logical inputs A_1 and A_2, one reference input R and three output ports B_1, B_2 and B_3 corresponded to output logical functions. The employed materials for cladding and core layers are SiO_2 and Si with the refractive indices of $n_c = 1.46$ and $n_r = 3.48$, respectively. For the wavelength of 1550 nm, the multi-mode waveguide has the width and length of $W_{MMI} = 2.5\mu$m and $L_{MMI} = 21.1\mu$m, respectively. Lateral access waveguides are located at lateral distance of $\pm W_e/3$ with respect to the center of MMI waveguide in order to obtain 3-fold images. The width of single mode access ports is $W_a = 0.4\mu$m. To optimize transmission characteristics, tapered waveguides with $W_t = 0.65\ \mu$m and $L_t = 1.5\ \mu$m have been considered in access points.

Insertion loss spectrum of the structure is shown in Fig. 2. Insertion loss of the input port i is defined as

$$I.L._i = 10\log_{10}\frac{P_{B1} + P_{B2} + P_{B3}}{P_{Ai}} \tag{4}$$

where P_{Bj} is the light power of ^{j}th output port and P_{Ai} is the input power of ^{i}th input port. Maximum insertion loss in whole C-band is -0.14dB.

III. Design Characteristics

We assume polarizations of input lights are the same. As from (2) and (3), the relationship between complex input and output fields of a 3×3 MMI coupler can be

TABLE I
Expected Group Outputs for Simultaneous XOR, NAND, and OR Logic Functions

Logical Inputs		Logical Outputs		
A_1	A_2	XOR B_1	NAND B_2	OR B_3
0	0	0	1	0
0	1	1	1	1
1	0	1	1	1
1	1	0	0	1

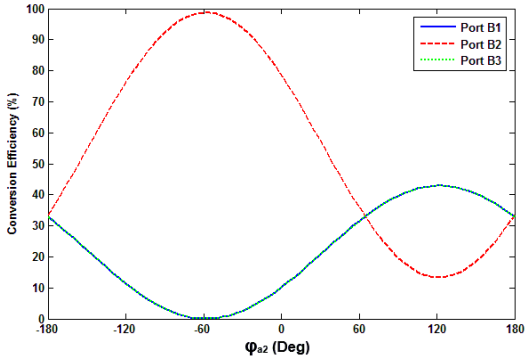

Fig. 3. Conversion efficiency when $\varphi_r = 0$ and $\varphi_{a1} = 0$ for $\lambda = 1550$ nm.

presented as

$$\frac{1}{\sqrt{3}}\begin{bmatrix} e^{-j\frac{\pi}{3}} & e^{j\frac{2\pi}{3}} & e^{j\pi} \\ e^{j\frac{2\pi}{3}} & e^{j\pi} & e^{j\frac{2\pi}{3}} \\ e^{j\pi} & e^{j\frac{2\pi}{3}} & e^{-j\frac{\pi}{3}} \end{bmatrix}\begin{bmatrix} A_1 \\ A_2 \\ R \end{bmatrix} = \begin{bmatrix} B_1 \\ B_2 \\ B_3 \end{bmatrix} \tag{5}$$

with $R = re^{j\varphi_r}$, $A_i = a_i e^{j(\varphi_{ai}+\varphi_r)}$, and $B_i = b_i e^{j(\varphi_{bi}+\varphi_r)}$, where φ_r is reference light phase and also φ_{ai} and φ_{bi} are relative phases of A_i and B_i with respect to the reference light, respectively.

Since we have considered three output ports, it is possible to access three functions like XOR, NAND and OR logics from output ports B_1, B_2 and B_3 at the same time. In order to obtain simultaneous logic functions, all of the output ports ought to be considered as a unit. Table I presents the expected group of logical outputs for XOR, NAND and OR functions.

As can be seen in Table I, in order to achieve the mentioned logics at the same time, four sets of desired outputs exist. By assuming the absence of light as logic 0 and presence of light as logic 1, for attaining the set of 0:1:0 respectively for B_1:B_2:B_3 light should be absent in outputs B_1 and B_3. Assuming same polarization and intensity for all input lights, one possible way of attaining $B_1 = 0$ is through phase expressions derived from (5) as follows:

$$(\pi + \varphi_r) - \left(\frac{2\pi}{3} + \varphi_{a2} + \varphi_r\right) = \frac{2\pi}{3} \tag{6}$$

$$\left(\frac{2\pi}{3} + \varphi_{a2} + \varphi_r\right) - \left(\frac{-\pi}{3} + \varphi_{a1} + \varphi_r\right) = \frac{2\pi}{3} \tag{7}$$

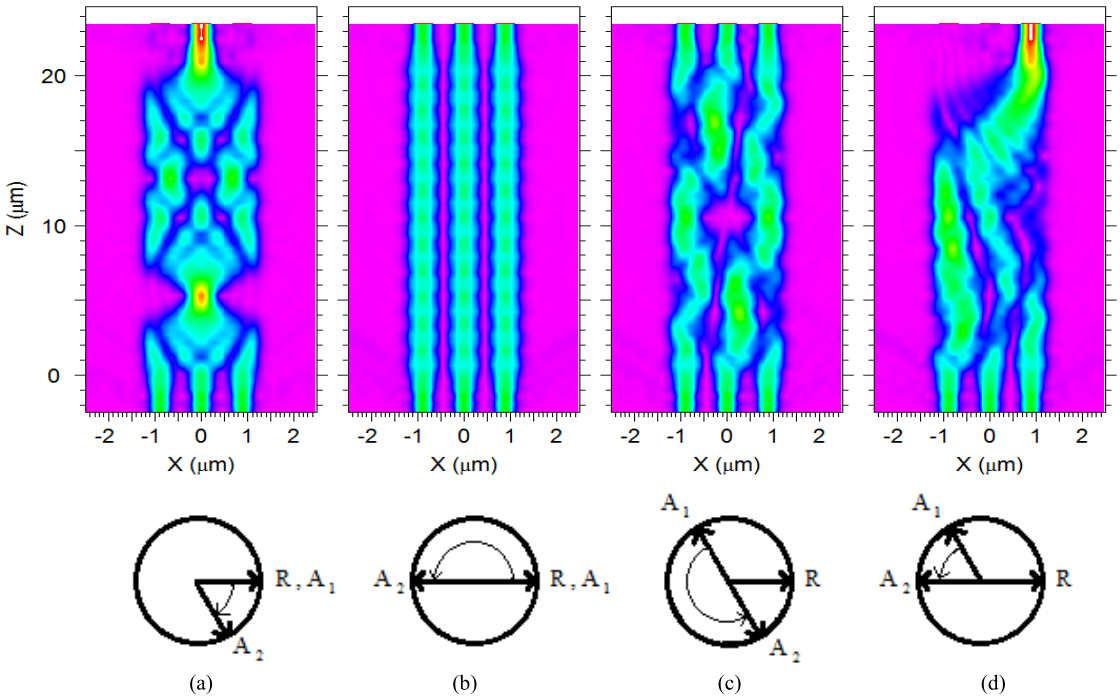

Fig. 4. BPM-simulated light intensity profile of proposed structure for $\varphi_r = 0$, and a) $\varphi_{a1} = 0$, $\varphi_{a2} = 5\Pi/3$ b) $\varphi_{a1} = 0$, $\varphi_{a2} = \Pi$ c) $\varphi_{a1} = 2\Pi/3$, $\varphi_{a2} = 5\Pi/3$ d) $\varphi_{a1} = 2\Pi/3$, $\varphi_{a2} = \Pi$.

TABLE II
PERFORMANCE OF SIMULTANEOUS MULTI-LOGIC GATE INVOLVING BPM-SIMULATED RESULTS OF FUNCTIONS XOR, NAND AND OR

Inputs					Outputs						Fig. 4
Logic A_1	Logic A_2	φ_r	φ_{a1}	φ_{a2}	B_1 (XOR)		B_2 (NAND)		B_3 (OR)		
					logic	η(%)	logic	η(%)	logic	η(%)	
0	0	0	0	5π/3	0	0.07	1	98.7	0	0.07	a
0	1	0	0	π	1	32.8	1	33.6	1	32.8	b
1	0	0	2π/3	5π/3	1	34.8	1	31.5	1	32.3	c
1	1	0	2π/3	π	0	0.002	0	0.07	1	98.5	d

Therefore if we assume $\varphi_r = 0$, input phases are estimated as $\varphi_{a1} = 0$ and $\varphi_{a2} = 5\pi/3$. It is evident from (5) that these conditions cause $B_3 = 0$ as well. Therefore, provided that phases of input lights A_1 and A_2 are 0 and $5\pi/3$ respectively, there will be no light at both output ports B_1 and B_3. It is clear that there are other circumstances which will result in $B_1 = 0$ as follows:

$$(\pi + \varphi_r) - \left(\frac{-\pi}{3} + \varphi_{a1} + \varphi_r\right) = \frac{2\pi}{3} \quad (8)$$

$$\left(\frac{-\pi}{3} + \varphi_{a1} + \varphi_r\right) - \left(\frac{2\pi}{3} + \varphi_{a2} + \varphi_r\right) = \frac{2\pi}{3} \quad (9)$$

In this case, the input phases can be changed as $\varphi_{a1} = 2\pi/3$ and $\varphi_{a2} = \pi$. These conditions also gain $B_3 = 0$ simultaneously. This means that when phases of A_1 and A_2 are considered to be $2\pi/3$ and π respectively, output lights from B_1 and B_2 become zero. Hence, in order to fulfill the requirements of Table I, phase of input lights A_1 and A_2 for the logics 0:1 are $0{:}2\pi/3$ and $5\pi/3{:}\pi$, respectively. It is obvious that specified conditions satisfy the other two group outputs. In practice there may be anphase error between inputs and reference light. The phase (input) to intensity (output) conversion efficiency of structure is assessed in Fig. 3. Conversion efficiency is defined as

$$\eta = \frac{P_{Bi}}{P_{Bi\,\max}} \times 100 \qquad for\ \ i = 1, 2, 3 \quad (10)$$

where P_{Bi} and P_{Bimax} are the power and maximum power of ^{i}th output, respectively.

IV. SIMULATION RESULTS

Beam propagation method (BPM) is applied to verify the performance of the structure under the defined circumstances.

Simulation results of proposed simultaneous multi-function logic gate are shown in Fig. 4. The performance of the design is indicated in Table II. The phases of inputs A_1 and A_2 for for logics 0:1 are $0{:}2\pi/3$ and $5\pi/3$:phases of inputs A_1 and A_2 for logics 0:1 are $0{:}2\pi/3$ and $5\pi/3{:}\pi$, respectively. If we assume the absence of light as logic 0 and the presence of light as logic 1, from Table II can be seen that output ports B_1, B_2 and B_3, respectively, function as XOR, NAND and OR logics simultaneously. Note that the reference phase is assumed to be zero; otherwise φ_r should be added to phases. Output light power can also be verified from Figure 3 when

TABLE III
REALIZATION OF XNOR AND NOT LOGICS BY EXCHANGING THE INPUT CONDITIONS

Inputs					Logic Outputs			Fig. 4
Logic A_1	Logic A_2	φ_r	φ_{a1}	φ_{a2}	B_1 (XNOR)	B_2 (NOT A_1)	B_3 (NOT A_2)	
0	0	0	0	π	1	1	1	b
0	1	0	0	$5\pi/3$	0	-	0	a
1	0	0	$2\pi/3$	π	0	0	-	d
1	1	0	$2\pi/3$	$5\pi/3$	1	-	-	c

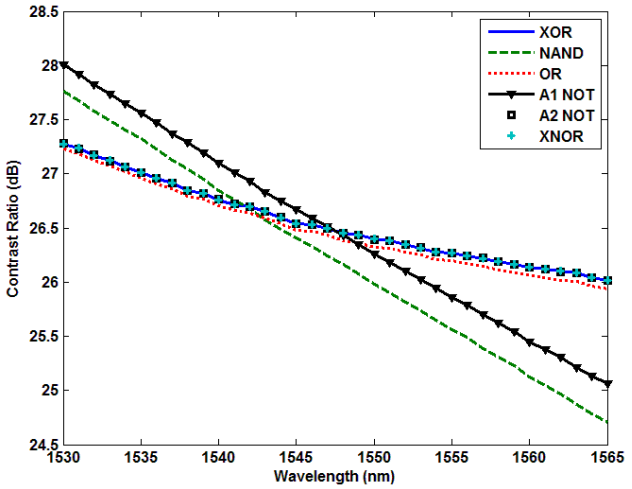

Fig. 5. The on-off logic-level contrast ratio of logic functions XOR, NAND, OR, XNOR and NOT, in C-band wavelengths.

the phase difference between the input lights A_1 and A_2 are π or $+5\pi/3$. Moreover, as can be seen, for the cases in which we have simultaneously two logic 0 with one logic 1 ($\varphi_{a2} = \pi/3$), and simultaneously three logic 1 ($\varphi_{a2} = \pi$) in outputs, the phase difference is $2\pi/3$.

By reconsideration of results shown in Table II, XNOR and NOT logic functions are also achievable by exchanging the order of group outputs. Table III shows the realization conditions of XNOR and NOT logic gates. By changing corresponding phases of logics 0:1 of input A_2 from $5\pi/3{:}\pi$ to $\pi{:}5\pi/3$ XNOR and NOT functions are realized. As the NOT function is defined for one input, with the aim of accessing NOT logic of one input, the other logic input is supposed to be zero. This means that the output B_2 will work as NOT logic of A_1, assuming $\varphi_{a2} = \pi$. In addition, if $\varphi_{a1} = 0$, the output B_3 will be NOT logic of A_2. Hence, in addition to XOR, NAND and OR logics, XNOR and NOT logic functions are realized. One of the main parameters which can show the performance of logic structures is the on-off logic-level contrast ratio which can be defined as:

$$C.R. = 10\log_{10}\frac{P_1}{P_0} \tag{11}$$

where P_0 and P_1 are the output powers corresponding to the worst logic 0 and 1 of a logic function, respectively. Figure 5 shows contrast ratio spectrum for each of the logic functions in whole C-band. As can be seen in Fig. 5, the least on-off contrast ratio of XOR, NAND, OR, XNOR and NOT logics are, respectively, 26.0 dB, 24.7 dB, 25.9 dB, 26.0 dB, 25.1 dB and 26.0 dB. For $\lambda = 1550$ nm, the corresponding contrast ratios are 26.4 dB, 26.0 dB, 26.6 dB, 26.4 dB, 26.3 dB and 26.4 dB.

V. CONCLUSION

We have established a method in order to design a simultaneous multi-logic gate in which each output port functions as an expected operation and there is no power loss in idle ports. Benefiting from phase-based format, we propose XOR, NAND and OR logic functions packed in one MMI-Based structure. In addition, through the replacement of current phase terms we are capable of demonstrating the other set of logical functions XNOR and NOT. Applying BPM, least On-Off level contrast ratio for XOR, NAND, OR, XNOR, and NOT logic functions is obtained 26.0 dB, 24.7 dB, 25.9 dB, 26.0 dB, 25.0 dB and 26.0 dB, respectively. For obtaining a constant level of intensity in output, a limiting amplifier like an SOA with a saturated gain in output can be considered. This proposal is a targeted approach into the design of future signal processing networks equipped with efficient ultra-compact devices.

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