A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems

Haibing Hu, *Member, IEEE*, Souhib Harb, *Student Member, IEEE*, Nasser Kutkut, Issa Batarseh, *Fellow, IEEE*, and Z. John Shen, *Fellow, IEEE*

***Abstract*—The reliability of the microinverter is a very important feature that will determine the reliability of the ac-module photovoltaic (PV) system. Recently, many topologies and techniques have been proposed to improve its reliability. This paper presents a thorough study for different power decoupling techniques in single-phase microinverters for grid-tie PV applications. These power decoupling techniques are categorized into three groups in terms of the decoupling capacitor locations: 1) PV-side decoupling; 2) dc-link decoupling; and 3) ac-side decoupling. Various techniques and topologies are presented, compared, and scrutinized in scope of the size of decoupling capacitor, efficiency, and control complexity. Also, a systematic performance comparison is presented for potential power decoupling topologies and techniques.**

***Index Terms*—Lifetime, microinverter, photovoltaic (PV), power decoupling, reliability, single-phase inverter.**

I. Introduction

ACCORDING to International Energy Outlook 2011 estimation, world electricity generation increases by 77 percent from 2006 to 2030, which increases from 18.0 trillion kWh in 2006 to 31.8 trillion kWh in 2030 [1]. Based on the most advanced scenario which corresponds to Intergovernmental Panel on Climate Change emission reduction targets, renewable energy, by 2050, will account for 46% of global power. Among the renewable energy technologies, photovoltaic (PV) will play a major role [2]. To meet the 2020 renewable energy targets of the European Union, the European Photovoltaic Industry Association recently estimated that the possible contribution of PV is up to 12% of the electricity supply by 2020. Over the past 20 years, solar electric energy has grown consistently by 30%. As shown in Fig. 1, world solar PV market installation reached a record high of 69.68 GW in 2011, representing a growth of 76% over the previous year, in which grid-connected systems represent the largest share of the market [3]. One of the key components of the grid-connected PV system is the grid-connected inverter.

The grid-connected inverter for PV system is categorized into three categories: centralized inverter, string inverter, and ac-module "microinverter" [4], [5]. Microinverter, with power levels ranging from 150 to 300 W, has become the trend for grid-connected PV systems due to its numerous advantages including improved energy harvest, improved system efficiency, lower installation costs, "Plug-N-Play" operation, and enhanced modularity and flexibility. However, many challenges remain in the way of achieving low manufacturing costs, high conversion efficiencies, and long life span. Since microinverter is typically attached to the back of the PV panel, and may be well integrated to the PV panel back skin, it is desirable that the inverter has a lifetime that matches the PV panel one. It is well known that electrolytic capacitors are the limiting components that determine the lifetime of the microinverter [6]. Hence, different inverter topologies have been proposed that use film capacitors instead as they will be explained thoroughly in this paper.

For applications with power level under several kilowatts, the single-phase connection is commonly used. However, in single-phase connection, the power flow to the grid is time varying, while the power extracted from the PV panel must be constant for maximizing energy harvest consequently, a mismatch between the input instantaneous power and the output instantaneous ac power. Therefore, energy storage elements must be placed between the input and output to balance (decouple the unbalance) the different instantaneous input and output power. Usually, a capacitor is used to serve as a power decoupling element. However, the lifetime of different types of capacitors varies greatly, e.g., electrolytic capacitors typically have a limited lifetime, namely 1000–7000 h at 105 °C operating temperature [7]. Most of presently available commercial microinverters use electrolytic capacitors as power decoupling storage elements due to their large capacitance and ease of implementation, which tend to limit the lifetime of the microinverter [6], [8]–[10]. Some researchers have explored various ways to reduce the size of the

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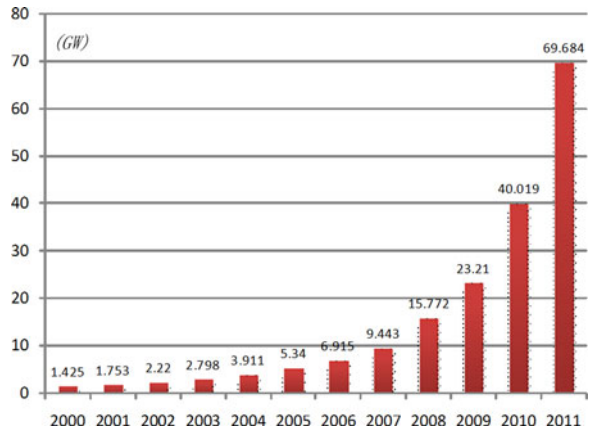

Fig. 1. Cumulative PV system installation in IEA PVPS member Countries.

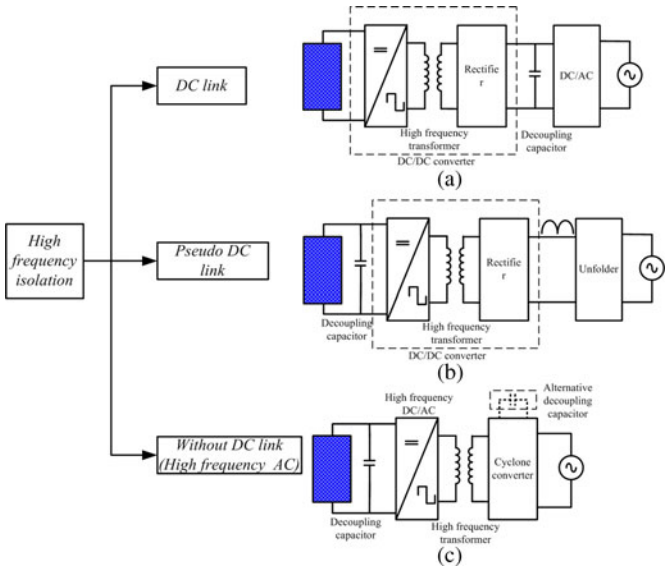

Fig. 2. Basic microinverter configurations.

required capacitance so as to allow for other longer lifetime capacitor technologies, such as film capacitors, to be used.

In grid-connected PV applications, the electrical isolation is necessary for safety issues [4]. In terms of the operating frequency of the isolation transformer, the microinverter configurations can be categorized into two basic groups: 1) isolation with line-frequency transformer; and 2) isolation with high-frequency transformer. Since the line transformer is bulky and costly, it is not recommended for microinverter applications. In this paper, we mainly focus on the microinverter configurations that employ high-frequency transformer.

Microinverter configurations with high-frequency transformer fall into three basic categories based on the dc-link configurations [5]: dc link, pseudo dc link, and high-frequency ac, as shown in Fig. 2.

As seen in Fig. 2(a), in the dc-link implementation, dc–dc converter is designed to implement the maximum power point tracking (MPPT) and amplify the PV dc voltage to a sufficient voltage level compatible with the grid. Any dc–dc topology that provides galvanic isolation can be the candidate for the dc–dc stage. Fig. 2(b) shows the microinverter configuration with pseudo dc link, where the voltage is expected to be rectified-sine waveform, and the unfolding inverter, operating at line frequency, converts the rectified sine waveform into the sine waveform. In this configuration, the power decoupling capacitor cannot be placed at the dc link. It is employed at PV side instead, and usually this results in a large capacitance due to low the dc level and the need for ripple-free voltage at PV side. If we replace the rectifier circuit at the secondary side with the cycloconverter, a new configuration without dc link is derived, as illustrated in Fig. 2(c). In this case, the cycloconverter directly converts the high-frequency ac into the desired line-frequency ac output. As for the power decoupling capacitor, in this case, usually it is placed at the PV side, which is similar to the previous case, and a large capacitance is needed. However, the power decoupling capacitor can be optionally employed at the ac side, and consequently, a very small capacitance is needed for the same power ratings.

This paper scrutinizes the various power decoupling techniques that have been proposed and compares their performance in terms of efficiency, cost, and control complexity. The paper is organized as follows. Power decoupling principle is presented in Section II. A review of the power decoupling techniques is presented in Section III. Section IV compares potential power decoupling techniques. Then, a performance discussion is presented in Section V, and finally, the conclusion is drawn in Section VI.

II. Power Decoupling Principle

In a grid-connected single-phase inverter, the injected current to the grid $i(t)$ and the grid voltage $u(t)$ are given by

$$\begin{cases} u(t) = U\sin(\omega_o t) \\ i(t) = I\sin(\omega_o t + \varphi) \end{cases} \tag{1}$$

where ω_o is the grid frequency, U and I are the amplitudes of the grid voltage and current, respectively. φ is the phase shift between the injected current and the grid voltage, which is desirable to be zero for unity power factor operation. The instantaneous output power $P_o(t)$ is given as follows:

$$P_o(t) = \frac{1}{2}UI\cos(\varphi) + \frac{1}{2}UI\cos(2\omega t + \varphi). \tag{2}$$

When phase shift φ is zero, the expression in (2) can be rewritten as

$$P_o(t) = \frac{1}{2}UI + \frac{1}{2}UI\cos(2\omega t). \tag{3}$$

The output instantaneous power in (3) consists of two terms: the average output power $^1\!/_2 UI$, and the time varying term (pulsating power) $^1\!/_2 UI\cos(2\omega t)$, which oscillates at twice the line frequency. However, the input power from the PV module $P_{\rm PV}$ is controlled to be constant and operate at maximum power point (MPP). Assuming a lossless inverter stage, the power generated by the PV module equals the average output power, as shown in Fig. 3.

To maintain power balance, the pulsating power, $P_{\rm oac} = P_o - P_{\rm dc}$, must be handled by an energy storage device. Usually,

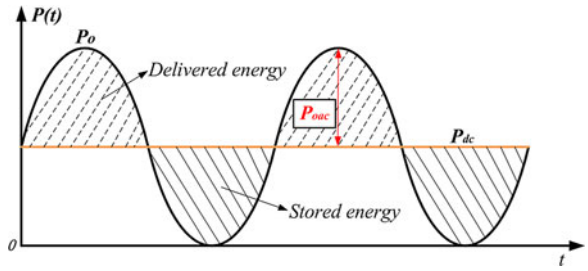

Fig. 3. Total power processed by the decoupling capacitor.

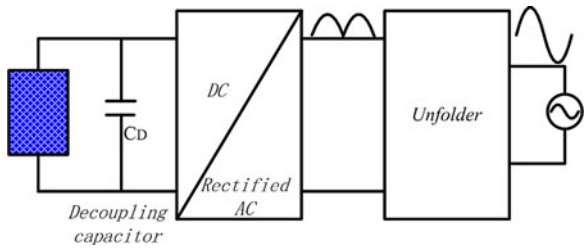

Fig. 4. Single-stage inverter.

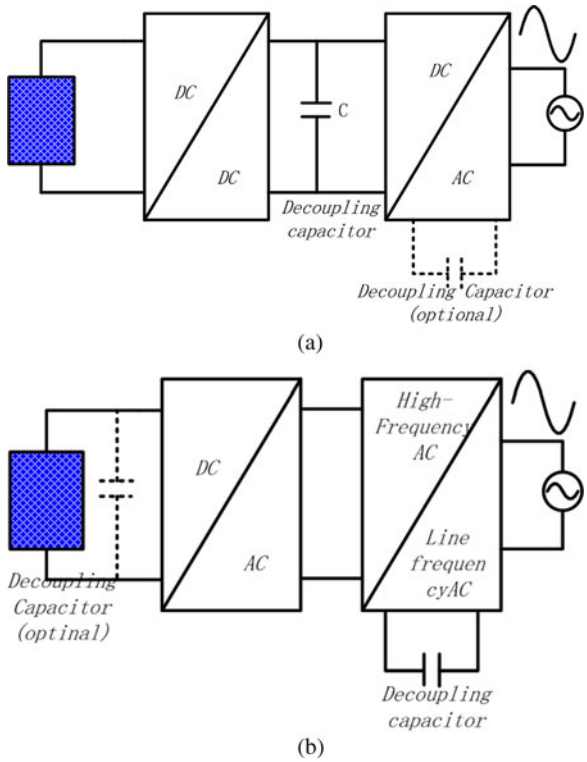

Fig. 5. Multistage inverter. (a) DC-link approach. (b) AC-link approach.

a capacitor "*decoupling capacitor*" is used to mitigate the power ripple effect at the PV-module side [11]. This decoupling capacitor can be embedded within the inverter stage or just connected in parallel with the PV module. The energy that is being charged to or discharged from the decoupling capacitor during a half-line cycle can be calculated by integrating one of shadowed area in Fig. 3

$$E_{CD} = 2\left(\int_0^{\frac{1}{8f_{\rm grid}}} (P_{\rm dc} - P_o(t))dt\right) = \frac{1}{2}C_D(U_{\rm dc\_max}^2 - U_{\rm dc\_min}^2) \quad (4)$$

where $f_{\rm grid}$ is the line (grid) frequency, and $U_{\rm dc\_max}$ and $U_{\rm dc\_min}$ are maximum and minimum voltages across the decoupling capacitor.

Combining (3) and (4), the required decoupling capacitance is found to be as follows:

$$C = \frac{P_{\rm dc}}{2\pi f_{\rm grid} U_{\rm dc} \Delta u} \quad (5)$$

where

$U_{\rm dc} = \frac{1}{2}(U_{\rm dc\_max} + U_{\rm dc\_min})$ is an average dc voltage across C_D, and

$\Delta U_{\rm dc} = U_{\rm dc\_max} - U_{\rm dc\_min}$ is the voltage ripple across C_D.

The expression for decoupling capacitance in (5) shows that, for a microinverter with a given power rating and line frequency, the size of the required decoupling capacitance is determined by the dc voltage and maximum allowable voltage ripple. Consequently, the only way to change the decoupling capacitance value is by manipulating these two parameters. A small capacitance can be achieved by increasing $U_{\rm dc}$ or (and) $\Delta U_{\rm dc}$.

III. Power Decoupling Techniques

Based on the microinverter topology that is being employed, different power decoupling techniques can be implemented. As shown in Section I, basically microinverter topologies can be divided into three groups, according to the dc-link configurations. Normally, the pseudo dc-link configuration is referred as single-stage inverters, while other configurations are referred as multistage inverters. The single-stage inverters, as shown in Fig. 4, accomplish both tasks: boosting the input voltage, and sine or rectified sine waveform modulation. In this case, the only way to employ the power decoupling capacitor is to place it at the PV side. On the other hand, multistage inverters can be further classified into dc–ac–dc–ac and dc–ac–ac, as shown in Fig. 5. For the topologies with dc–ac–dc–ac configurations, the first power stage usually is used to boost the low PV voltage to a high dc voltage level compatible to the grid voltage, as well providing electrical isolation. In this case, it is recommended to place the decoupling capacitor at the high-voltage dc link, which will reduce the required decoupling capacitance, according to (5). By adding several active switches and reactive components, the decoupling capacitor can also be placed at the ac output side. Cycloconverters, changing high-frequency ac to line-frequency ac, are used in topologies with dc–ac–ac implementation, in which the power decoupling capacitor can only be placed at the PV side or at the ac side. Detailed description and analysis are given in the following sections. Based on the location of the decoupling capacitor and associated circuitry, three decoupling techniques can be identified: 1) PV-side decoupling; 2) dc-link decoupling; and 3) ac-side decoupling.

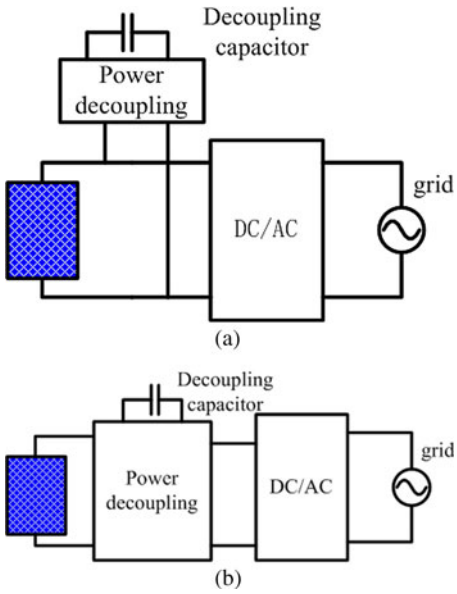

Fig. 6. Employing power stage to realize power decoupling at the PV side. (a) Decoupling circuit in parallel with PV. (b) Decoupling circuit in series with PV.

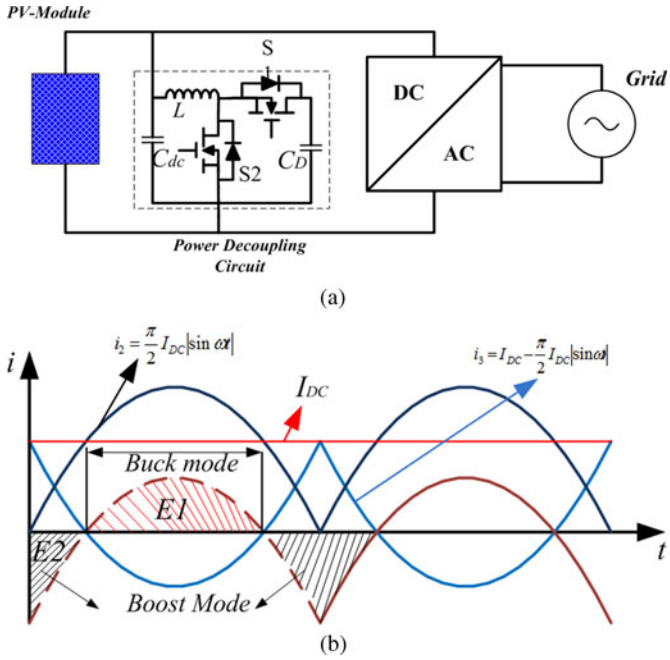

Fig. 7. (a) Topology proposed by Kyritsis *et al*. [12]. (b) Power decoupling control strategy.

A. PV-Side Decoupling

In a single-stage microinverter topology as shown in Fig. 4, having the power capacitor across the PV panel terminals results in a very large capacitor since the allowable voltage ripple must be kept to very low values (<1%) in order to achieve high MPP efficiency [4], [11]. For example, for a 200-W microinverter, the minimum decoupling capacitance required is 13.9 mF in order to achieve a 98% PV utilization factor [4]. This represents a very large value, which increases the size of the microinverter and, more importantly, negatively impacts its lifetime. One potential solution is to add an auxiliary circuitry, between the PV panel and the inverter, to decouple the ac pulsating power while maintaining the MPP voltage stable, as shown in Fig. 6.

A bidirectional buck–boost converter was proposed by Kyritsis *et al*. [12] to realize the power decoupling, as shown in Fig. 7(a). With this active filter technique, the decoupling capacitor C_d is reduced from 3000 to 100 μF by increasing the average voltage and ripple voltage across the decoupling capacitor to 62 and 35 V, respectively. As shown in Fig. 7(b), the average current i_2, injected to the grid, is a rectified sinusoidal waveform. To maintain the input current $I_{\rm DC}$ constant, the buck–boost current i_3 should be complementary to the current i_2 with the offset $I_{\rm DC}$. Based on the current direction, the buck–boost converter has two operation modes: In buck mode, the energy stored in the decoupling capacitor is released to the grid, while in boost mode, the surplus power from the PV source is stored to the decoupling capacitor. Current hysteresis control is employed to control the current and make it follow a given reference. Although in [12] no specific number regarding the overall inverter efficiency is mentioned, the power losses associated with the decoupling circuit will reduce the overall efficiency. Moreover, using a smaller decoupling capacitor leads to higher stresses for the power devices, which may result in more losses and lower efficiency. Similar concept is also found in other applications [13], [14].

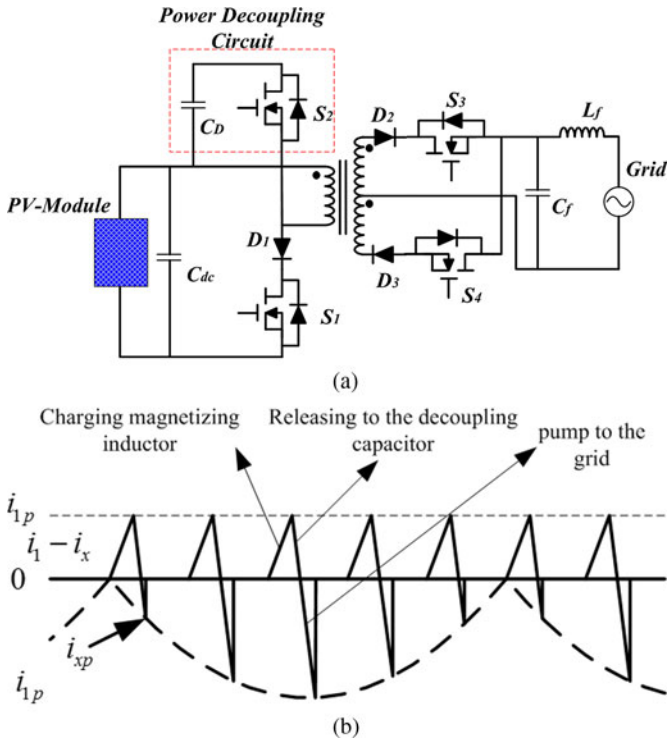

Fig. 8. (a) Topology proposed by Shimizu *et al.* [15]. (b) Magnetizing currents at primary side.

The topology, shown in Fig. 8(a), is a flyback-type single-stage microinverter with a decoupling power circuit, in which a 40-μF film capacitor was used for a 100-W system. In this topology, the constant power from PV is first transferred to

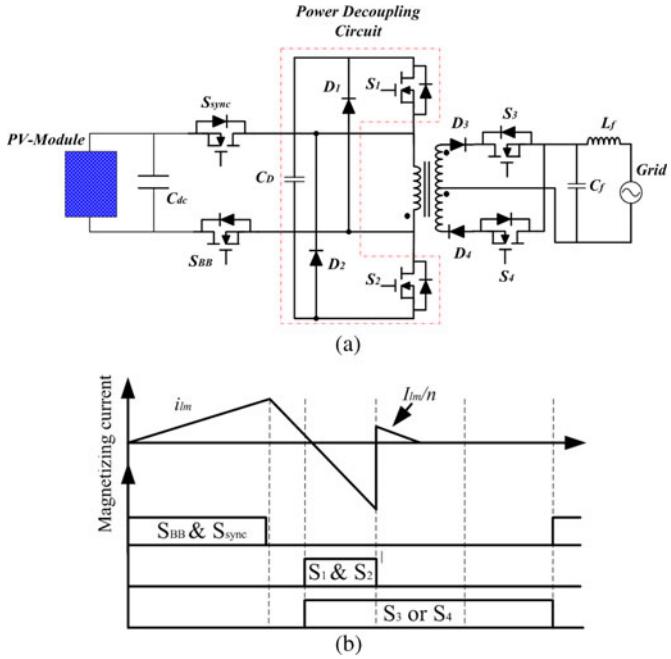

Fig. 9. (a) Modified topology proposed by Kjaer and Blaabjerg [16]. (b) Key waveforms in one switching cycle.

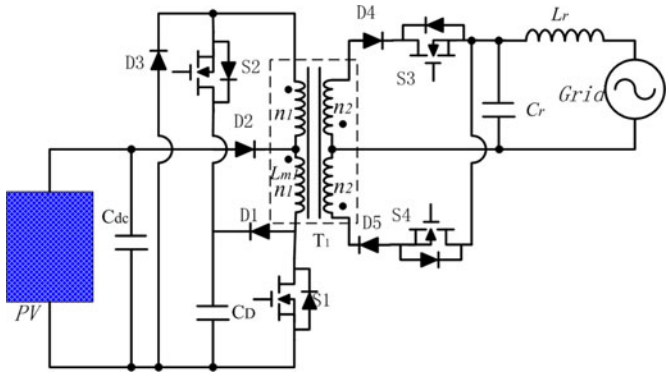

Fig. 10. Topology proposed by Hu *et al.* [17].

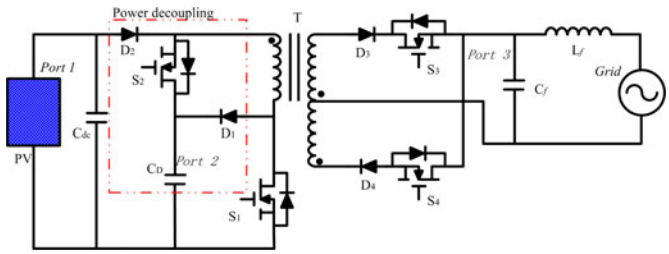

Fig. 11. Topology proposed by Harb *et al.* [18].

the decoupling capacitor C_D, which is then modulated with a rectified sine waveform and pumped into the grid. As shown in Fig. 8(b), the power from PV first is charged to the fly-back transformer and then is released to the decoupling capacitor C_D. After that, the energy stored in the capacitor pumps to the grid in a sinusoidal form. Given the cascaded conversion process, the projected efficiency will be low, as indicated in [15], where 70% is achieved as the peak efficiency.

Fig. 9(a) shows a modified topology proposed by Kjaer and Blaabjerg [16], where the leakage inductance energy is recycled using a "dual-switch flyback converter." As shown in Fig. 9(b), the energy from PV is stored in the magnetizing inductor by switching ON $S_{\rm sync}$ and $S_{\rm BB}$ simultaneously. Then, the energy in the magnetizing inductor is charged to the decoupling capacitor through D_1 and D_2 once the switches $S_{\rm sync}$ and $S_{\rm BB}$ turn OFF. When the switches S_1 and S_2 turn ON at the same time, same to the fly-back converter, the decoupling capacitor C_D charges the energy to the magnetizing inductor again and in this manner, the sinusoidal current to be injected to the grid is controllable by switching on a specific duration for S_1 and S_2. Even with design optimization, the estimated peak efficiency is 86.7% [16].

The authors in [17] and [18] proposed three-port flyback topologies with one port dedicated to the power decoupling function, as shown in Figs. 10 and 11. The power decoupling capacitor serves both as an energy storage element and as a snubber to recycle the leakage energy. For a 100-W inverter, the decoupling capacitance can be as low as 46 μF with an average voltage of 150 V and a 40-V ripple across the decoupling capacitor. The operation principle of these two topology is quite the same, whose key waveforms are illustrated in Fig. 12, except that the peak magnetizing current in Fig. 10 is constant, while in Fig. 11, its peak value is variable in mode I and is constant in mode II. These two topologies have two operation modes: In mode I, where the input power is larger than output power to the grid, the surplus energy from PV is charged to the decoupling capacitor C_D; in mode II, where the input power is less than the output power, the power from the decoupling capacitor compensates the deficit power by switching on the S_2. By operating the converter in discontinuous conduction mode, the peak efficiency can reach up to 90.6% including auxiliary power consumption [17].

Fig. 13(a) shows a novel microinverter with power decoupling capability, which is composed of a push–pull type forward converter, an unfold inverter, and a decoupling circuit depicted in a dotted-line area [19]. For a 500-W microinverter, the decoupling capacitance is as small as 50 μF in simulation and the voltage ripples across its terminals are around 100 V. As shown in Fig. 13(b), the topology has two operation modes: 1) in mode I, the surplus power is charged to the decoupling capacitor by turning ON the S_{x0} and the switch S_{m1} or S_{m2} turns ON alternatively to pump the power to the grid. 2) In mode II, besides the power transfers from the PV source directly to the grid by turning ON the S_{m1} or S_{m2}, decoupling capacitor C_x also pumps its energy stored in mode I to the grid by turning ON S_{x1} or S_{x2}. The reported conversion efficiency is 95% [19]. Hirao *et al*. also proposed a flyback-based microinverter, as shown in Fig. 14(a) [20].

A time-shared magnetizing modulation method is employed to avoid double power conversion as shown in Fig. 14(b), whose operation principle is similar to those in Figs. 10 and 11. The decoupling capacitor only stores surplus power from the PV in mode I and releases the deficit power in Mode II, which results in higher conversion efficiency in comparison to those in

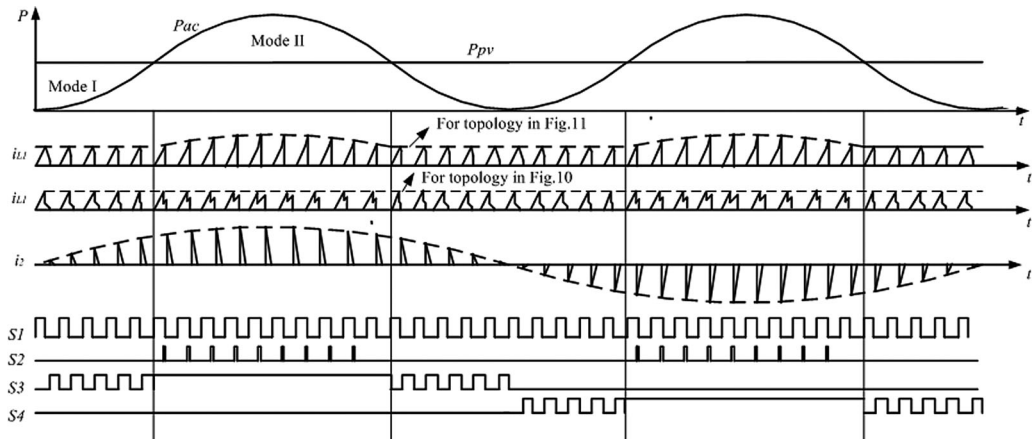

Fig. 12. Key waveforms for Figs. 10 and 11.

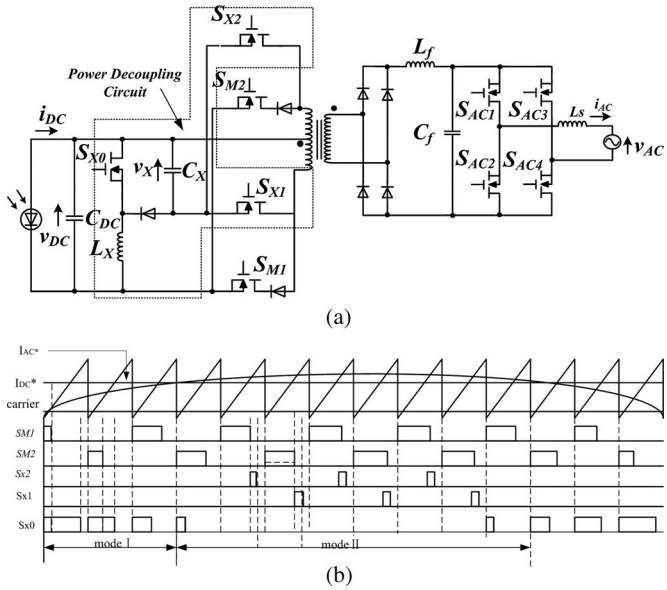

Fig. 13. (a) Topology proposed by Shinjo *et al.* [19]. (b) Driver signal generation.

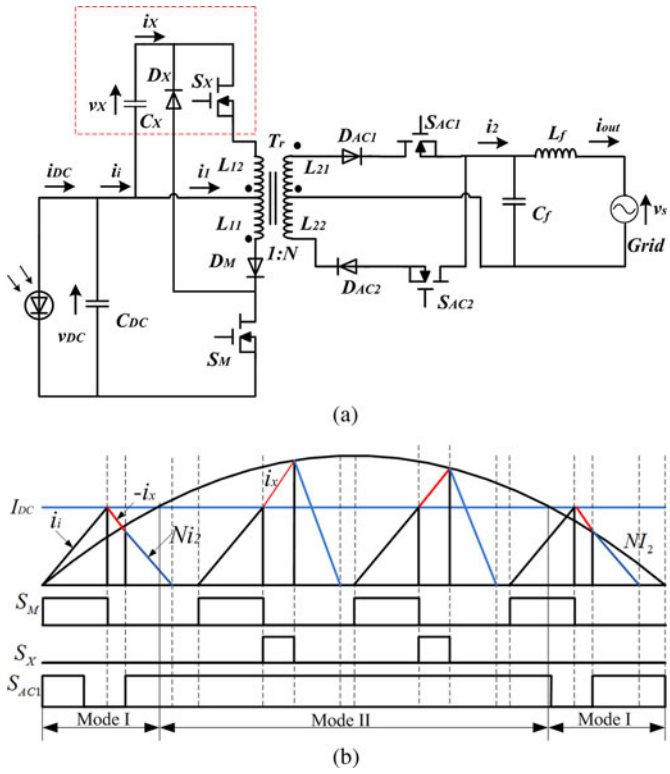

Fig. 14. (a) Topology proposed by Hirao *et al.* [20]. (b) Magnetizing current and driver signals.

[15] and [16]. Although the proposed topology and method can improve the conversion efficiency, the efficiency only increases from 65% to 73%, which is still too low from practical point of view [20].

Chen and Liao added additional winding and an active power decoupling circuit on a conventional Flyback, as shown in Fig. 15(a). As shown in Fig. 15(b), in mode I, the surplus power from PV source is charged to the decoupling capacitor through the third winding and two switches S_{M4} and S_{M6}, while in Mode II, the energy stored in the decoupling capacitor C_3 is delivered by turning ON the S_{M5} and S_{M3} to the magnetizing inductor to offer the deficit power. Only 40-μF decoupling capacitor is used for a 200-W microinverter system, and the voltage ripple across the decoupling capacitor can reach as high as 100 V [21]. Li *et al*. proposed a new flyback-based microinverter, as shown in Fig. 16(a), by using a boost converter to store the energy in the decoupling capacitor C_D, and release this energy to magnetizing inductor through S_2 [22], whose operation principle is illustrated in Fig. 16(b). In Mode I, the power delivered to the grid is controlled by turning ON S_3, while the surplus power is charged to the decoupling capacitor by turning ON S_1. In mode II, after the switch S_1 turns OFF, the magnetizing current continues to be charged by switching ON S_2 till the energy is exactly equal to that required at ac side.

Tan *et al*. [23] combined the boost and flyback topologies to propose a new topology that is capable of implementing power decoupling with smaller capacitance, as shown in Fig. 17(a). As shown in Fig. 17(b), the energy stored in the decoupling capacitor C_2 is delivered to the grid through the forward converter as S_2 turns ON, while as S_1 switches ON, the source V_s charges to the inductor L_1 and when S_1 turns OFF, the energy stored

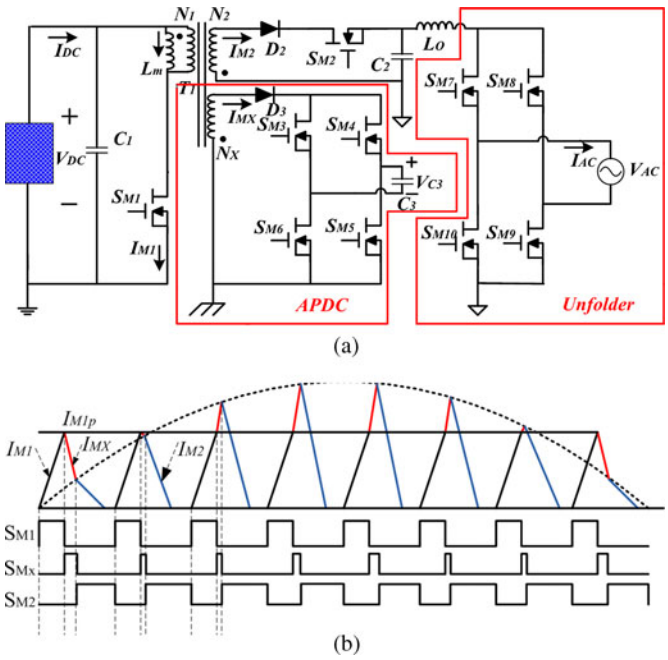

Fig. 15. (a) Topology proposed by Chen and Liao [21]. (b) Key waveform for topology in Fig. 15(a).

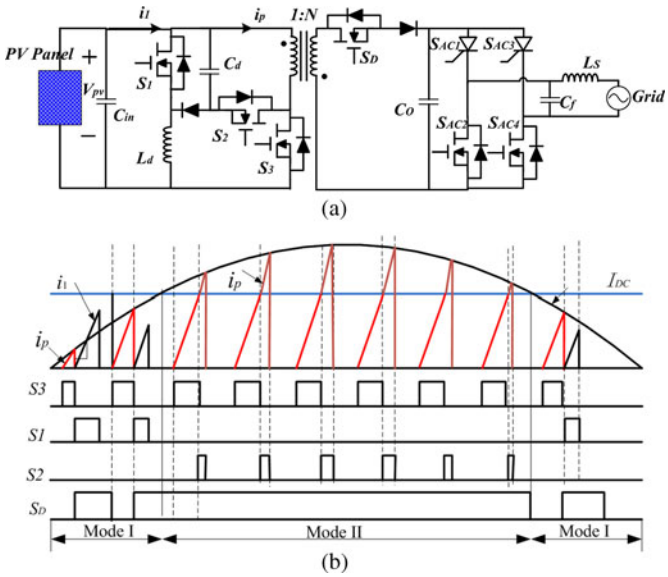

Fig. 16. (a) Topology proposed by Li *et al.* [22]. (b) Operation modes and driving signals.

in the inductor L_1 is transferred to the decoupling capacitor. It can be viewed as a two-stage power conversion with first stage for processing the dc power from PV, and the second stage for implementing the ac power modulation. Using this technique, the size of the decoupling capacitor will be reduced due to the relatively high voltage level and voltage ripple allowed across its terminals.

B. DC-Link Decoupling

For multistage microinverter design, the main power decoupling capacitor is placed at the high-voltage dc link, as shown

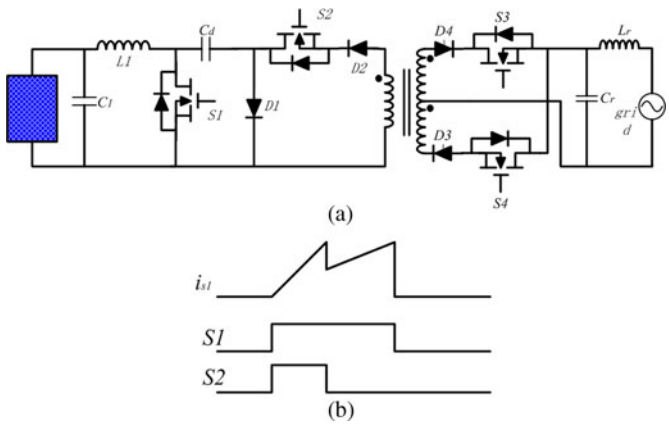

Fig. 17. (a) Topology proposed by Tan *et al.* [23]. (b) Key waveforms.

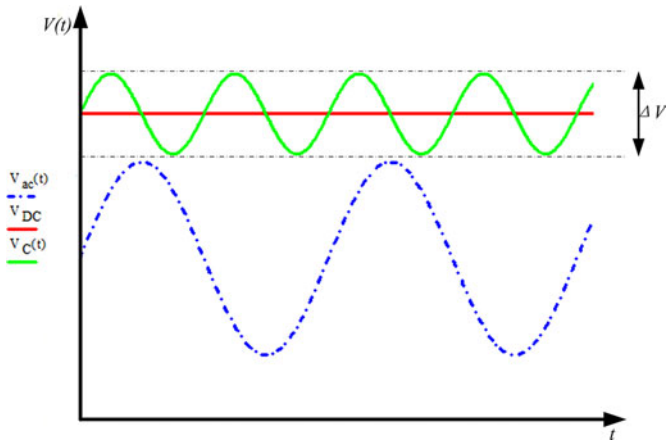

Fig. 18. DC-link voltage and the output ac voltage waveforms.

in Fig. 5(a). Unlike PV-side decoupling, where the PV nominal voltage is relatively low and the voltage ripple should be limited to a very small range to maximize the energy harvest from the PV, dc-link decoupling allows for a higher dc-link voltage as well as a higher voltage ripple voltage. Thus, this leads to a smaller decoupling capacitance according to (5).

Although increasing the dc-link level and voltage ripple leads to a reduced value of decoupling capacitance, the minimum voltage across its terminals must be higher than the peak value of the output voltage, as shown in Fig. 18 [24]. More specifically, the instant dc-link voltage must be greater than the ac instant voltage, as illustrated in Fig. 19, otherwise the inverter would malfunction. Detailed explanation and calculations on how to select the dc capacitance is given in [25]. The authors in [26] used this concept to minimize the dc-link capacitance in ac/dc application, and also proposed a third-harmonic injection method to further reduce the size of the capacitance by compromising the power factor and capacitance [27], [28].

Having a large voltage ripple across the dc link may result in deterioration of the output current waveform. To resolve this issue, several control techniques have been proposed. A simple method to mitigate the dc voltage ripple impact is to decouple the dc voltage, as proposed by Enjeti and Shireen [29], in which a modified modulation strategy to reject the dc-link voltage

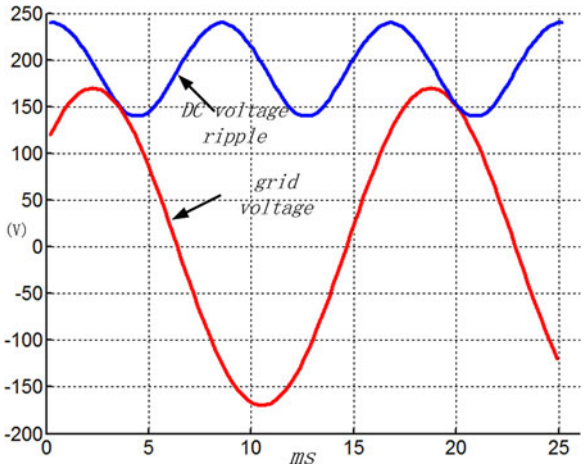

Fig. 19. Allowed maximum dc voltage ripples [24].

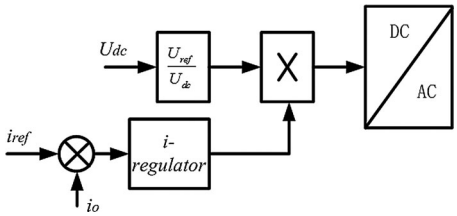

Fig. 20. Modulation technique proposed by Enjeti and Shireen [29].

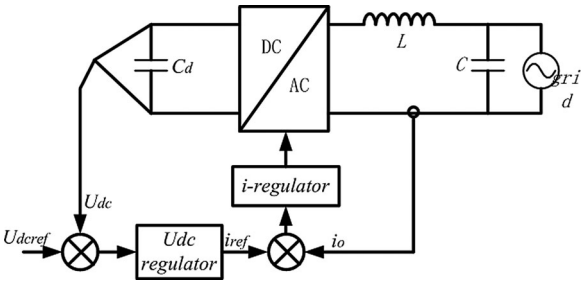

Fig. 21. Control scheme proposed by Brekken *et al*. [30].

ripple in the control system is proposed. The proposed control scheme is illustrated in Fig. 20. Brekken *et al*. proposed a control technique, shown in Fig. 21 [30], that allows for 25% ripple voltage without distorting the output current waveform. In this design, the voltage loop cutoff frequency was designed at 10 Hz, greatly attenuating the double line-frequency dc voltage ripple in the control loop. However, with such low cutoff frequency, the proposed control system definitely degrades the system dynamic performance.

To achieve a higher bandwidth for the voltage control loop, Ninad and Lopes proposed a dc voltage ripple estimation control strategy, as shown in Fig. 22 [31]. In the proposed strategy, no dc voltage ripple is fed to the dc voltage regulator. This is done by subtracting dc voltage from the estimated voltage ripple. The authors in [32] proposed a predictive dc voltage regulator, based on the power balance and the relationship between energy and dc capacitor voltage, to achieve low current distortion on the ac side and high voltage ripples across the dc bus. The detailed design on how to maintain the constant current drawn from PV

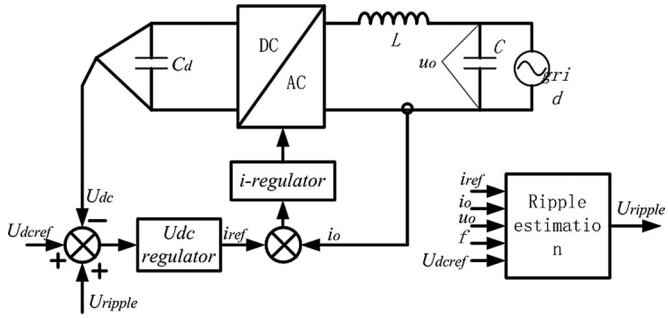

Fig. 22. Voltage-ripple estimation strategy for large dc ripple proposed by Ninad and Lopes [31].

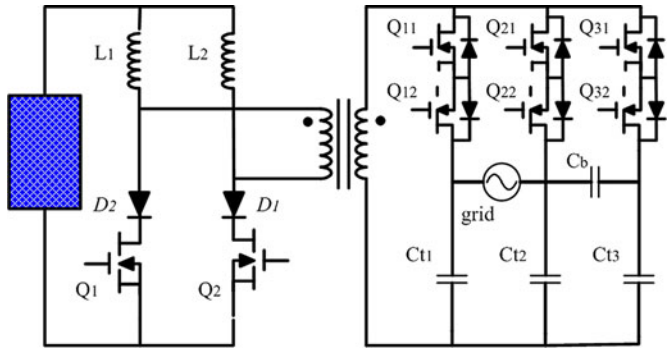

Fig. 23. Topology proposed by Li *et al.* [37].

source and push power to the grid with unity power factor, while allowing the 25% dc voltage ripples of the rated dc bus voltage, is presented in [33]. In this manner, the dc voltage regulator can achieve a faster transient response. The authors in [34]–[36] follow the same concept to allow the voltage ripple as large as possible, while making the injected current acceptable in terms of total harmonic distortion (THD).

C. AC-Side Decoupling

In ac-side decoupling techniques, the decoupling capacitor is usually embedded in the inverter stage itself. Because of the high voltage swing at the ac side, the capacitor value can be very small, and a nonpolarized (film) capacitor can be used. In topologies that employ this kind of decoupling, bidirectional switches are required to provide a path for the positive and negative currents. The possible integration of the bidirectional switch and its driver circuitry could simplify these topologies, and enhance the overall system reliability. Two topologies that employ ac-side decoupling are shown in Figs. 23 and 24 [37], [38]. The concept in both topologies is quite similar. An additional phase leg is added to the ac side to accommodate the decoupling capacitor between the inverter and the grid. Both topologies are based on the current source inverter implementation. The authors in [39] and [40] proposed a voltage source inverter with additional phase leg for compensating the pulsating power in single-phase ac/dc applications, as shown in Figs. 25 and 26. Although the topologies are different, the principle of power decoupling at the ac side is quite the same, and can be applied to dc/ac applications as well.

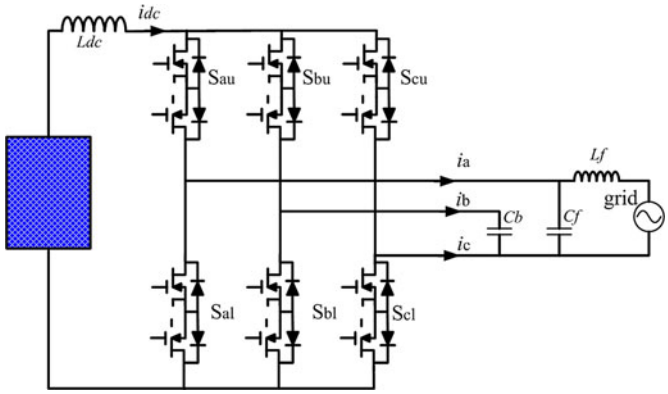

Fig. 24. Topology proposed by Bush and Wang [38].

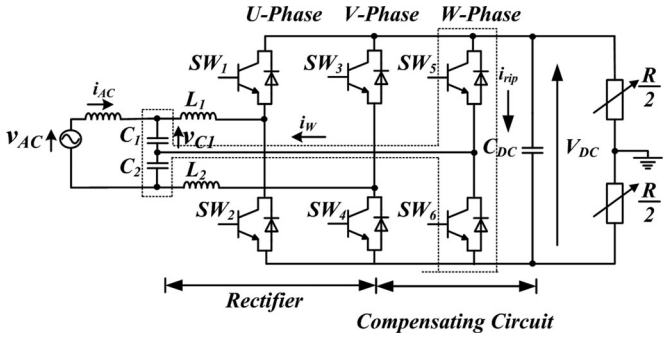

Fig. 25. Topology proposed by Shimizu *et al.* [39].

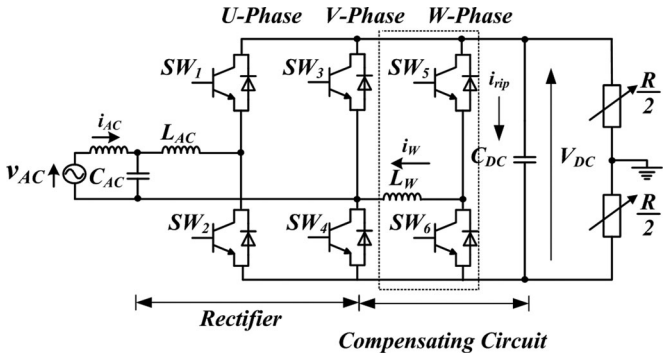

Fig. 26. Topology proposed by Tsuno *et al.* [40].

The aforementioned topologies, which employ ac-side decoupling technique, are a typical unbalanced three-phase system with three phase voltages and currents described as follows:

$$\begin{cases} u_a = U_a \sin(\omega t) \\ u_b = U_b \sin(\omega t + \varphi_{ub}) \\ u_c = 0 \end{cases} \tag{6}$$

$$\begin{cases} i_a = I_a \sin(\omega t + \varphi_{ia}) \\ i_b = I_b \sin(\omega t + \varphi_{ib}) \\ i_c = -i_a - i_b \end{cases} \tag{7}$$

where ω is the angular frequency of the grid, U_a, U_b, I_a, and I_b are the amplitudes of voltages and currents in phase a and b, respectively. φ_{ub} is the phase angle of phase b voltage, and φ_{ia} and φ_{ib} are the phase angle of phase a and b currents.

The total instantaneous power can be calculated as

$$\begin{aligned} P_{\text{total}} &= u_a i_a + u_b i_b + u_c i_c \\ &= \underbrace{\frac{U_a I_a \cos\varphi_{ia}}{2} + \frac{U_b I_b \cos(\varphi_{ub} - \varphi_{ib})}{2}}_{P_1} \\ &\quad \underbrace{- \frac{U_a I_a}{2}\cos(2\omega t + \varphi_{ia}) - \frac{U_b I_b}{2}\cos(2\omega t + \varphi_{ub} + \varphi_{ib})}_{P_2}. \end{aligned} \tag{8}$$

As indicated in (8), the first two terms, P_1, are constant, while the last two terms, P_2, are time-varying. To maintain the power P_{total} constant, the only solution is to make the sum of the last two terms, P_2, zero. Therefore, the following two constraints have to be satisfied:

$$\begin{cases} U_a I_a = U_b I_b \\ \varphi_{ia} = \varphi_{ub} + \varphi_{ib} + \pi. \end{cases} \tag{9}$$

Since only the capacitor is connected in phase b, the angles and amplitudes of voltage and current in phase b have the following constraints:

$$\begin{cases} \varphi_{ib} = \varphi_{ub} + \dfrac{\pi}{2} \\ I_b = \omega C U_b \end{cases} \tag{10}$$

where C is the power decoupling capacitance connecting to phase b.

Substituting the expression (10) into (9), we can draw the following constraints for power balance operation:

$$\begin{cases} I_b = \sqrt{\omega C U_a I_a} \\ \varphi_{ib} = \dfrac{1}{2}\left(\varphi_{ia} - \dfrac{\pi}{2}\right). \end{cases} \tag{11}$$

Based on these constraints (11), the control scheme can be calculated by using the symmetrical component method to decompose both positive and negative components.

IV. Performance Comparison of the Decoupling Circuits

The power decoupling techniques presented previously will impact the overall system reliability, cost, and efficiency. For the efficiency comparisons, we use η_0 as the conversion efficiency without the power decoupling circuit, while η_d is the efficiency of the added power decoupling circuit.

The power process in the grid-connected PV system with power decoupling circuit is shown in Fig. 27.The main inversion stage will process the total power from the PV module, while the power processed by the decoupling circuit would be at least the shadowed area in Fig. 3, whose power can be calculated as

$$P_{\text{decoupling}} = 4 f_{\text{grid}} \int_0^{\frac{1}{4 f_{\text{grid}}}} |P_{\text{dc}} - P_o| = \frac{2}{\pi} P_{\text{dc}}. \tag{12}$$

Based on the aforementioned assumptions on the efficiency, the overall efficiency with the decoupling circuit is expected to be $\eta_o - \frac{2}{\pi}(1 - \eta_d)$. Table I shows the comparison results of the

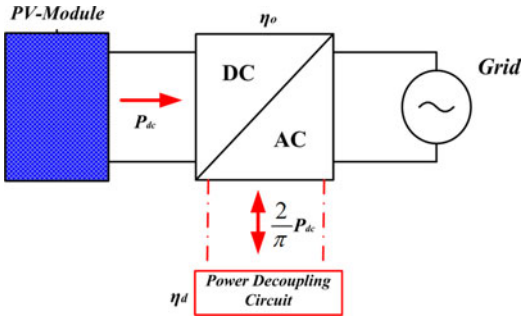

Fig. 27. Power process in the PV system with power decoupling circuit.

various decoupling techniques with respect to the size of decoupling capacitor, the added cost, the impact on the efficiency, and the decoupling control circuit complexity. For PV-side decoupling techniques, from an efficiency aspect, having the decoupling capacitor directly across the PV output terminals would be the best choice. However, the capacitance is quite large, which will increase the cost, reduce the power density, and shorten the lifetime. As for dc-link decoupling techniques, the cost is low due to the fact that no additional circuitry or only control is needed, and the efficiency will be relatively high. However, these techniques can only apply to the multistage inverter configurations with dc-link implementation. In the ac-side decoupling techniques, the capacitance can be very small due to the high voltage swing. However, another phase leg is added, which will increase cost, especially in the aforementioned two current-source based topologies which need bidirectional switches. This would negatively affect the overall efficiency and control complexity.

In order to have a more fair and conclusive comparison for these topologies, the loss and cost calculation have been done again using the same specifications: 100-W power rating, 60-V input voltage, 110 rms output voltage, 50-kHz switching frequency, and 46-μF decoupling capacitance. Using these specifications, the stresses on the semiconductors, for each topology, were roughly calculated. Then, the topology in Fig. 10 was selected as a comparison bench topology, and other topologies can be normalized to it.

To give a general comparison reference and avoid choosing the specific MOSFETS, diodes, and cores for different topologies, we assume that the diode loss, MOSFET loss, and core loss have following relationships.

For diode loss calculation

$$D_{\text{loss}} = \left(0.7 + 0.1\frac{V_{\text{stress}}}{V_{\text{stress\_base}}}\right) \times I_{\text{rms}}. \tag{13}$$

For switch loss calculation (define $S_{\text{VA}} = I_{\text{stress}} \times V_{\text{stress}}$)

$$S_{\text{loss}} = \frac{S_{\text{VA}}}{S_{\text{VA\_base}}} \times S_{\text{loss\_base}}. \tag{14}$$

For inductor and transformer loss

$$T_{\text{loss}} = \frac{T_{\text{VA}}}{T_{\text{VA\_base}}} \times T_{\text{loss\_base}} \tag{15}$$

where

I_{rms} the RMS current through the diode;
V_{stress} voltage stress across the MOSFET or diode;
I_{stress} the current stress through MOSFETS;
$S_{\text{loss\_base}}$ MOSFET base losses;
$T_{\text{loss\_base}}$ transformer or inductor base losses;
T_{VA} the capacity of the reactive component.

Then, knowing that the power processed by MOSFETs, inductors, or transformers is different from one topology to another, the power losses for these components are proportionally related to the amount of the power processed by them, and the power losses can be adjusted as follows:

$$S_{\text{loss\_}SX} = \frac{P_{SX}}{P_{S\_\text{base}}} \times \frac{S_{\text{VA}}}{S_{\text{VA\_base}}} \times S_{\text{loss\_base}} \tag{16}$$

$$T_{\text{loss}} = \frac{P_{TX}}{P_{T\_\text{base}}} \times \frac{T_{\text{VA}}}{T_{\text{VA\_base}}} \times T_{\text{loss\_base}} \tag{17}$$

where P_{SX} and P_{TX} represent the power processed by the switch and passive component (transformer and inductor), respectively, while the P_{s_base} and P_{T_base} are the powers processed by S_1 and transformer T_1 in [17] as base values. Table II shows the normalized comparison results for the topologies with power decoupling at PV side based on the aforesaid assumptions. Then, by taking into consideration voltage stresses, current stresses, and power ratings, the losses can be estimated using the following expression:

$$P_{\text{loss\_total}} = \sum D_{ix\_\text{loss}} + \sum S_{ix\_\text{loss}} + \sum T_{ix\_\text{loss}}. \tag{18}$$

V. Discussion

In single-stage microinverter designs, power decoupling circuits can reduce the size of the required energy storage capacitor, thus improving the inverter lifetime, which is a much desired feature for ac-module PV system. However, the power decoupling circuit will result in additional power losses, due to the power flow through the decoupling circuit, consequently, reducing the overall efficiency. Although the power decoupling circuit may increase the total system cost due to the additional circuitry required, the extended lifetime eliminates the reoccurring cost of inverter replacement that haunts current PV system return on investment. To reduce the decoupling circuit power loss, the power processed by the decoupling circuit should be minimal and limited to $^2/_\pi P_{\text{dc}}$. Furthermore, to reduce the cost of decoupling circuit and achieve high conversion efficiency, the three-port converter with features of low component count, high integration, and high conversion efficiency is believed to be one of the best choices, with one port implementing MPPT and a second port dedicated to power decoupling. Recently, many three-port converters have been proposed to interface a renewable system.

Following are two examples that use a third port to realize the power decoupling, as shown in Figs. 28 and 29 [41], [42]. As shown in Fig. 28(b), the constant power from PV is controlled by the switch S_1 and in mode I, the power to be pumped to the grid is controlled by S_4, while the surplus power from PV is charged to the decoupling capacitor through the magnetizing inductor of the transformer. In mode II, the deficit power is supplied to

TABLE I
PERFORMANCE COMPARISON OF THE VARIOUS POWER DECOUPLING TECHNIQUES

Decoupling techniques		***Power rating(W)***	***decoupling capacitor***	***Additional Cost***	***Theoretical Efficiency***	***Experimental/calculation efficiency***	***Control Complexity***
PV side Decoupling	Fig.4	200	13.9mF	Capacitor	η_0	-	No control
	Fig.7	70	100uF	Capacitor+2 switches+1 inductor	η_0-2/π(1- η_d)	-	Active filter control
	Fig.8	100	40uF	Capacitor+1 switch	η_0-2(1- η_d)	70%	Peak current control
	Fig.9	156	314uF	Capacitor+2 switches	η_0-2(1- η_d)	86.7%	Peak current control
	Fig.10	100	46uF	Capacitor+1 Switch +3 Diodes	η_0-2/π(1- η_d)	90.6%	Discontinuous current control +Power balance control
	Fig.11	100	46uF	Capacitor+1 Switch +2 Diodes	η_0-2/π(1- η_d)	-	Power balance control
	Fig.12	500	50uF	3 switches+1capactitor+1 inductor +1 diode	η_0-2/π(1- η_d)	-	Discontinuous current control +Power balance control
	Fig.13	100	44uF	1 capacitor +1 switch+ 1 diode	η_0-2/π(1- η_d)	73%	Discontinuous current control +Power balance control
	Fig.14	200	40uF	4 switches+ 1 diode+1 capacitor +1 winding	η_0-2/π(1- η_d)	-	Power balance control
	Fig.15	100	40uF	2 switches +1 inductor+1diode+1capacitor	η_0-2/π(1- η_d)	-	Power balance control
	Fig.16	500	50uF	Capacitor+1 switch+1 inductor	$\eta_0 * \eta_d$	-	control for Boost +Flyback
DC side Decoupling	Fig.19	-	-	Capacitor	η_0	-	DC voltage Feed-forward control
	Fig.20	200	15uF	Capacitor	η_0	-	Low voltage loop bandwidth
	Fig.21	100	500uF	Capacitor	η_0	--	Voltage ripple estimation
AC side Decoupling	Fig.22	100	5.53uF	Capacitor+2 switches	η_0-2/π(1- η_d)	-	three-phase current modulation
	Fig.23	-	-	Capacitor+2 switches	η_0-2/π(1- η_d)	-	Modified three-phase current modulation
	Fig.24	100	165uF	2 switches+ capacitor	η_0-2/π(1- η_d)	-	Three-phase voltage modulation
	Fig.25	1000	-	2 switches+ 1 Inductor	η_0-2/π(1- η_d)	~94%	Three-phase voltage modulation

TABLE II
NORMALIZED COMPARISONS FOR THE TOPOLOGIES WITH POWER DECOUPLING CIRCUITS

Topologies	Component(Voltage, current stresses, processed power, and reactive power)	Power device losses(W)	Passive component losses(W)
Fig.7(a)	S1,S2(170V,2.12A, 127.2W,-);L(60V, 2.12A,63.6W,127.2 VA)	0.4(1)	0.38(1)
Fig.8(a)	S1(170V, 10A,100W,-);S2(340V, 4A,100W,-);S3,S4(596V, 5.4A,100W, -);D1(110V, 1.67A,-,-) ;D2,D3(596V,0.9A,100W);T(60V,10A,200W,600VA)	7.32	3.63
Fig.9(a)	Ssync, SBB (170V, 10A, 100W,-);S1,S2(170V, 4A, 100W,-); D1,D2(170V,0.667A ,-,-);D3, D4(594V,0.9A,-,-); S3,S4(594V, 5.4A,100W),T(60V,10A,200W,600VA)	8.52	3.63
Fig.10	D1(170V,0.424A,-,-,-); D2(25V,1.67A,-,-);D3(170,~0A,-,-); D4,D5 (311V, 0.9A,-,-,-);S1(170V,6.6A, 163.6W,,-);S2(170V,6.6A, 63.6W,-); S3,S4 (311V, 3.6A, 100W,-);T(60V,6.6A,163.6W,396VA);Lr(110ac,0.9A,100W, 100VA)	5.0	1.2
Fig.11	D1(170V,0.424A,-,-,-); D2(110V,1.67A,-,-,-);D3,D4(594V, 0.9A,-,-,-); S1 (170V, 13.2A, 163.6W,-); S2(170V,13.2A, 63.6W,-); S3,S4(594V,3.6A,100W,-);T(60V, 13.2A,163.6W,792VA);	8.46	1.2
Fig.13(a)	SM1, SM2(120V, 1.67A,163.6W,-); Sx1,Sx2(340V,0.37A,63.6W,-);Sx0(170V, 1.06A, 63.6W,-);D1(110V, 0.37A,-,-); D2-D5(200V,0.9A,-,-); T(60V,1.67A,100W,100VA); Lx(60,2.12A,63.6W,127.2VA)	3.52	0.28
Fig.14(a)	SM:(230V, 6.67A,100W,-); Sx:(170V,6.67A, 63.6W,-); Dx(230V,1.06A,-,-); DM :(110V, 1.67A,-,-);DAC1-DAC2: (594V, 0.9A,-,-);SAC1-SAC2:(594V, 3.6A,100W,-); Tr(60V,6.6A,163.6W, 396VA);	6.65	2.3
Fig.15(a)	SM1: (120V, 6.67A,100W-);D2:(311V,0.9A,-,-); D3(170V, 0.424A ,- ,-) ; SM3-SM6: (170V,1.49A,63.6W,-);T1(60, 6.67A, 163.6W, 396VA)	2.37	1.2
Fig.16(a)	S1(110V,4.24A, 63.6W,-);S2(230V, 1.69A,63.6W,-); S3(120V ,6.67A ,100W ,-) ; D1(110V , 0.424A, -, -); SD(596V, 3.6A, 100W,-); D2(594V, 0.9A ,- ,-) ;T(60V,6.67A,100W,396VA); L(60V,2.12A,63.6W,127.2VA)	4.08	1.45
Fig.17(a)	S1(170V, 8.67A, 300W, -);S2(311V, 5.33A,100W,-); D2(311, 0.667A , -,-);D3,D4(311V, 0.9A,-,-);S3,S4(311V, 3.6A, 100W, -) ;L1 (60V, 3.34A, 100W, 200VA);T(150V,2.67A,100W, 400.5VA)	7.22	2.27

(1) Since in this topology only the decoupling circuit is given, the losses are only for the decoupling circuit.

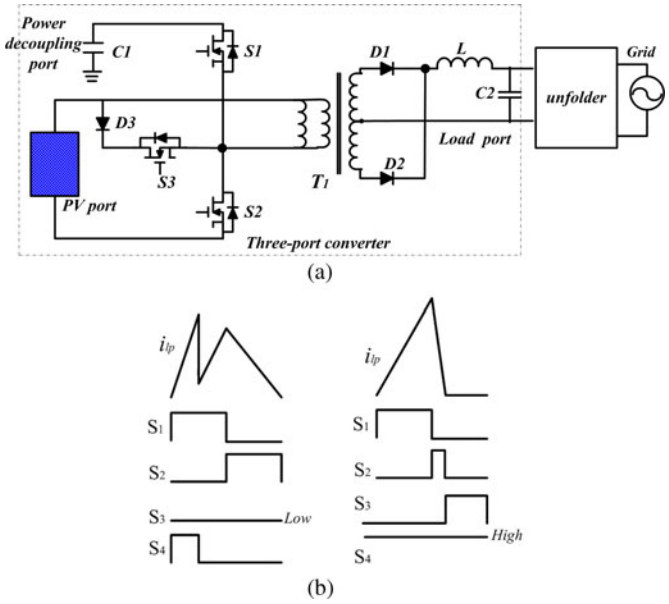

Fig. 28. (a): Integrated three-port inverter with power decoupling capability proposed by Qian *et al.* [41]. (b) Driving strategy for topology in Fig. 28(a).

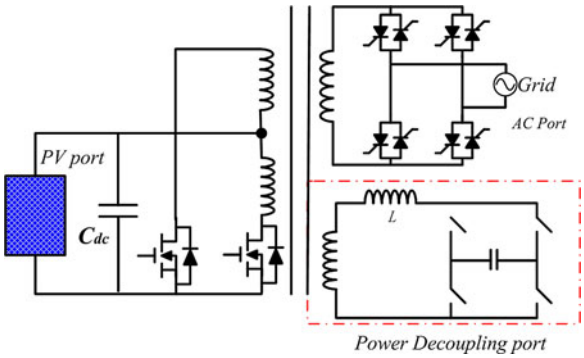

Fig. 29. AC-link implementation of a three-port converter proposed by Krein and Balog [42].

the ac grid by turning ON S_2. The authors in [42] only gave the conceptual description on the proposed topology. Careful design should be considered and additional circuits are necessary to controllably distribute the power for the two secondary windings.

Also, the topology proposed by Liu and Hui can be tailored to implement power decoupling function for microinverter, as shown in Fig. 30(a) [43], where the area marked by blue line is added to realize the microinverter functions. To distribute the power among different ports, a phase-shift control scheme is employed, as shown in Fig. 30(b). More detailed control strategy studies should be carried out to both implement power decoupling and pump the sinusoidal current to the grid.

As a result, many three-port topologies, as shown in Figs. 31 and 32, can be candidates for the microinverter topology with the power decoupling capability [44]–[52]. Topologies in Fig. 31 are derived from conventional topologies by adding a few reactive components, whose cost is relatively low and power density is expected to be high. Fig. 31(e) shows the energy allocation for each port in one switching cycle. The energy from PV source

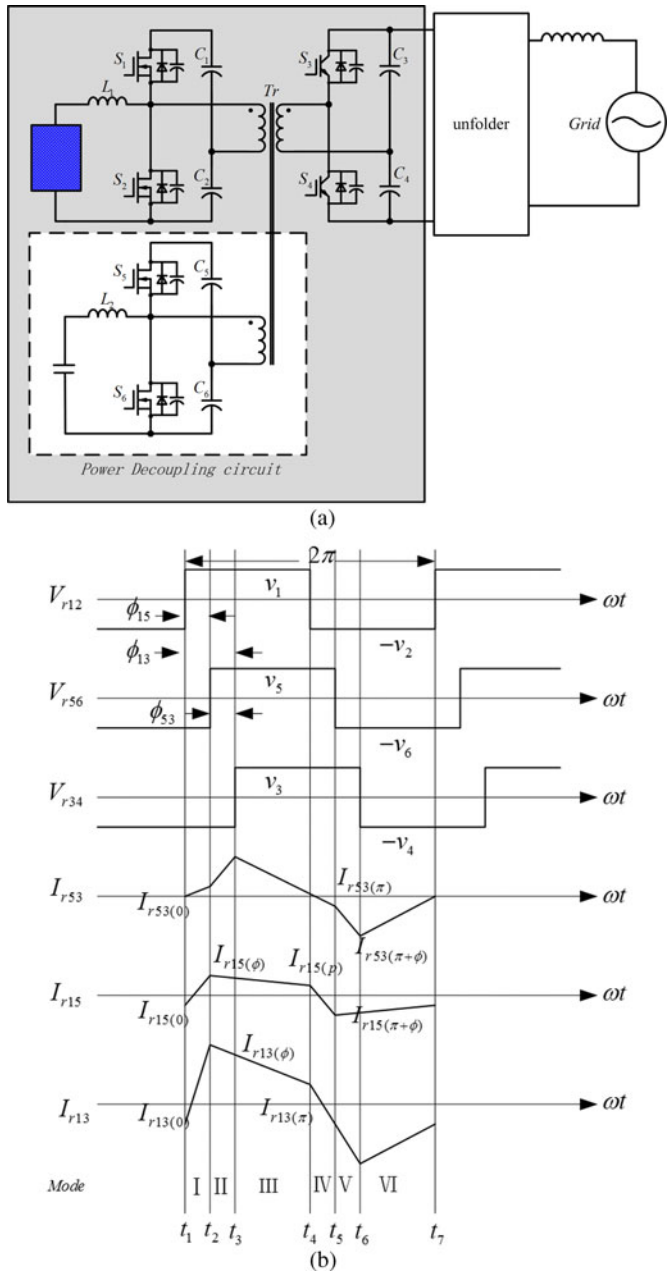

Fig. 30. (a) Topology in shadowed area proposed by Liu and Hui [43]. (b) Phase shift control strategy for power distribution.

is divided into two parts: 1) the first part is charged to the decoupling capacitor through the inherited boost converter at primary side; (2) the second part is charged to the ac side. In this period, to balance the transformer's magnetizing current, the energy from both PV and the power decoupling capacitor should be same. The power from PV source is partially pumped to the decoupling capacitor and partially combines with the power from decoupling capacitor to form the sinusoidal power with dc bias at the ac side.

Topologies in Fig. 32 use high-frequency transformer as an intermediate to interface different power ports, where both active switches and reactive components are required to implement power decoupling, which may lead to high cost. The main idea

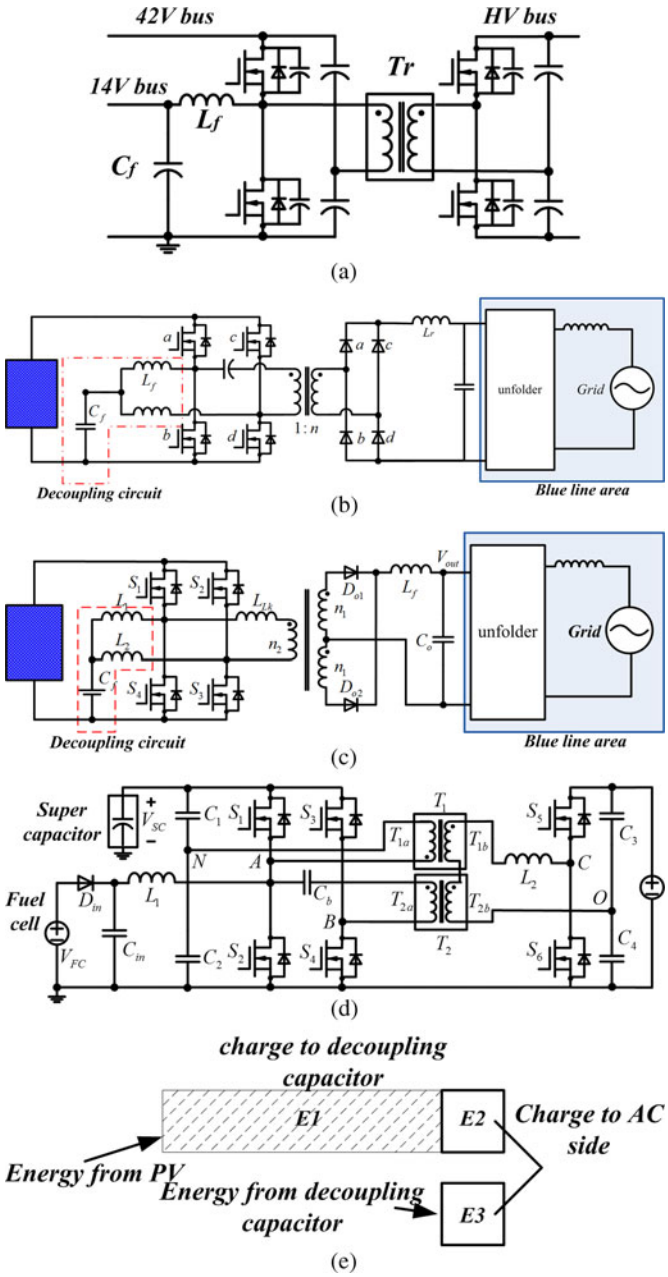

Fig. 31. Topologies by integrating power decoupling circuit with conventional topology. (a) Topology proposed by Su and Tang [44]. (b) Topology proposed by Al-Atrash and Batarseh [45]. (c) Topology proposed by Li *et al.* [46]. (d) Topology proposed by the authors in [47] and [48]. (e) Energy allocation for the topologies in this figure.

of the control strategies for these topologies is quite same. They use the phase shift control strategies to allocate the power for each port, as shown in Fig. 32(e). The power P_{12} (denoted as a power flows between ports 1 and 2) is a function of phase shift φ_{12}, so do the powers P_{13} and P_{23}. According to this power allocation principle, the power decoupling control strategy for each topology can be designed and developed correspondently.

In ac–dc LED driver applications, where LED needs constant power from ac grid, many research works have been proposed to eliminate the electrolytic capacitor, and use a high-reliability capacitor technology instead to extend its lifetime, as shown

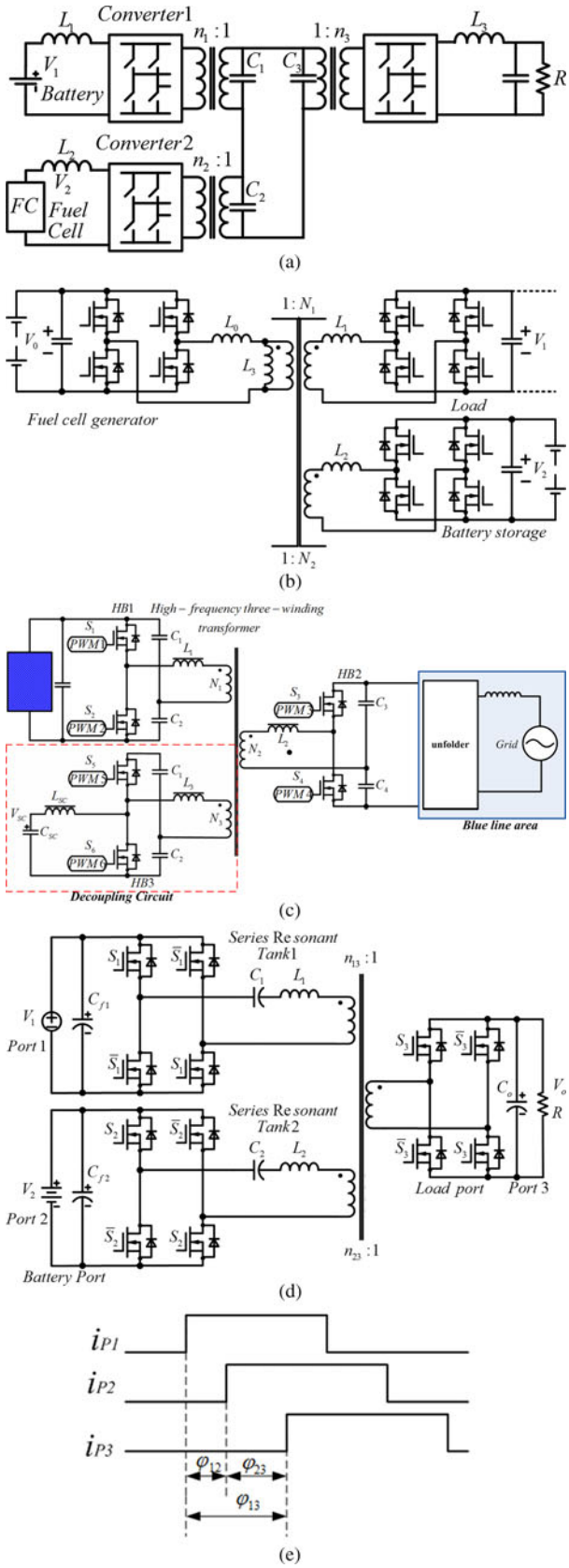

Fig. 32. Topologies with power decoupling function by adding a third port through high-frequency transformer. (a) Topology proposed by Krishnaswami and Mohan [49]. (b) Topology proposed by Duarte *et al.* [50]. (c) Topology proposed by Tao *et al.* [51]. (d) Topology proposed by Tao *et al.* [52]. (e) Phase shift control strategy.

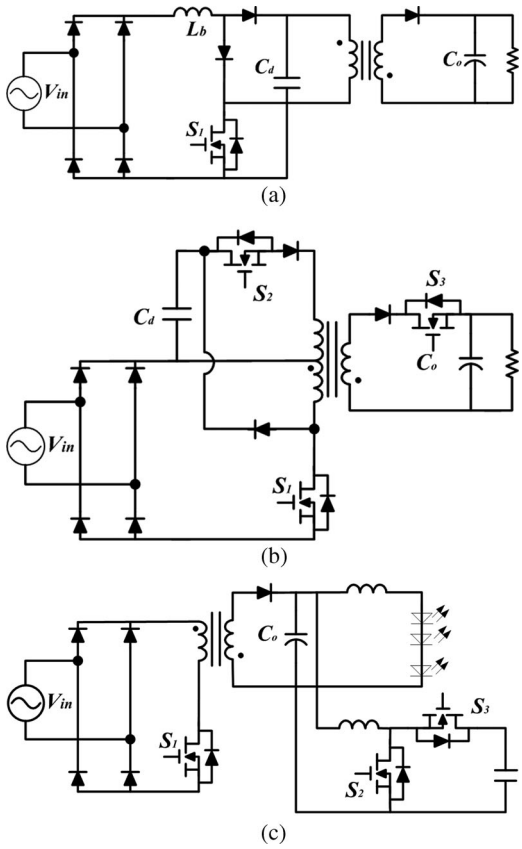

Fig. 33. Topologies used in ac/dc application without electrolytic capacitor. (a) Topology proposed by Zhang *et al.* [53]. (b) Topology proposed by Chen and Hui [54]. (c) Topology proposed by Wang *et al.* [55].

in Fig. 33 [53]–[55]. Although the operation principles are different among these flyback-based topologies, the main idea is the same. The input power from the grid is time varying and the constant power is required at LED load side. Thus, the power decoupling circuit is required to buffer the imbalanced power between input and output. When the instantaneous input power from the grid is low, the decoupling capacitor supplies the deficit, while the input power is high, the surplus power is stored to the decoupling capacitor. For more detailed operation principles, refer to these references.

A systematic derivation of the three-port converters is given, as shown in Fig. 34 [56]. All these topologies can be tailored to realize single-phase inverter with power decoupling capability, which could be a future trend for electrolytic capacitor-less microinverter. All these derived topologies are based on the half-bridge converter. The primary magnetizing inductor serves as a boost inductor to configure the power path from PV source to the decoupling capacitor, while the amount of the power to be delivered to the load can be controlled by switch S_3 or/and S_4.

For multistage microinverter designs, which incorporate a dc link, the power decoupling employing a high-voltage dc-link capacitor may be the best choice for its simplicity, low cost, and high efficiency. To reduce the decoupling capacitance, a higher dc-link voltage as well as a higher voltage ripple can be used with the constraint that the lowest dc-link voltage should be greater than or equal to the peak grid voltage. To mitigate the effect of large dc voltage ripple on the grid current and achieve

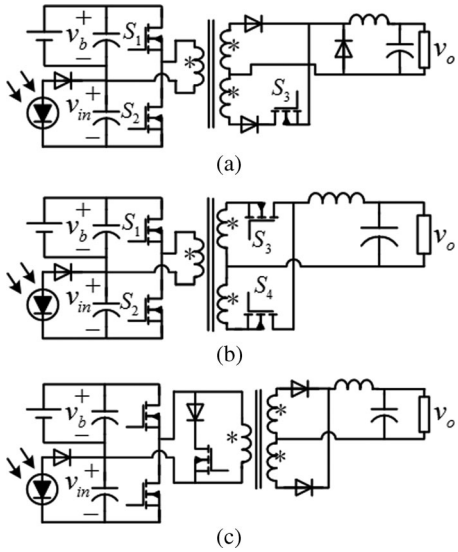

Fig. 34. Topologies derived by Wu *et al.* [56].

the good dynamic responses, sophisticated control strategies should be employed.

The smallest decoupling capacitance can be achieved by ac-side decoupling techniques; however, due to the need for using bidirectional switches or a third switch leg, this could lead to an increase in the cost of the microinverter as well as the control complexity, and reducing the overall efficiency.

VI. Conclusion

The reliability of the microinverter is becoming a crucial feature in the ac-module PV system. Recently, many research works have been proposed to improve its reliability by using high-reliability decoupling capacitor techniques. This paper reviews various power decoupling techniques that have been employed in a single-phase microinverter to reduce the size of the energy storage capacitor and improve the inverter life expectancy. Conventionally, for single-stage inverters, the decoupling capacitor is placed across PV panel terminals resulting in a large size capacitor. PV-side power decoupling circuits can be employed to reduce the capacitor size. However, the overall inverter efficiency is negatively affected. Three-port converters may offer better alternatives for single-stage inverters due to their lower cost and higher efficiency. For multistage microinverter topologies with dc link, the dc-link capacitor offers the best alternative for power decoupling. However, sophisticated control strategies should be employed to allow for higher voltage ripple and to maintain the low current THD injected to the grid, and thus reducing the size of the dc decoupling capacitor. Finally, ac-side decoupling involves incorporating a third phase to implement the power decoupling, where a very small capacitance is required, but the control complexity is increased dramatically.

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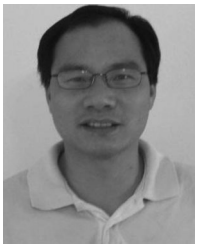

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