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Low cost and highly reliable radiation hardened latch design in 65 nm CMOS technology ☆

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ABSTRACT

As a consequence of technology scaling down, gate capacitances and stored charge in sensitive nodes are decreasing rapidly, which makes CMOS circuits more vulnerable to radiation induced soft errors. In this paper, a low cost and highly reliable radiation hardened latch is proposed using 65 nm CMOS commercial technology. The proposed latch can fully tolerate the single event upset (SEU) when particles strike on any one of its single node. Furthermore, it can efficiently mask the input single event transient (SET). A set of HSPICE post-layout simulations are done to evaluate the proposed latch circuit and previous latch circuits designed in the literatures, and the comparison results among the latches of type 4 show that the proposed latch reduces at least 39% power consumption and 67.6% power delay product. Moreover, the proposed latch has a second lowest area overhead and a comparable ability of the single event multiple upsets (SEMUs) tolerance among the latches of type 4. Finally, the impacts of process, supply voltage and temperature variations on our proposed latch and previous latches are investigated.

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1. Introduction

With the technology scaling down, circuits have become more and more sensitive to radiation, which make the reliability issue of circuits become one of the major concerns for circuit designers [1]. Due to the reduction of supply voltage and node capacitance, the amount of charges that can be stored on a node is also reduced, making the circuit susceptible to particle-induced charge. When the amount of accumulated particle-induced charge is high enough, a transient fault will appear as an electrical pulse which is called a single event transient (SET). In addition, the current induced by a particle hit always flows from n-type diffusion to p-type diffusion through a p–n junction [2,3]. It means that if a latch is made up of only PMOS transistors, a radiation particle strike cannot flip the node voltage from 1 to 0; vice versa, if only NMOS transistors, the node voltage cannot flip from 0 to 1 [4]. If an SET propagates through the combinational logic circuits and once be latched by the downstream sequential logic cell such as memory cell or latch, a single event upset (SEU) will happen, which causes the stored value to be incorrectly flipped in memory cell or latch. For memory cells, error correction codes (ECC) [5–9] can be used at low cost to tolerate SEUs due to particle strike. However, latches are integrated into the logic and widely spread across the chip, ECC cannot be employed [10].

Researchers devote to harden latches by adding additional transistors to its basic circuit structure, and many radiation harden latches have been proposed [11–18]. We can classify these latches (will be discussed in details in Section 2) into four different types similar to [12,18]. The first type (type 1) of latches are those that they have more capability of tolerating SEU than traditional latches, but they are not fully SEU immune. In other words, these latches have one or more nodes to which an energetic particle strikes, could corrupt their latched value. The latches designed in [11,12] are of type 1. The second type (type 2) of latches are those that they can fully tolerate SEU when particles strike on any one of its single node, but they cannot filter out the input SET and its output node will take a high impedance state when a particle strikes on some of their internal single node. The latches designed in [13, 14, HLR, 15] are of type 2. Type 3 latches are those ones that they are fully SEU immune when particles strike on any one of their single node and their output nodes will not take high impedance states, but they cannot filter out the input SET. The proposed latches in [14, HLR-CG1 and HLR-CG2, 16, 17, FERST] are of type 3. Type 4 latches are those ones that they are fully SEU immune when particles strike on any one of their single node and the output nodes will not take high impedance states; they can filter out the input SET,

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too. The proposed latches in [17, Enhanced version of FERST mentioned as EVFERST here, 18] are of type 4.

In this paper, we propose a low cost and highly reliable radiation hardened latch which is belong to the category of type 4. Simulation results are carried out by means of HSPICE with 65 nm CMOS commercial technology. Compared with previous type 4 latches, the proposed latch has a much better performance in terms of power, D to Q delay and power delay product (PDP), and has a second lowest area overhead as well as a comparable ability of single even multiple upsets (SEMUs) tolerance. The impacts of process, supply voltage and temperature variations on proposed latch are also analyzed.

The remaining of this paper is organized as follows: Section 2 gives a review of previous hardened latch designs. In Section 3, the proposed low cost and highly reliable hardened latch is discussed. Simulation results of both the proposed latch and previous latches are shown in Section 4. Section 5 investigates the impact of process, supply voltage and temperature variations on the proposed latch. Section 6 concludes this paper.

2. Previous works

The latches designed in [11,12] are of type 1. As shown in Figs. 1 and 2, both latches are based on the hysteresis property of Schmitt trigger circuit (S) and time redundancy to tolerate SET. The latches in [11,12] are more reliable than traditional latches, but as mentioned in Section 1, they are not fully immune. For example, the latch designed in [11] may upset when an energetic particle strikes on its node int1 or even strikes on its output node Q, while the latch designed in [12] may also upset when an energetic particle strikes on its node nq.

In order to solve the problems mentioned in type 1 latches, the latch designed in [13], belonging to type 2, has been proposed and is shown in Fig. 3. Compared with type 1 latches, the latch designed in [13] can guarantee not to be affected by any single node particle strike, but it does not have the ability of input SET filtering. Besides, if an energetic particle strikes on its node int5 (or int6), nodes int1 and int2 (or int3 and int4) may both upset, making int5 (or int6) a permanent flip. Then the value stored on node int5 becomes opposite to the value stored on node int6 which results in a high impedance state on output node Q. Further improvements have been made in type 3 latches [14, HLR-CG1 and HLR-CG2, 16, 17, FERST]. They can tolerate any single node particle strike and can prevent the output nodes from taking high impedance states. However, they cannot filter out input SET.

To solve above problems, three robust latch structures have been designed in [17, EVFERST, 18], which are of type 4, shown in Figs. 4 and 5. Those latches are the most reliable latches due to their toleration of any single node particle strikes and ability to filter out input SET, as well as the feature to not take a high impedance state at output node. However, the latch designed in [17, EVFERST] has a massive amount of transistors resulting in high power consumption and large area; latches proposed in [18] have active feedback loops when they work at their transparent modes, which also lead to high power consumptions.

In addition, all the latches discussed above suffer from the problem of having active feedback loop to some extent when work at their transparent modes, which would increase power consumptions. This problem will be properly solved by our proposed latch which is of type 4, shown in Section 3.

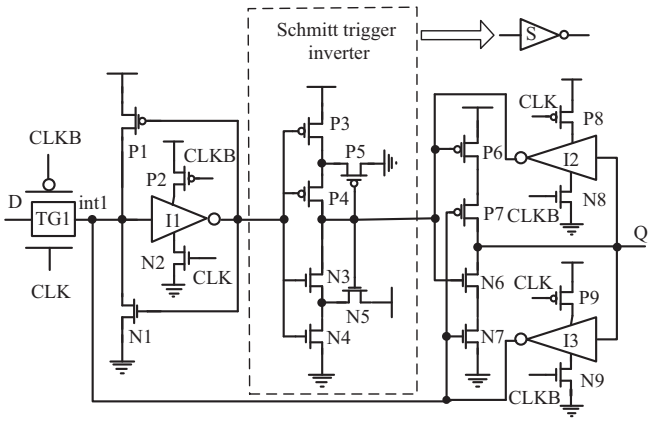

Fig. 1. Hardened latch proposed in [11].

3. Proposed hardened latch design

The proposed latch shown in Fig. 6 overcomes the defects mentioned in Section 2 by reasonable structure design, which allows designers to cut off all the loops when works at its transparent mode. By using clocked inverters in all feedback loops and clocked C-element, power consumption is reduced. Besides, the proposed latch can reuse its part3 to attain the capability of SET tolerance and prevent the output node from taking its high impedance state. While, the functions of tolerating SET and preventing high impedance state are implemented by two parts in LSEH-1 latch, this means C-element in LSEH-1 latch has to work actively all the time, which would increases power consumption.

In this proposed latch structure, the input node D is separated into three nodes, which form three paths. Two of these paths are finally applied to the input nodes of C-element through part1 and part2, separately; another one is finally applied to the output node Q of C-element through part3. In this way, when CLK signal takes its one value, the transmission gates TG1, TG2 and TG3 are turned on and the latch works at its transparent mode. D propagates to Q through Schmitt trigger circuit (S), internal node int1 and int4 are connected to node D through TG1 and TG3, respectively. Internal node int3 is driven by node D through TG2 and inverter I3 in order. The inverters I2, I5, I6 and C-element are turned off by the clock signal, in other words, all feedback loops are cut off, including C-element. If the input contains an SET in its transparent mode, the SET pulse will be filtered out due to the hysteresis property of Schmitt trigger circuit (S).

When the CLK signal takes its zero value, the transmission gates TG1, TG2 and TG3 are turned off, the inverters I2, I5, I6 and C-element are turned on, which makes each feedback loop actively and C-element work normally, the latch works at its hold mode. Then, part3 is isolated from input node D, while it is still connected to the output node Q, this can prevent the output node from taking a high impedance state when particles strike on any one of its internal node. That is to say, the part3 can not only filter out input SET in its transparent mode, but also guarantee the output node Q not to take a high impedance state in its hold mode. Therefore, the proposed latch fulfills the reuse of part3.

In the hold mode, the three keepers of part1, part2 and part3, hold the latched value. If node int1 (or int2) is affected by an energetic SET, part1 will upset due to its positive feedback structure, however, this error cannot propagate through the C-element because part2 holds their original values, in other words, the output node Q will not be affected and not be a high impedance state because of part 3; in the same way, if the node int4 (or int5) is affected by the strike of an energetic SET, the output node Q will not be affected, either; if node Int3 is affected by SET, because of the hysteresis property of Schmitt trigger circuit (S), output can hardly be affected, even if output node Q is flipped directly by an energetic SET or indirectly by int3, the output node Q will be

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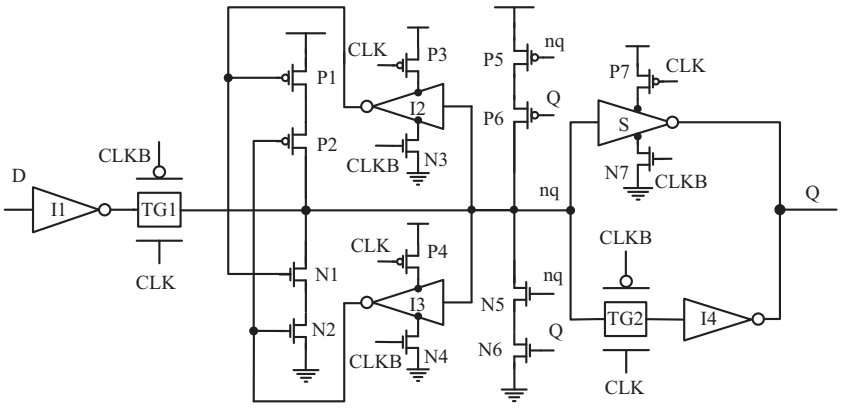

Fig. 2. Hardened latch proposed in [12].

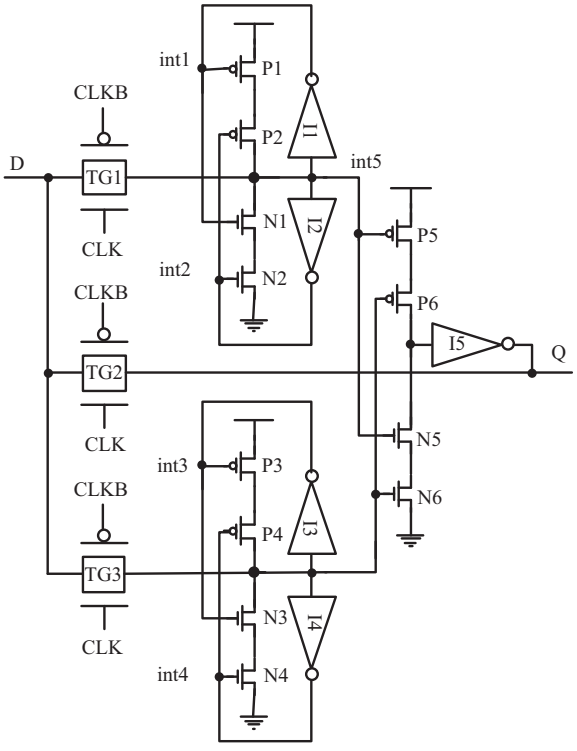

Fig. 3. Hardened latch proposed in [13].

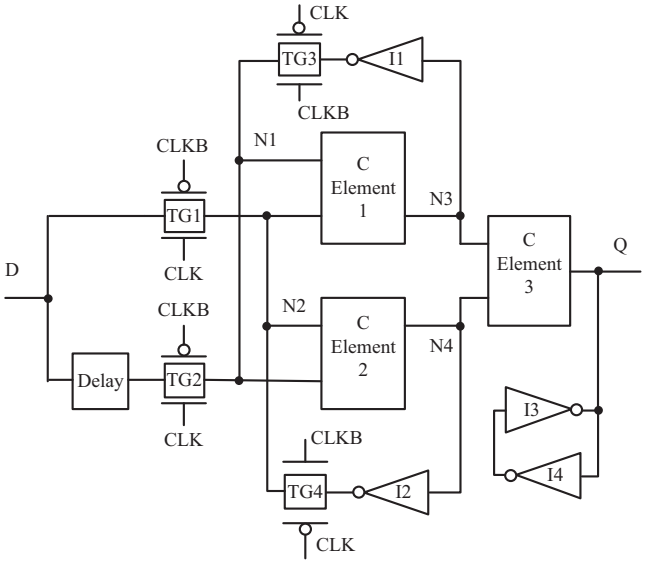

Fig. 4. Enhanced version of FERST proposed in [17].

corrected by int2 and int5 which hold their original values, and only a glitch may appear at the output node. To summarize, our proposed latch can fully tolerate SEU on any one of its single node.

In Figs. 7 and 8, an SET is injected to internal node int1 and int5 separately, and the model employed for SET injection is an exponential current source which will be introduced in details in Section 4. As shown in Fig. 7, a particle strikes on node int1 results in node int2's upset, but it cannot affect the output node Q, because node int5 is at its original state; accordingly, in Fig. 8 if a particle strike on node int5, it will result in node int4's upset, and this upset will not propagate through C-element, either, because of the original state held by node int2. So it can be concluded that any particle strike on single node int1, int2, int4 or int5 cannot affect the output node Q, which verifies the theoretical analyses above.

Fig. 9 shows the results that a particle strikes indirectly on node int3 or directly on output node Q, it indeed can make the output node Q upset. However, it will come back to its original state after the strike, because int2 and int5 hold their original states, which means that a particle strike on node int3 or node Q can affect the output node only by imposing a glitch on it and the output will come back to its original state, which also verifies the theoretical analyses. Fig. 10 shows the simulation results of the SET masking capability of our latch, it can be seen that a smaller width of the input SET can be filtered out completely, and the maximum width of filtered input SET will be given in Section4. Fig. 11 shows the layout of the proposed hardened latch.

4. Latch evaluation and comparison

In this section, a traditional latch shown in Fig. 12 is added as a reference latch. All the following simulations in this section are HSPICE post-layout simulations using 65 nm commercial technology with 1.2 V power supply at room temperature (27 °C). For a fair comparison, minimal area design rule is applied for all latches, which means the minimum possible transistor sizes making the latches work properly are utilized. According to the ratio of PMOS and NMOS in [11] and considering the difference of the mobility between PMOS and NMOS, the minimal gate widths/lengths of PMOS and NMOS transistors are set to 300 nm/60 nm and 120 nm/60 nm, respectively. However, the HLR-CG1 latch designed in [14] is an exception, the PMOS and NMOS of its DICE storage cell are all set to 120 nm/60 nm. In addition, the authors

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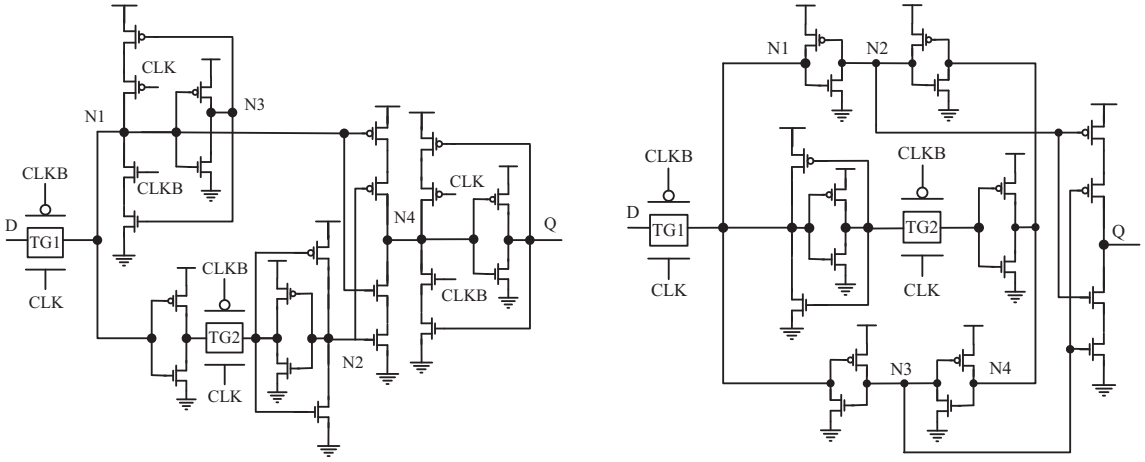

(a) LESH-1. (b) LESH-2.

Fig. 5. Hardened latch proposed in [18].

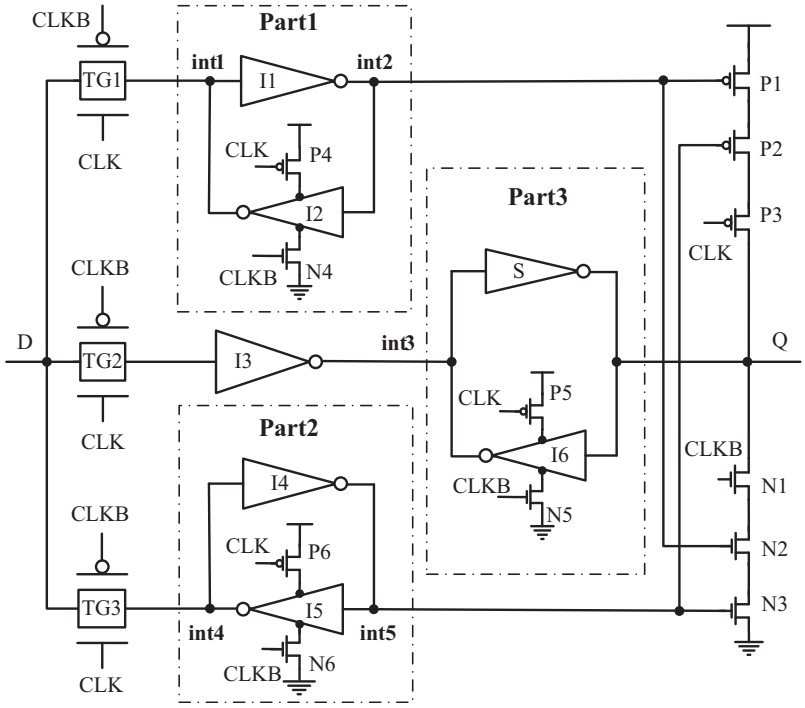

Fig. 6. Proposed latch in this work.

in [17] have not determined a specific circuit for the employed delay element, in order to have a better SET filtering ability, in this paper, an inverter and a Schmitt trigger circuit are used as a delay element, and the structure of Schmitt trigger circuit is shown in Fig. 1.

To simulate the behavior of the upset striking on a node, a well-known time-varying exponential current source is utilized which is proposed in [19]. Although the double exponential model cannot completely describe all of the physics and resulting transient characteristics, it is widely used for comparative studies. And the exponential current source can be expressed as follows [19]:

$$I(t) = I_0\left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}}\right) \quad (1)$$

where τ_α is the collection time constant of the junction; τ_β is the time constant for initially establishing the ion track. The time constants τ_α and τ_β are dependent on process technology, however, the authors in different literatures [16,20–23] employing different process technologies use the same values of 164 ps and 50 ps for τ_α and τ_β in simulating process. Considering references [23–26] which all employ 65 nm technology, τ_α and τ_β are set to 164 ps and 50 ps, respectively.

In Table 1, the evaluation costs of the proposed latch and other latches are compared in terms of area, D to Q delay, power and power delay product and so on. As can be seen in Table 1, the power consumption of the proposed latch is 355.50%, 70.13%, 48.45%, 85.87%, 136.02%, 133.49%, 32%, 60.98% and 33.16% of Ref. latch and the latches designed in [11–14,16–18], respectively. The power consumption can be divided into two parts which are dynamic and static power, and the main part of the power consumption is due to dynamic power which is affected mainly by

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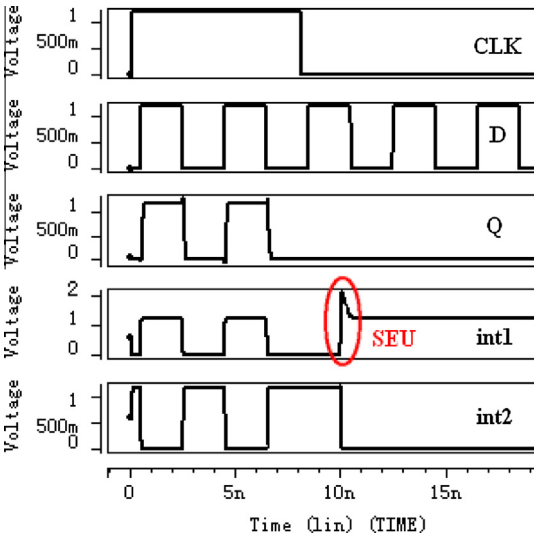

Fig. 7. SEU injection to node "int1".

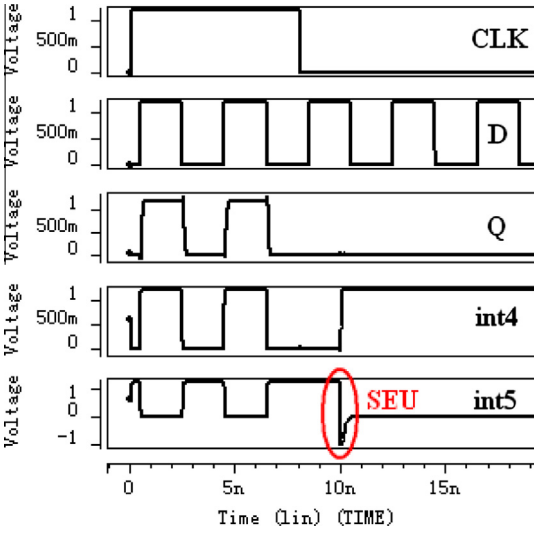

Fig. 8. SEU injection to node "int5".

switching activity, supply voltage, node capacitances and feedback loop operation. The latches designed in [12, 17, EVFERST] have the most switching activity, so their power consumptions are larger than our proposed latch, latches designed in [11–13,18] have active feedback loops when they work in their transparent modes, which makes them take a longer time to change the value stored on node capacitances, then increasing the power consumption. Our proposed latch has overcome these problems by rationally arranging the transmission gate to reduce switching activity and by cutting off all undesired feedback operation. Ref. latch and latch designed in [14] have lower power consumptions, this is mainly because of their smaller node capacitances, and the latch designed in [16] not only has smaller node capacitances, but also use four C-elements forming stacking to reduce power consumption.

Based on 65 nm CMOS commercial technology, the total areas of various latches mentioned before have been compared in Table 1. The area is affected by the amount and size of the transistors and also by the complexity of concatenation among transistors in a latch. A lower complexity of concatenation means more source and drain sharing which remarkably reduces the area. Our proposed latch has the second largest amount of transistors, only less than latch designed in [17, EVFERST], so its area overhead is bigger than Ref. latch and the latches proposed in [11, 14, HLR-CG1, 16, 18, LSEH2]. However, it has an equal amount of transistors, but lower complexity of concatenation than latch designed [12], so its area is smaller than that of latch in [12]. LSEH1 in [18] has smaller amount of transistors, but a larger area than our proposed, this is because LSEH1 contains a closed feedback loop. As a result, transmission gate 2 and its front inverter have to own a larger size to drive this loop, resulting in an increase area. To summarize, the proposed latch has a larger area than the latches designed in [11, 14, HLR-CG1, 16, 18, LSEH2] and Ref. latch. However, the latch designed in [11] cannot fully immunize SEU, the latches designed in [14, HLR-CG1, 16] cannot filter out input SET and LSEH2 designed in [18] has second largest power consumption. The proposed latch has a comparable area overhead compared with the latches designed in [13,18, LSEHI]. The latch designed in [17, EVFERST] has a largest area overhead among all the mentioned latches because of its largest amount of transistors.

Power delay product (PDP) is a useful metric for evaluation of cost, which shows the trade-off between power and performance. Here we use the PDP as stated in [18]:

$$\mathrm{PDP} = \mathrm{Pwr} \times (T_D - T_P) \tag{2}$$

where, Pwr denotes the total consumed power, $T_D - T_P$ mentioned as real delay; T_D and T_P are the time of D to Q and the maximum filtered SET width, respectively. In this metrics, the real delay is induced by two inverters and a transmission gate in Ref. latch, a transmission gate and a C-element in [11]-latch, a transmission gate and an inverter in our proposed latch, and so on. By analyzing the contribution to the real delay, we can see that our proposed latch has a better delay than latches in [11, 12, 17, EVFERST, 18] and Ref. latch, but a worse one than latches [13,14,16] whose delays

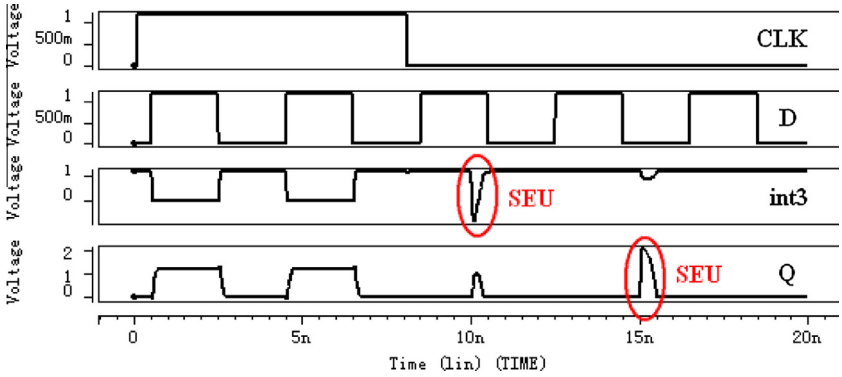

Fig. 9. SEU injection to node "int3" and node "Q".

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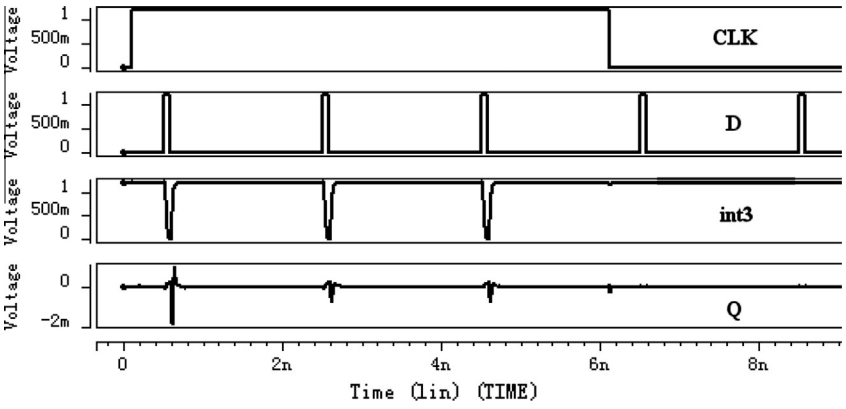

Fig. 10. SET filtering capability of the proposed latch.

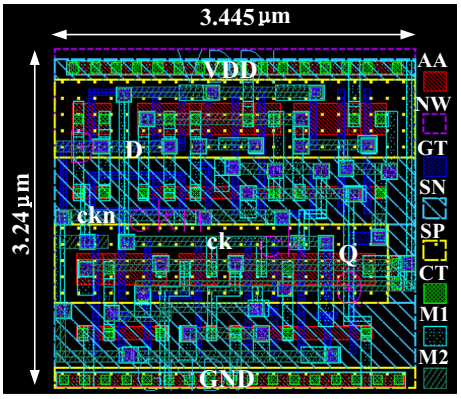

Fig. 11. Layout of the proposed latch.

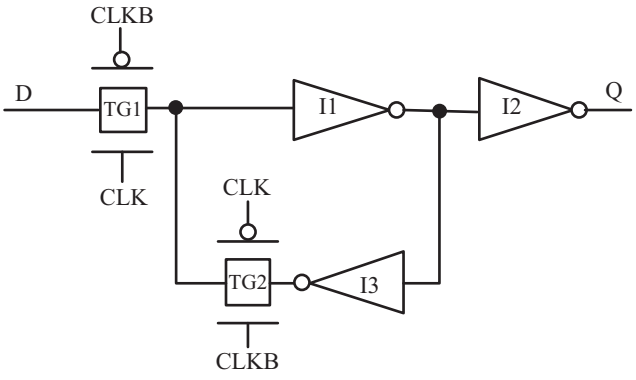

Fig. 12. Reference latch.

are only induced by a transmission gate. After analyzing the power consumption and real delay, the PDPs of these nine latches are given in Table 1, the proposed latch has the third lowest PDP, whose PDP is 201.17%, 39.84%, 31.69%, 90.48%, 304.14%, 197.35%, 12.06%, 32.44% and 16.08% of the other latches in Table 1, respectively.

The maximum filtered SET width and the D to Q delay are also a trade-off, the larger a latch can filter out the SET width, the longer D to Q delay it will have. In other words, to have a better ability of SET filtering, more D to Q delay should be induced, so a simple comparison in terms of the Max width of filtered SET or in terms of the delay D to Q among these latches is not fair. In order to have a fair comparison among the evaluated latches, we define the ability of SET filtering (AOSF) as following relation:

$$\mathrm{AOSF} = T_P/T_D \times 100\% \quad (3)$$

where the T_D and T_P are the same factors with formula 1, respectively. In terms of this metric, a larger AOSF means a better ability of input SET filtering. In this part, only the proposed latch and the type 4 latches are compared. From Table 1, it can be concluded that the proposed latch has a better AOSF than the latch designed in [18, LSEH2], and a comparable AOFS compared with the latch designed in [18, LSEH1], while a worse AOSF than the latch designed in [17, EVFERST].

At nanoscales, the density of integrated circuits is very high, hence a particle striking on a circuit may be collected by multiple nodes. The effects of charge collection and diffusion in nanoscale VLSI are significant features for assessing the capability to tolerate a single event with a multiple-node upset. So we have investigated

Table 1
Performance comparison in terms of power, delay and area and so on.

latch	Power (µW)	D–Q delay (ps)	PDP (j)	Max. width of filtered SET (ps)	Area (µm^2)	SET filtering?	Fully SEU immune?	AOFS (%)	Type
Ref. latch	0.564	48.6	2.741E−17	–	3.854	No	No	–	–
Design in [11]	2.859	328.4	1.384E−16	280	9.921	Yes	No	85.3	Type 1
Design in [12]	4.138	130.1	1.740E−16	88	13.013	Yes	No	67.7	Type 1
Design in [13]	2.335	26.1	6.094E−17	–	11.734	No	Yes	–	Type 3
HLR-CG1 in [14]	1.474	12.3	1.813E−17	–	6.944	No	Yes	–	Type 3
Design in [16]	1.502	18.6	2.794E−17	–	6.193	No	Yes	–	Type 3
EVFERST in [17]	6.265	325.5	4.573E−16	252.5	14.323	Yes	Yes	77.6	Type 4
LSEH1 in [18]	3.288	198.7	1.700E−16	147	11.541	Yes	Yes	74.0	Type 4
LSEH2 in [18]	6.047	189.2	3.429E−16	132.5	10.222	Yes	Yes	70.1	Type 4
Proposed	2.005	105.0	5.514E−17	77.5	11.162	Yes	Yes	73.8	Type 4

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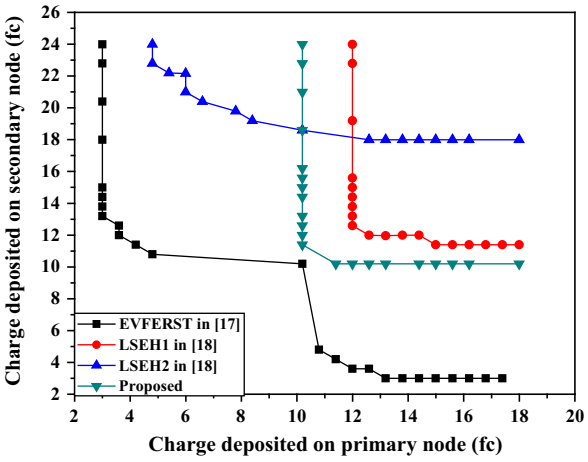

Fig. 13. Critical charge plot of the critical pair.

the SEMUs tolerance capability among the latches of type 4. The simulations of a multiple-node upset start with identifying the critical pair of the circuit, and the critical pairs are nodes N3 and N4 in [17, EVFERST]-latch, nodes N1 and N4 in LSEH1 latch, N1 and N4 (or N1 and N2, depends on the storing state) in LSEH2 latch, nodes int1 and int4 in our proposed latch. By finding these critical pairs, the curve of the primary node charge versus the secondary node charge is plotted. Fig. 13 shows the simulation results for the single-event multiple-node upset. This plot can provide a criterion to quantify the tolerance to a multiple-node upset, and the area under the curve corresponds to the tolerance. Using this criterion, we can easily find that our proposed latch has a better capability of SEMUs tolerance than the latch design in [17, EVFERST], and a comparable one compared with LSEH2 latch, but it has a worse one than LESH1 latch.

5. Supply voltage, temperature and process variations effects

In the following of this section, we investigate the impacts of the temperature, supply voltage and process variations on the proposed latch and previous latches. To do this, we have performed a set of Monte Carlo post-layout simulations using HSPICE tool. Similar to [18], the results for each of the latches are normalized to related parameter with no variation (i.e. the values presented in Table 1), except for supply voltage versus total power consumption.

Fig. 14 shows the supply voltage variation effects on latch circuits, and the supply voltage is changed from 0.9 V to 2.0 V. With the increasing of the supply voltage, the power consumption is increasing as they are shown in Fig. 14(a). This is because high supply voltage provides high noise margin for a circuit. Hence, the required noise to affect the circuit also increases, which has been mentioned in [12]. However, the D–Q delay is decreasing with the increasing supply voltage, this is because high supply voltage results in high conducted current on the device, then circuit delay will decrease. Fig. 15 shows the temperature variation effects on the latch circuit in terms of power consumption and D–Q delay. Temperature is changed from −40 °C to 120 °C. It can be seen that the power consumptions and D–Q delay of the considered latches are all increasing with the increasing of temperature. The reason has been mentioned in [12], which is due to the decreasing of the device carrier mobility.

Finally, Monte Carlo simulations with section mc of 65 nm commercial technology model are done to investigate the process variation effects on all the latches mentioned in this paper. In order to get parameters of deviation (σ) and standard deviation (dev) for every latch, 500 monte carlo simulations have been run at 1.2 V power supply and room temperature (27 °C), the deviations are stated in [18], which are restated here:

$$\sigma = \sqrt{\frac{\sum (x_i - x_m)^2}{N}} \tag{4}$$

$$dev = \frac{\sum |x_i - 1|}{N} \tag{5}$$

where σ is the parameters of deviation, dev is standard deviation, N, x_i and x_m denote the number of values that is 500, the values and the average of values, respectively.

Figs. 16 and 17 shows the impacts of process variation on power consumption and D–Q delay. It can be seen that our proposed latch has less sensitivity to process variation as compared to other latches. These conclusions can be validated by Tables 2 and 3, which show parameters of deviation (σ) and standard deviation

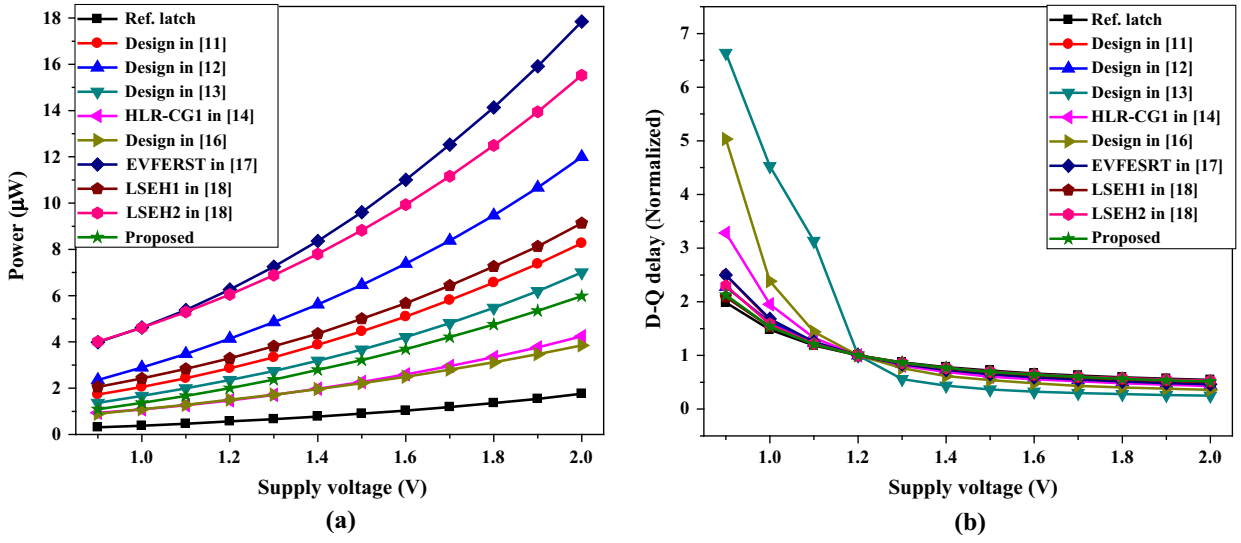

Fig. 14. Supply voltage variation impact on: (a) total power consumption; (b) D–Q delay.

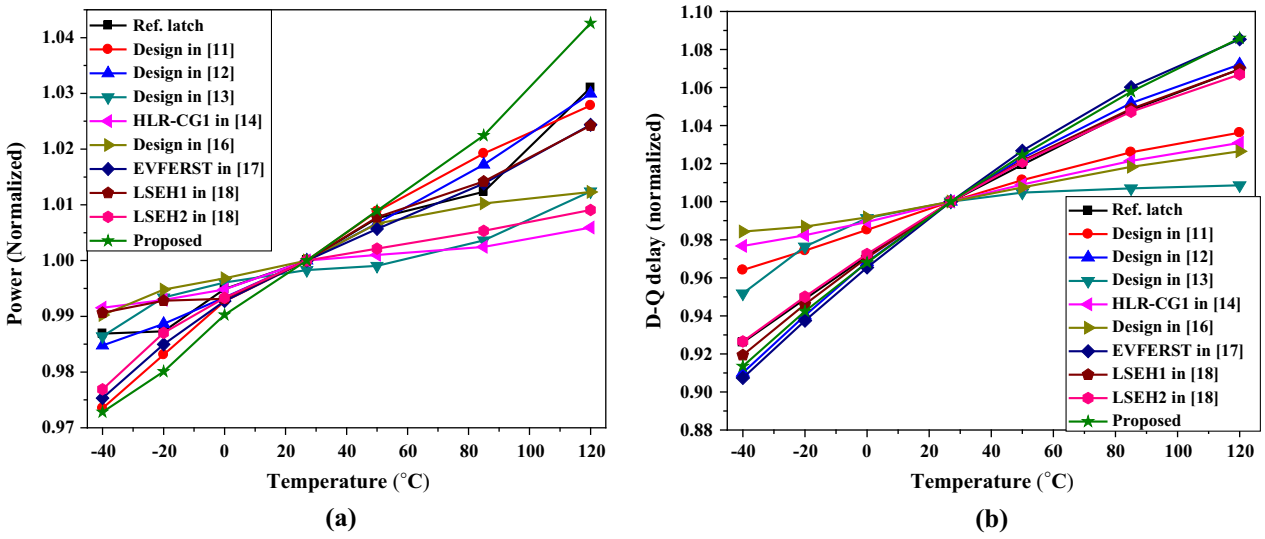

Fig. 15. Temperature impact on: (a) total power consumption; (b) D–Q delay.

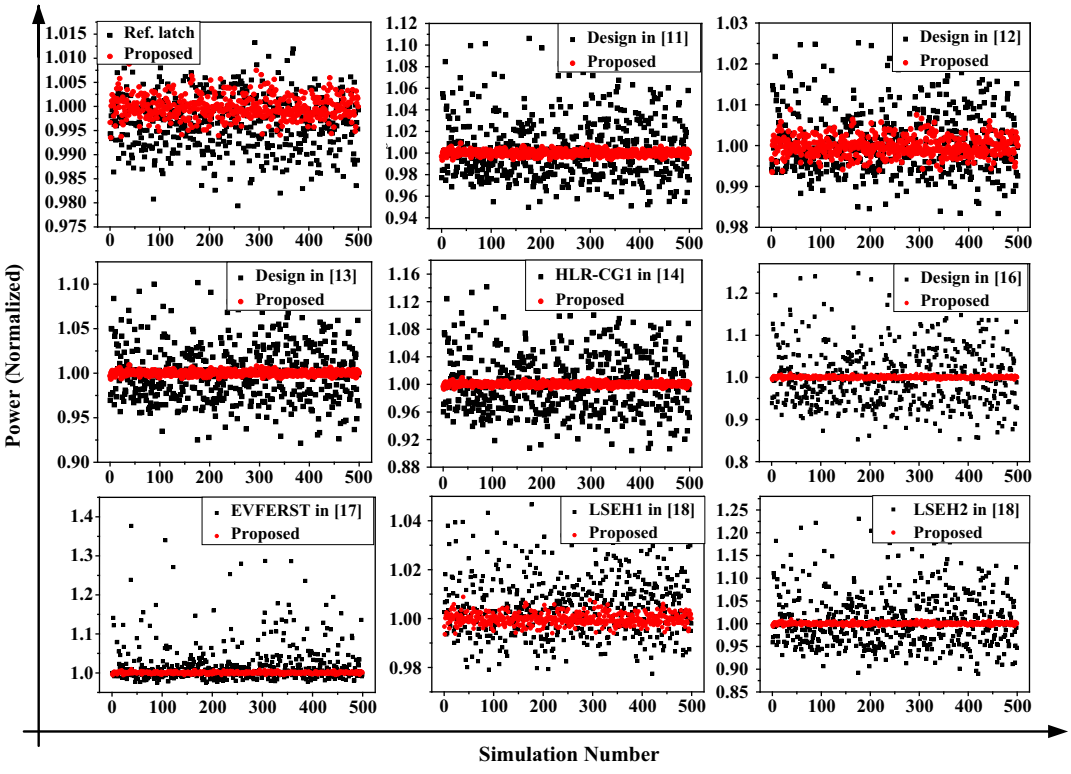

Fig. 16. Monte Carlo simulations vs. power (normalized).

(*dev*) of power consumption and deviations of D–Q delay, respectively. From Fig. 16 and Table 2, it can be seen that our latch receives so lower impact from process variation on its power consumption than the other designs. This result may owe to the following reasons. The first and perhaps most important reason is that, it is well known from feedback theory that positive feedback loop increases the circuit sensitivity to parameter variations [27,28]. Fortunately, our proposed latch does not have active positive feedback loops while the other hardened latches mentioned in this paper all suffer this problem to some extent when they work at their transparent modes; this makes our proposed latch have a lower impact from process variation. Secondly, Schmitt trigger circuit (S) used in our proposed latch can increase the margin of threshold voltage due to its hysteresis property, which finally reduces the impact of process variation. Besides, using stacked transistors is another reason why our proposed latch has a lower impact from process variation [29]. To summarize, only our proposed latch mentioned in this paper meets the factors of not having active positive feedback loop, employing Schmitt trigger circuit (S) and using stacked transistors simultaneously, these factors finally make our latch have a lower impact from process variation on its power consumption compared with the other latches.

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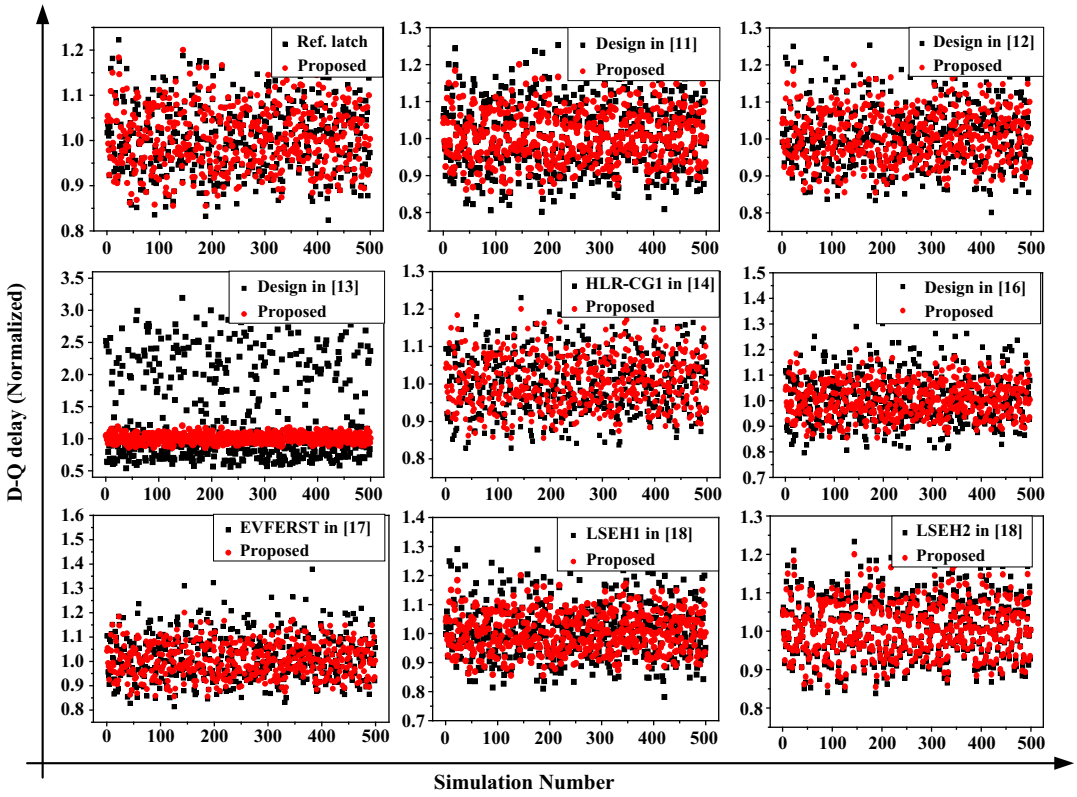

Fig. 17. Monte Carlo simulations vs. D–Q delay (normalized).

Table 2
Deviations of power consumption.

	Ref. latch	Design in [11]	Design in [12]	Design in [13]	HLR-CG1 in [14]	Design in [16]	EVFERST in [17]	LESH1 in [18]	LESH2 in [18]	Proposed
σ	0.0055	0.0288	0.0079	0.0328	0.0456	0.0731	0.0761	0.0125	0.0612	0.0024
dev	0.0052	0.0223	0.0062	0.0261	0.0362	0.0574	0.0343	0.0105	0.0470	0.0019

Table 3
Deviations of D–Q delay.

	Ref. latch	Design in [11]	Design in [12]	Design in [13]	HLR-CG1 in [14]	Design in [16]	EVFERST in [17]	LESH1 in [18]	LESH2 in [18]	Proposed
σ	0.0752	0.0936	0.0825	0.7463	0.0805	0.0976	0.0966	0.0936	0.0761	0.0672
dev	0.0612	0.0769	0.0654	0.6117	0.0649	0.0761	0.0758	0.0743	0.0628	0.0554

6. Conclusion

This paper has proposed a low cost and highly reliable radiation hardened latch circuit which is implemented in 65 nm commercial technology. By reasonable structure design, the proposed latch is fully SEU immune which means that it can tolerate an SEU on any one of its internal single node. In addition, the proposed latch is capable of SET filtering. Hence, the proposed latch not only can tolerate the soft errors caused by input SETs in combinational parts, but also can tolerate internal SEUs in sequential parts. The proposed latch has also overcome the problem of taking a high impedance state when a particle strikes on some of its internal nodes. Compared with the latches of type 4, our proposed latch features at least 39% and 67.6% reduction of power consumption and power delay product, respectively, in other words, our proposed latch has the lowest power consumption and power delay product among the latches of type 4, while it features a second lowest area overhead and has a comparable ability of SEMUs tolerance. The impacts of process, supply voltage and temperature variation on proposed latch are also investigated, which shows that our proposed latch is less sensitive to voltage and process.

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