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Research Article

A New Digital to Analog Converter Based on Low-Offset Bandgap Reference

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This paper presents a new 12-bit digital to analog converter (DAC) circuit based on a low-offset bandgap reference (BGR) circuit with two cascade transistor structure and two self-contained feedback low-offset operational amplifiers to reduce the effects of offset operational amplifier voltage effect on the reference voltage, PMOS current-mirror mismatch, and its channel modulation. A Start-Up circuit with self-bias current architecture and multipoint voltage monitoring is employed to keep the BGR circuit working properly. Finally, a dual-resistor ladder DAC-Core circuit is used to generate an accuracy DAC output signal to the buffer operational amplifier. The proposed circuit was fabricated in CSMC 0.5 μm 5 V 1P4M process. The measured differential nonlinearity (DNL) of the output voltages is less than 0.45 LSB and integral nonlinearity (INL) less than 1.5 LSB at room temperature, consuming only 3.5 mW from a 5 V supply voltage. The DNL and INL at −55°C and 125°C are presented as well together with the discussion of possibility of improving the DNL and INL accuracy in future design.

1. Introduction

Along with the development of the semiconductor technology, phased array radar system has become more and more attractive in the area of space communication. However, due to the source limitation in space environment, it constrains that the design of the transmit/receive (TR) module has to have many control ability to switch between transmit and receive mode. This has motivated the design of high performance control chip with respect to accuracy, linearity, and stability under harsh space environment [1–4].

The duty of the control chip is to deliver different bias voltage to corresponding chip by following instructions from command computer. Therefore, its performance is highly relay on the design of its digital to analogous converter (DAC). There are many types of DAC structures that have been proposed in the literature [5–12]. Resistor based DAC architecture is one of the most attractive due to its simplicity structure, high stability, high monotonic, and low power consumption [12] and is a good choice for space application. However, for resistor type of DAC architecture, the DAC's number of bits is proportional to the number of resistor used in the circuit. The higher number of resistors further leads to larger of chip area. It also faces the increasing of instability due to the effectiveness of processing technology on the larger number of resistors. In order to solve such problems, the researchers have developed many types of architecture such as subranging [5], dual-ladder resistor [6], resistor-floating-resistor-string [7], embedded operational amplifier [8], and multibits calibration [9]. Nonetheless, all those methods are able to improve some the DAC circuit in different ways; there are still more space that can be improved, especially in the application of space environment. This has motivated the introduction of low-offset bandgap reference (BGR) structure [10, 11]. The good side is that the BGR circuit is able to provide a reference voltage to the DAC circuit for improving the stability of DAC circuit for a normal application, but for the harsh environmental application such as space application, the BGR circuit needs to be improved further to cope with the application.

In this work, we have introduced a new development of a 12-bit high precision, low power consumption, and high stability DAC circuit based on an improved low-offset BGR

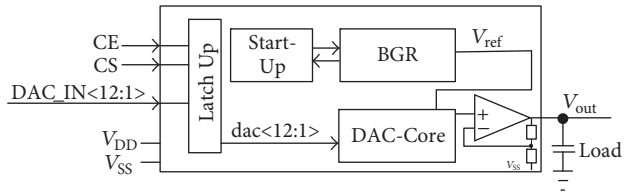

Figure 1: Block diagram of the proposed DAC circuit.

and dual-resistor ladder circuit. Three main blocks have been optimized to achieve the design constrains.

2. DAC Overall Circuit Design

The proposed circuit design mainly includes three parts: BGR block, Start-Up Block, and DAC-Core Block as illustrated in Figure 1. The input signal of the proposed DAC includes a pair of latch up signal "CE" and "CS"; it decides which input DAC instruction is stored into the "Latch Up" register. The "DAC IN<12:1>" is a 12-bit input instruction from an upper-computer which will be transferred to a set of bias voltages "V_{out}" and act on the following chipset in a TR module. "V_{DD}" and "V_{SS}" correspond to "+5 V" and "0 V" and are the power supply of the DAC. The reference voltage from BGR circuit is $V_{ref} = 2.5$ V. The end stage operational amplifier is a two-stage PMOS class-AB output buffer with a 0.2 V to 4.8 V output voltages.

3. The BGR Circuit Design

The aim of the BGR circuit is to provide a stable reference voltage "V_{ref}" to the "DAC-Core" circuit without the effects from variation of power supply and environment condition such as temperature and radiation. There are two ways that have been employed in this paper to improve the stability of "V_{ref}." One is the use of two-cascade transistor structure; the second is the use of two low-offset operational amplifier with self-contained feedback circuit. They are detailed as follows.

First, let us start with analysis of the traditional BGR circuit illustrated in Figure 2 [12]; the output voltage "V_{ref}" can be written as

$$V_{ref} = V_{be\text{-}Q_2} + \left(1 + \frac{R_2}{R_1}\right)\left(V_t \ln(n) - V_{OS}\right), \quad (1)$$

where "$V_{be\text{-}Q_2}$" is base-emitter voltage for Q_2 (≈ 0.7 V), "V_t" is the electron thermal voltage (≈ 0.026 V), "V_{OS}" is the input offset voltage for operational amplifier, "n" is the ratio between number of Q_2 and number of Q_1. From (1), we know that the most troublesome part is "V_{OS}." If we can reduce the effect of "V_{OS}," then we have found a way of stabilize the overall DAC circuit. This is done by using a low-offset BGR circuit which is shown in Figure 3. This architecture employs two-cascade transistors to minimize the contribution of "V_{OS}" on "V_{ref}."

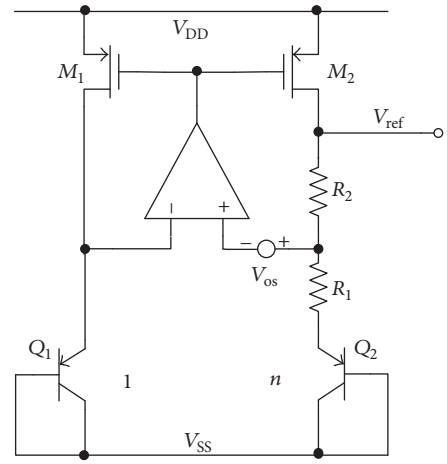

Figure 2: The traditional BGR circuit.

From Figure 3, the output voltage of the improved low-offset BGR circuit is written as

$$V_{ref} = 2V_{be\text{-}Q_3Q_4} + \left(1 + \frac{R_2}{R_1}\right)\left(2V_t \ln(n) - V_{OS}\right), \quad (2)$$

where "$V_{be\text{-}Q_3Q_4}$" is the base-emitter voltage for transistor "Q_3" and "Q_4". Comparing (1) and (2), the effectiveness of "V_{OS}" to the "V_{ref}" is reduced by increasing the value of "$2V_{be\text{-}Q_3Q_4}$" and "$2V_t \ln(n)$." However, the value of "V_{OS}" is untouched from (2), which still causes problems. Therefore, in order to reduce the effect of "V_{OS}" further, two low-offset operational amplifiers (see Figure 4) with self-contained feedback circuit are employed in here to reduce the effects of PMOS current-mirror mismatch and its channel modulation without the decrease of supply power redundancy. It further leads to the reducing of "V_{OS}" value of the overall BGR circuit.

4. Start-Up Circuit Design

The Start-Up circuit has a self-bias and multipoint monitor structure which provides a self-bias current to the BGR circuit. As demonstrated in Figure 5, when the power of the DAC is switched on, points A and B will have a high voltage level; "V_{ref1}" and "V_{ref2}" are at low voltage level. The current at BGR circuit is "0." The MOSFET M7–M10 are "off." M5 and M6 are "on." Current is injected into BGR circuit and the voltage level starts to drop at points A and B at the same time. Following this process, M1 and M2 are switched on which indicates the BGR circuit is fully functioning. M7 and M8 mirror the BGR circuit current "ib." At this point, M5 and M6 are switched off, and the Start-Up circuit changes to low power consumption state. The voltages at "V_{ref1}", "V_{ref2}," and point A are monitored during the DAC working state. Once the voltage at those three points is affected by the environment condition, they will wake up the Start-Up circuit to keep the BGR circuit working properly.

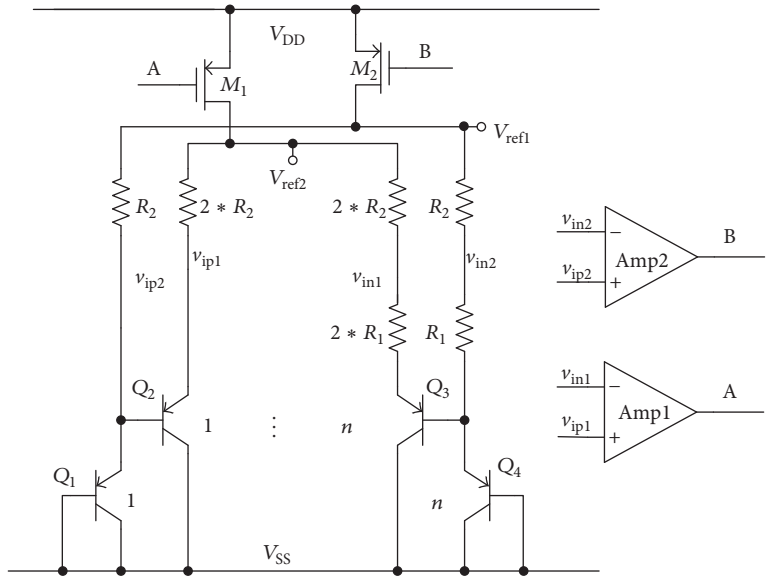

Figure 3: Improved low-offset BGR circuit.

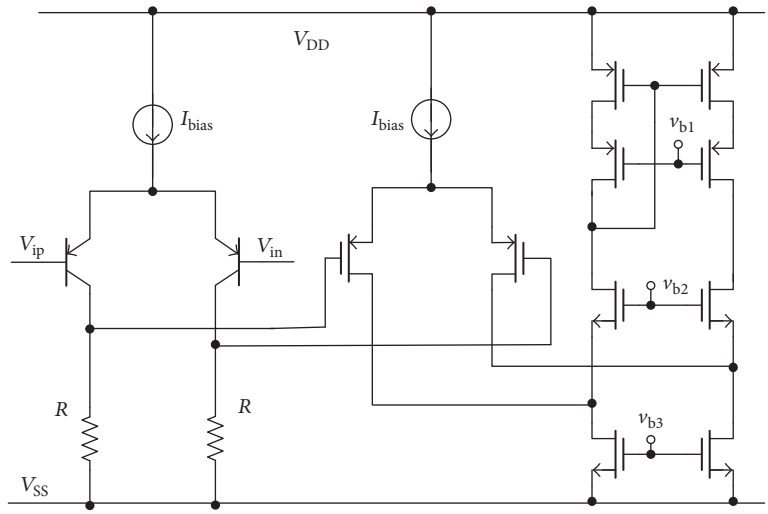

Figure 4: Low-offset operational amplifier circuit.

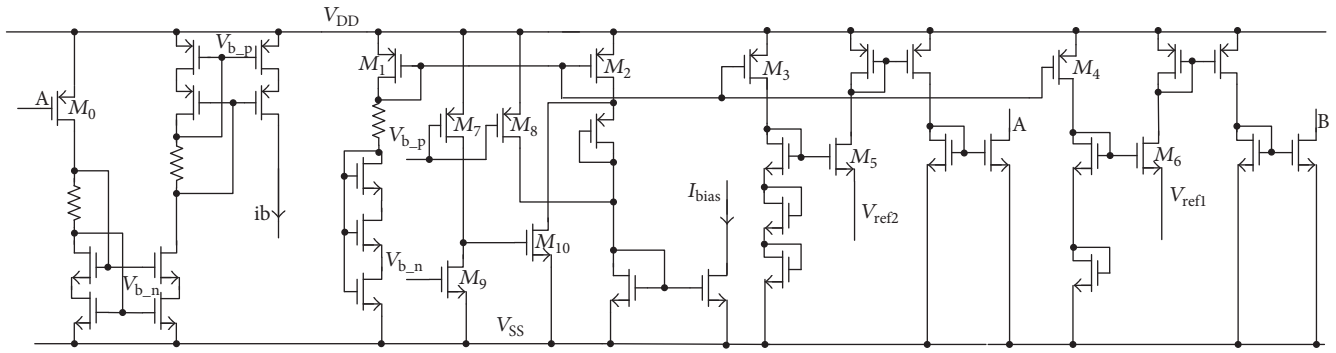

Figure 5: Start-Up circuit with self-bias current source.

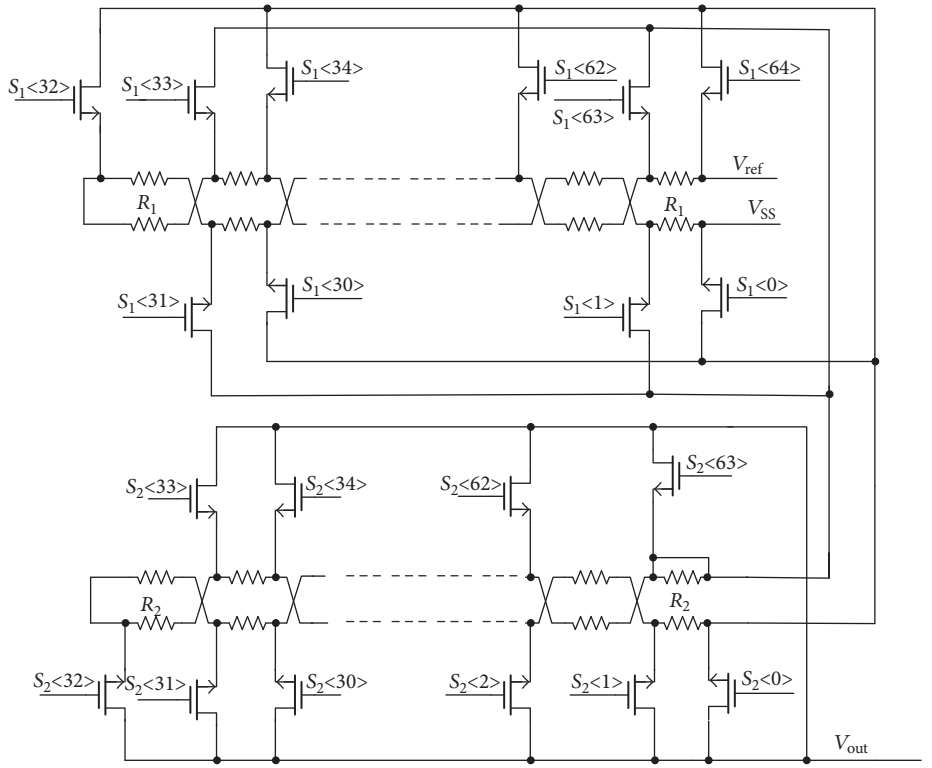

Figure 6: Dual ladder resistor string circuit.

5. DAC-Core Circuit Design

The design of the DAC-Core circuit is based on resistor structure to achieve high output monotonic and stability with simply layout and low power dissipation. A two stage dual-ladder resistor string circuit structure is used in here to trade off between the accuracy and chip size. R_1 and R_2 are the voltage splitter at the first and second stage. There are two switches S_1 and S_2. They have been controlled by DAC IN<12:7> for S_1 and DAC IN<6:1> for S_2.

The main problem of such design is that when S_1 is in action, the fluctuation of its switch on resistance (R_{on}) will result in the voltage value change for the second stage resistors. This leads to the lower of the DAC output accuracy. In order to solve this problem, we have adjusted the size of the 65 switches to achieve a full match, low variation of switch on resistance. This is done as follows. First, when the switches in the first stage are switched on in pair, the connection point voltage can be written as "V_r" and "V_p" (see Figure 7); then the effective resistance between those two points is written as

$$R_{\text{Parallel}} = R_1 \parallel (2R_{\text{on}} + 63R_2) = \frac{R_1 (63R_2 + 2R_{\text{on}})}{R_1 + 63R_2 + 2R_{\text{on}}}. \quad (3)$$

Before switching,

$$V_1 = \frac{R_{\text{par}} V_{\text{ref}}}{63R_1 + R_{\text{par}}} \times \frac{63R_2 + R_{\text{on}}}{63R_2 + 2R_{\text{on}}} + V_r. \quad (4)$$

After switching,

$$V_2 = \frac{R_1 + R_{\text{par}} \times (R_{\text{on}} / (63R_2 + 2R_{\text{on}}))}{63R_1 + R_{\text{par}}} V_{\text{ref}} + V_r. \quad (5)$$

The DAC output variation before and after the switching can be written as

$$\begin{aligned} V_{\text{step1}} &= V_2 - V_1 \\ &= \frac{R_1 - \left(63R_2 R_{\text{par}} / (63R_2 + 2R_{\text{on}})\right)}{63R_1 + R_{\text{par}}} V_{\text{ref}}. \end{aligned} \quad (6)$$

Voltage step size in the second stage before switching is illustrated as

$$V_{\text{step2}} = \frac{R_{\text{par}} (R_2 / (63R_2 + 2R_{\text{on}}))}{63R_1 + R_{\text{par}}} V_{\text{ref}}. \quad (7)$$

In order to achieve a high accuracy output of the DAC, V_{step1} has to be equal to V_{step2}, which means that

$$R_{\text{on}} = \frac{R_2 - R_1}{2}. \quad (8)$$

Due to the fact that MOSFET is working at the linear region under switching on condition, then R_{on} can be rewritten as

$$R_{\text{on}} = \frac{1}{\mu_n C_{\text{ox}} (W/L) (V_{\text{GS}} - V_{\text{TH}})}. \quad (9)$$

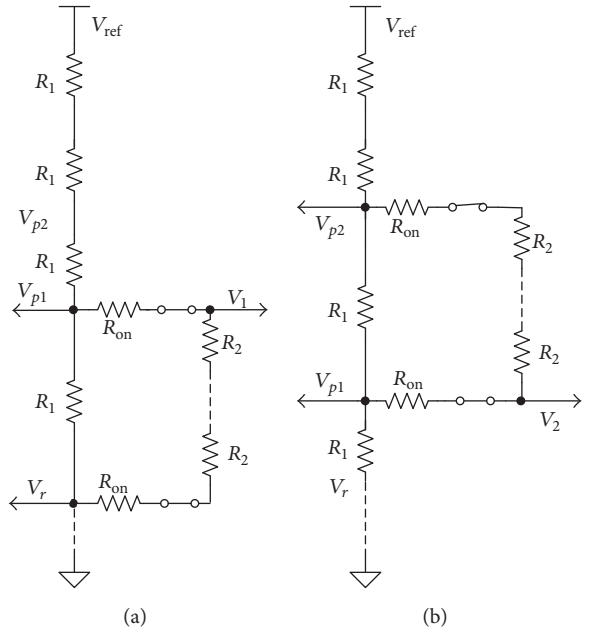

Figure 7: The schematic diagram of switching.

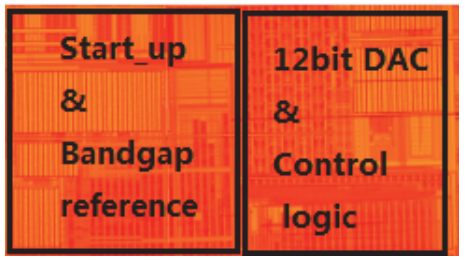

Figure 8: Photography of the proposed DAC chip.

Then the width and length ration of the switches in the first stage have to satisfy the following relation:

$$\frac{W}{L} = \frac{1}{R_{on}\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})}. \quad (10)$$

Therefore, by tuning the width and length ration of the switches in the first stage, the switching resistance effect on the DAC accuracy is reduced.

6. Test Results and Discussion

The proposed DAC circuit is fabricated by using CSMC 0.5 μm 5 V 1P4M process. Its photography is shown in Figure 8.

At the first instance, the 12-bit digital commands from "000000000000" to "111111111111" are tested at three temperature points, −55°C, 25°C, and 125°C, by using a PXI test system and a probe station. The variation of the output DAC is illustrated in Figure 9. It is almost unchanged under the temperature test which indicates that the proposed DAC is every stable at this point. However, this cannot prove that the designed DAC are good enough definitely. Therefore, in order to evaluate the DAC performance more deeply, the NDL and INL results are illustrated as follows.

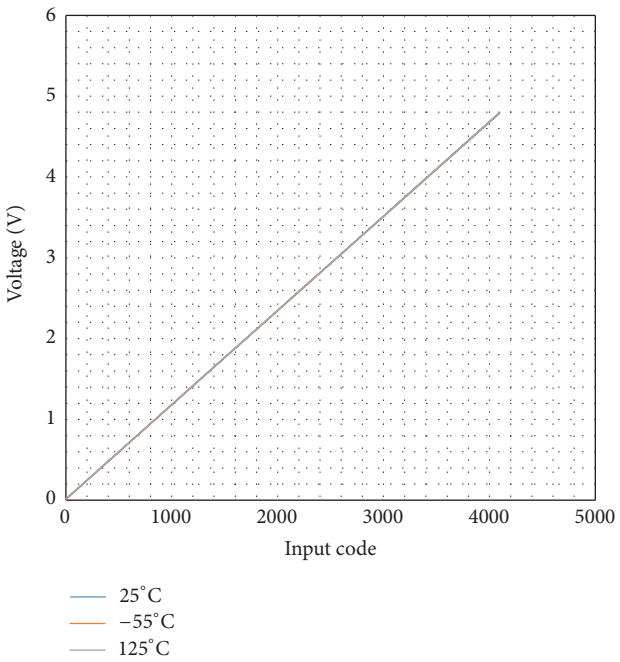

Figure 9: DAC output with different input code.

In Figure 10, the DNL verse input command is shown. The overall DNL is less than 0.45 LSB. There are no periodic properties (there is no sudden changes for every 64 commands within total 4096 commands) that have been observed; this indicates that the proposed DAC the step-size accuracy is kept well by the circuit shown in Figure 6.

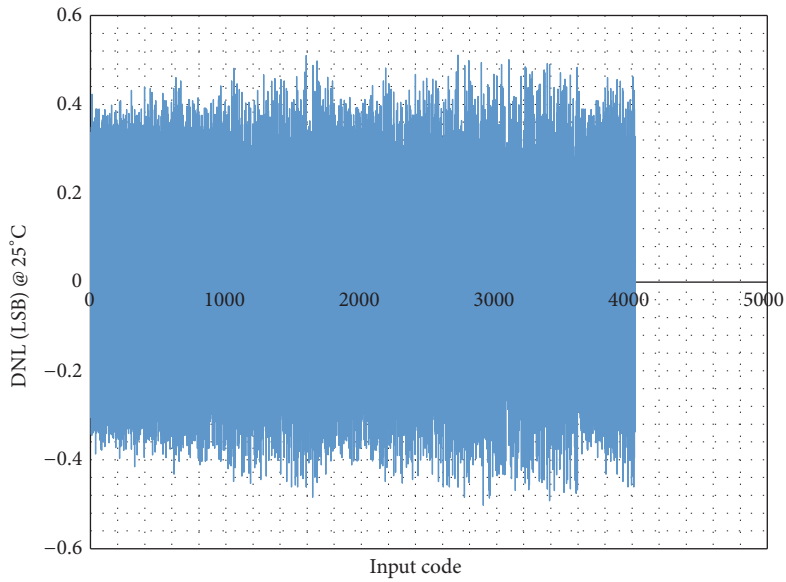

Figure 10: DNL at 25°C.

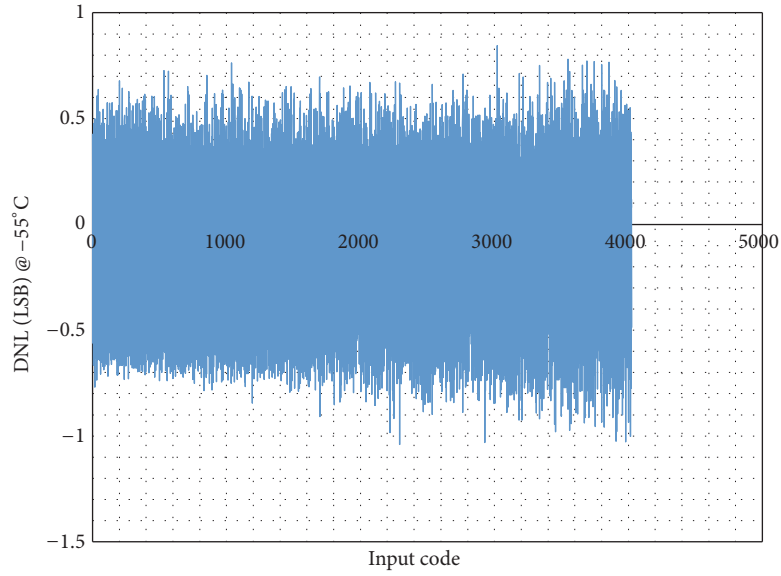

Figure 11: DNL at −55°C.

The DNL under −55°C is illustrated in Figure 11. As shown, the DNL is getting worse with a maximum increase of 0.5 LSB. This is mainly due to the fact that the MOSFET has contributed to the power divider circuit in Figure 6. For MOSFET under low temperature condition, the resistance value for each MOSFET highly depends on its bias voltage which varies rapidly. Those variations have effects on the DAC's DNL significantly. In case of high temperature at 125°C, the MOSFET has been less affected by the temperature; therefore, it results in a better DNL variation compared with the low temperature. This conclusion is illustrated in Figure 12. As illustrated, the DNL variation is less than 0.15 LSB with respect DNL value at 25°C.

The variations of DNL at low temperature are very harmful characteristics for DAC design; they could cause a code jumping when DNL is greater than 1. However, they can be reduced by adding more resistor ladders to reduce the effects of the MOSFET switching resistance. The downside is the increasing of chip size. Therefore, tradeoff between the output accuracy and chip size has been considered during DAC design.

The INL versa input commands are shown in Figure 13. The INL value is less than 1.5 LSB. The shape of the INL curve is not monotonous; it has a "sine wave"-like shape, which indicates the INL has no accumulative error for the full command swap.

In Figures 14 and 15, the INL at −55°C and 125°C are shown. The shapes of the INL are preserved, but the INL value has increased up to 2.5 LSB at 125°C. This is because, during the wafer processing, the concentration for producing

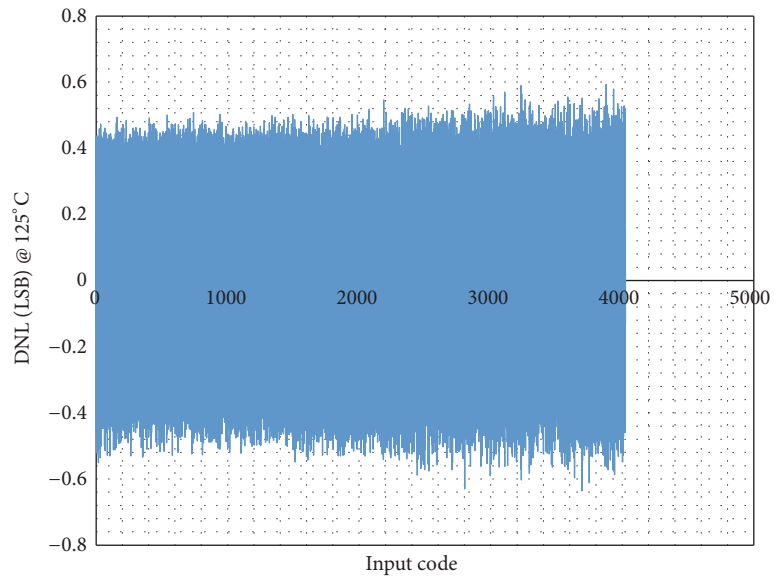

Figure 12: DNL at 125°C.

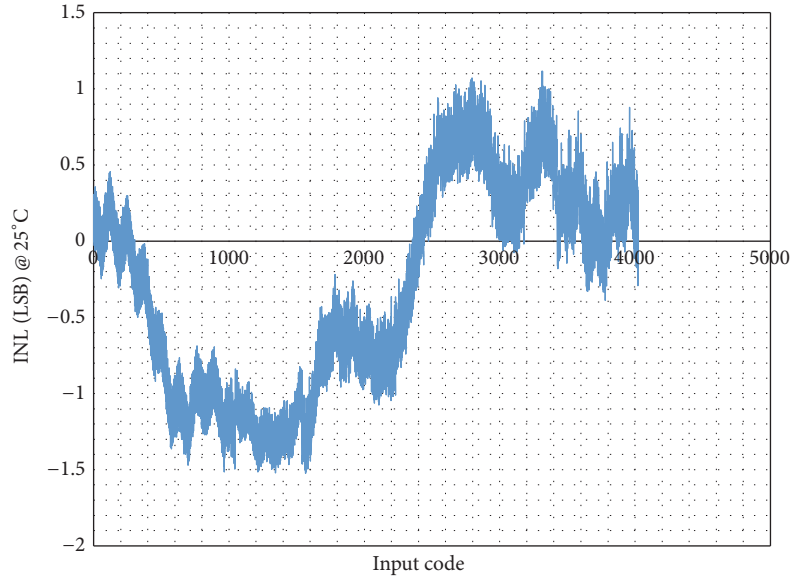

Figure 13: INL at 25°C.

the resistor has a huge effect on the quality of the resistors, and the resistors are sensitive to the high temperature as well compared with the low temperature. This results in that the INL has been getting worse along with the increase of temperature. Another source of uncertainty is that the switch on resistance of the MOSFET is highly affected by the temperature which leads to a poor INL performance. Those can be explained by using a resistors mismatch model illustrated in Figure 16.

As shown in Figure 16, during the wafer process, there will be a resistance gradient which results in a resistance change. This can be demonstrated by introducing ΔR to represent the resistance changes with respect to wafer process (in here, the resistance is modeled as a linear incasing of resistance form the bottom of the resistance ladder to the top). Therefore, the resistance mismatch has created the change of V_{out} under different temperature and leads to the INL and DNL change under temperature.

In case of DNL, it is highly affected by the voltage step size V_{step} as

$$\text{DNL}(k) = \frac{V_{\text{step}}(k) - V_{\text{step}}(\text{ideal})}{V_{\text{step}}(\text{ideal})}. \tag{11}$$

Then the error can be written as follows where $(V_p - V_r)$ is related to the Bandgap reference voltage V_{ref} and ΔR_1:

$$V_{\text{step,error}} = \left(V_p - V_r\right) \frac{|\Delta R_2|}{63R_2 + 2R_{\text{on}}}. \tag{12}$$

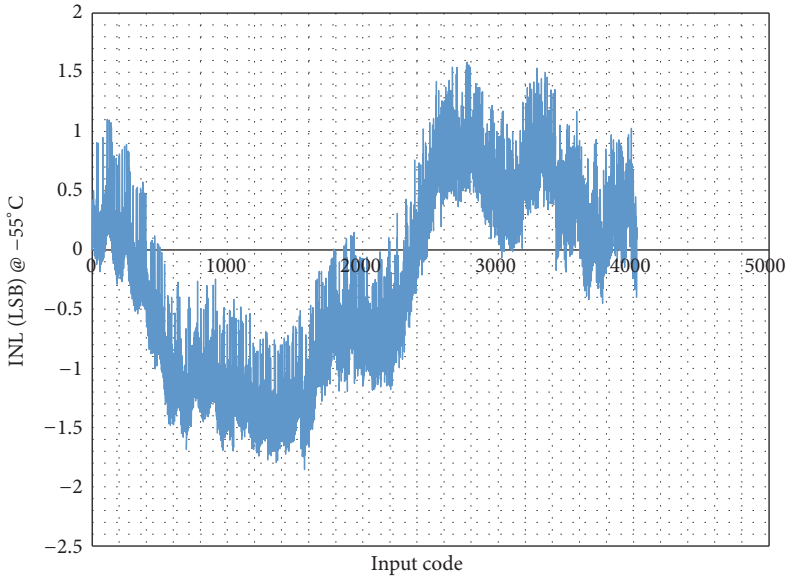

Figure 14: INL at −55°C.

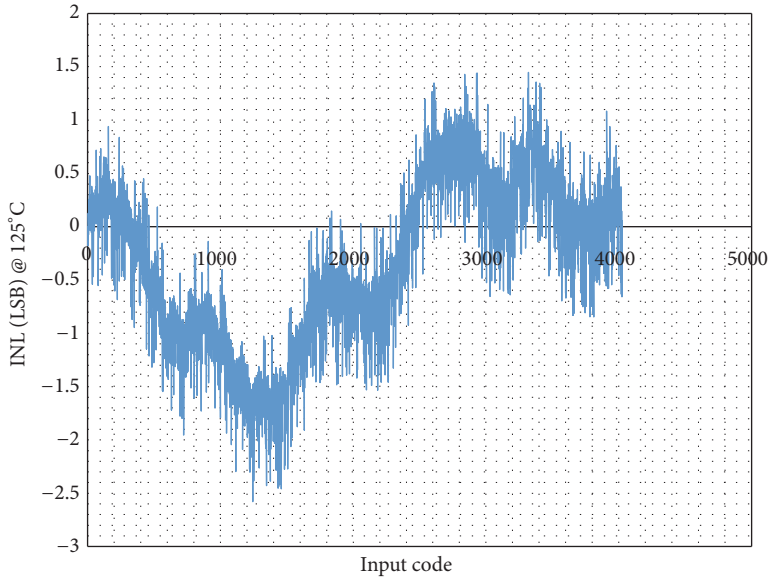

Figure 15: INL at 125°C.

Let k_1 and k_2 represent the temperature coefficient of $R_1(R_2)$ and R_{on}, respectively. The equation of $V_{step,error}$ can be approximated as

$$V_{step,error} = \left(V_p - V_r\right) \cdot \frac{\beta}{63 + 2\left(R_{on}\left(1 + k_2\Delta T\right)/R_2\left(1 + k_1\Delta T\right)\right)}, \quad (13)$$

where β represents the resistance mismatch ratio, $\beta = \Delta R_2/R_2$, and ΔT represents the change of temperature from room temperature. Then, the step error is ultimately affected by V_{ref}, resistance, and its temperature coefficient. Combined with the design in this paper, we can draw the following conclusion: when the temperature becomes high, $V_{step,error}$ becomes larger and the DNL performance decreases.

In case of INL, it is the error between the theoretical voltage and actual voltage which can be expressed as

$$\mathrm{INL}(k) = \frac{V(k) - V_{ideal}(k)}{\mathrm{LSB}} = \sum_{n=0}^{k} \mathrm{DNL}(n). \quad (14)$$

As illustrated in Figure 16, when the temperature changes, all the node voltage in the first ladder will change, while the effect of divider resistance will decrease and the absolute value will deviate from the theoretical value, resulting in INL performance decline. On the other hand, as can be seen from the definition of INL, it can be regarded as the accumulation

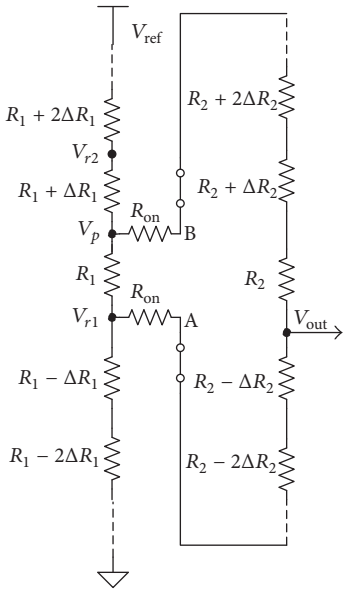

Figure 16: The model of resistors mismatch.

of DNL, so the mechanism of temperature influence on DNL is also applicable to the analysis of INL. The same conclusion can be realized that INL performance is decreased under high temperature.

This can be improved by increasing the resistors value at the second ladder and reducing the resistors value at the first ladder at the same time. This method will reduce the effects of the switching on resistance from the MOSFET. However, we have to be alarmed that the power consumption will increase along with the increasing of the resistor value at the second ladder.

7. Conclusion

In conclusion, a new 12-bit digital to analog converter (DAC) circuit based on a low-offset BGR circuit was presented. In order to improve the stability of the BGR circuit, two cascade transistor structures and two self-contained feedback low-offset operational amplifiers are employed to reduce the effects of offset operational amplifier voltage effect on the reference voltage, PMOS current-mirror mismatch, and its channel modulation. A Start-Up circuit with self-bias current architecture and multipoint voltage monitoring was also used to keep the BGR circuit working properly. The DAC-Core circuit with a dual-resistor ladder structure is employed to produce an accuracy output signal. The INL and DNL results of the proposed circuit using CSMC 0.5 μm 5 V 1P4M process at −55°C, 25°C, and 125°C are presented. The measured DNL of the output voltages is less than 0.45 LSB and INL is less than 1.5 LSB at room temperature, consuming only 3.5 mW from a 5 V supply voltage. The discussion of improving the INL and DNL in the future design is detailed as well to provide a vision of high accuracy, low power consumption, and high stability DAC design.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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References

[1] G. M. Rebeiz, K. J. Koh, T. Yu et al., "Highly dense microwave and millimeter-wave phased array T/R modules using CMOS and SiGe RFICs," in *Proceedings of the IEEE 12th Annual Wireless and Microwave Technology Conference (WAMICON '11)*, pp. 1–5, April 2011.

[2] A. Bettidi, D. Carosi, F. Corsaro, L. Marescialli, P. Romanini, and A. Nanni, "MMIC Chipset for wideband multifunction T/R module," in *Proceedings of the IEEE MTT-S International Microwave Symposium (IMS '11)*, Baltimore, Md, USA, June 2011.

[3] F. W. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 603–621, 2003.

[4] F. Faccio, K. Kloukinas, A. Marchioro et al., "Single event effects in static and dynamic registers in a 0.25/spl mu/m CMOS technology," *IEEE Nuclear Science Transactions*, vol. 46, no. 6, pp. 1434–1439, 1999.

[5] A. G. F. Dingwall and V. Zazzu, "An 8-MHz CMOS subranging 8-bit A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 6, pp. 1138–1143, 1985.

[6] C.-W. Lu, C.-M. Hsiao, and P.-Y. Yin, "A 10-b two-stage DAC with an area-efficient multiple-output voltage selector and a linearity-enhanced DAC-embedded op-amp for LCD column driver ICs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1475–1486, 2013.

[7] C.-W. Lu, P.-Y. Yin, C.-M. Hsiao, M.-C. F. Chang, and Y.-S. Lin, "A 10-bit resistor-floating-resistor-string DAC (RFR-DAC) for high color-depth LCD driver ICs," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2454–2466, 2012.

[8] J.-S. Kang, J.-H. Kim, S.-Y. Kim et al., "10-bit driver IC using 3-bit DAC embedded operational amplifier for spatial optical modulators (SOMs)," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2913–2922, 2007.

[9] K. Parthasarathy, T. Kuyel, Y. Zhongjun, C. Degang, and R. Geiger, "A 16-bit resistor string DAC with full-calibration at final test," in *Proceedings of the IEEE International Test Conference (ITC '05)*, Austin, Tex, USA, November 2005.

[10] C. M. Andreou, S. Koudounas, and J. Georgiou, "A novel wide-temperature-range, 3.9 ppm/∘C CMOS bandgap reference circuit," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 574–581, 2012.

[11] C. Y. Leung, K. N. Leung, and P. K. T. Mok, "Design of a 1.5-V high-order curvature-compensated CMOS bandgap reference,"

in *Proceedings of the IEEE International Symposium on Cirquits and Systems (ISCAS '04)*, May 2004.

[12] R. Behzad, "Design of analog CMOS integrated circuits," *International Edition*, vol. 400, 2001.