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Direct Digital Converter for a Single Active Element Resistive Sensor

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***Abstract*— A direct digital converter that provides a digital output, proportional to the measurand being sensed by a single active element resistive sensor is presented in this paper. To accomplish this task, the structure and the switching sequence of a conventional dual slope, analog to digital converter (DSADC) is appropriately altered so that the altered DSADC accepts the resistance of the sensor as an integral part and provides a digital output that is linearly proportional to the physical quantity being sensed by the resistive sensor. Since the output of the dual slope resistance to digital converter (DSRDC) is dictated only by the magnitudes of a pair of dc reference voltages, a fixed value resistor and the transformation constant of the sensor, the error in the output is minimal. Hence, a high level of linearity and accuracy is achieved. Simulation studies establish the efficacy of the proposed scheme.**

Keywords— Dual Slope digital converter; Resistance to Digital Converter; Resistive sensor; Strain Gage; Resistance Temperature Detector (RTD)

I. INTRODUCTION

As digital systems provide greater processing power and better user interface compared to analog systems, instrumentation systems are invariably implemented in the digital domain. Interfacing a transducer possessing an analog output to a digital instrumentation system requires the use of an analog to digital converter (ADC) [1]. It would be advantageous if an ADC is designed such that it accepts element(s) of a sensor directly as input and provides a linear digital output. Such an arrangement would obviate the need for intermediate analog signal conditioning circuitry and result in digital output transducers. ADCs that can directly operate on sensor elements are called 'direct digital converters'. Direct digital converters would be more compact and robust as the number of components and hence the complexity gets reduced. Reduced complexity and components also lead to reduced errors and increased reliability. Some of the earlier attempts in this direction resulted in capacitance or resistance to frequency / time-period converters [2]-[5] and direct capacitance to digital converters [6], [7]. Owen has proposed a direct resistance to digital converter (RDC) suitable for a differential type resistive sensor that requires four integration periods (T_A, T_B, T_C and T_D - while T_A and T_C are set, T_B and T_D are measured) and a complex arithmetic and logic unit to compute the output as $(T_B - T_D)/(T_B + T_D)$ [8]. An improved direct resistance to digital converter (RDC) suitable for differential resistive sensors that avoids subtraction; employs a simple up-down counter and obtains the final output with only three integrations [9], instead of the four required in Owen's method and another using only two integrations [10] were also proposed earlier. However, none of the methods proposed so far can handle single active resistive sensors, such as a Resistance Temperature Detector (RTD) or strain gage.

In this paper, a dual slope, direct resistance to digital converter (DSRDC) suitable for use with a single resistive sensor is proposed. Since the method proposed here is based on the dual slope principle, it possesses all the attendant advantages and limitations.

II. THE DUAL SLOPE RESISTANCE TO DIGITAL CONVERTER

In the proposed DSRDC, the resistance of the integrator in a conventional dual slope ADC is replaced with two resistances R_1 and R_2 as shown in Fig. 1. Here, R_1 is the resistance of a single element sensor (a strain gage or a resistive temperature device (RTD) or a potentiometer) and can be expressed as:

$$R_1 = R_0 (1 + kx), \tag{1}$$

where k is the transformation constant and R_0 is the nominal value of the resistance of the sensor when x, the physical quantity being sensed is zero. R_2 is chosen to be a fixed resistance having a value equal to R_0, the nominal value of the resistance of the of the sensor. One terminal each of R_1 and R_2 are tied together and the common terminal thus formed is connected to the inverting input of the opamp OA as indicated

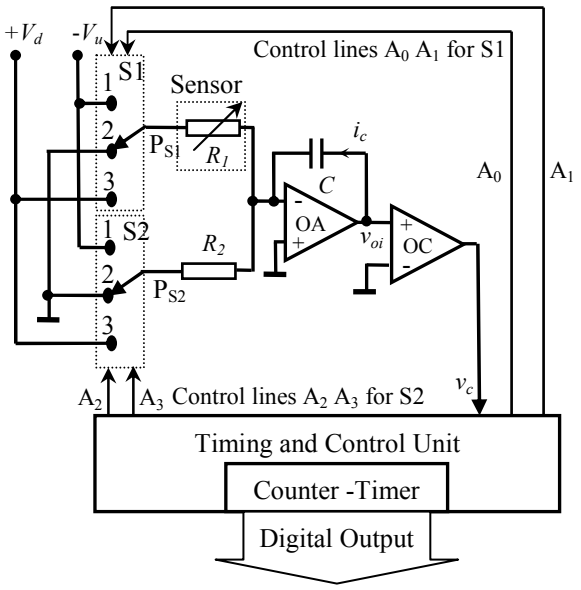

Fig. 1 Block Schematic of the proposed DSRDC

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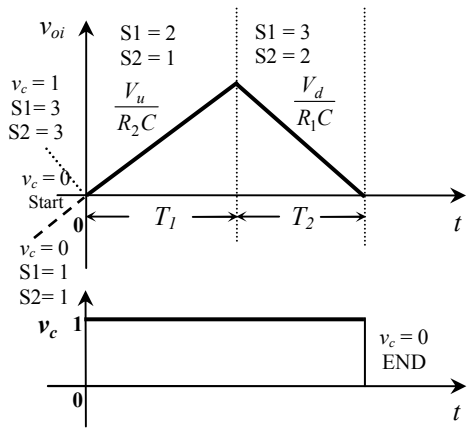

Fig. 2 Waveform of the integrator output v_{oi} for a complete conversion.

in Fig. 1. The free end of R_1 is connected to the output P_{S1} of a single-pole three way switch S1. Similarly the free end of R_2 is tied to the output P_{S2} of another single-pole three way switch S2. Digital control lines A_0 and A_1 control switch S1. Similarly A_2 and A_3 control S2. If A_0 A_1 is "01" then position 1 is selected on switch S1 and $-V_u$ is applied to R_1. If A_0 A_1 is "11" then position 3 is selected and $+V_d$ is applied to R_1. If A_0 A_1 is "10" then position 2 is selected and R_1 is grounded. Similarly lines A_2 and A_3 switch $-V_u$ (A_2 A_3 = "01") or $+V_d$ (A_2 A_3 = "11") or ground (A_2 A_3 = "10") to R_2. The voltages $+V_d$ and $-V_u$ are two stable reference dc voltages, equal in magnitude ($V_u = V_d = V_R$) but of opposite polarity. Hence the sensor becomes an integral part of the integrator (realized with opamp OA and feedback capacitor C) in the DSRDC. The output of the integrator, v_{oi} is fed to a comparator (OC) which functions as a zero-crossing detector. If the output of the integrator is positive ($v_{oi} \geq 0$) then the comparator output (v_c) would be "1" (high); else v_c will be "0" (low). The output of the comparator v_c is fed as input to a timing and control unit (TCU). The TCU is made of a logic unit that senses v_c and sequences two integrations by suitably controlling switches S1 and S2 through signals A_0 A_1 and A_2 A_3. As in a dual slope technique, in the proposed DSRDC also the first integration period is set and the time period of the second integration is measured employing a timer-counter incorporated into the TCU. A conversion is preceded by an "auto zero phase".

A. Auto zero phase

In the auto zero phase, the TCU senses the comparator output v_c. If v_c is high then both A_0 A_1 and A_2 A_3 are set as "11" (both S1 and S2 are set at position 3) thus connecting $+V_d$ to both R_1 and R_2. Hence the integrator output is made to ramp down to zero as shown in Fig. 2. On the other hand, to start with, if v_c is low, then both S1 and S2 are set to position 1 (A_0 A_1 and A_2 A_3 are set as "01"), connecting $-V_u$ to R_1 and R_2, forcing the integrator output to ramp up towards zero. In either case, the integrator becoming zero is indicated to the TCU by a transition (high to low in the former case and low to high in the latter) on v_c, annunciating the end of the auto zero phase. The logic for the auto zero phase is shown in the form of a flowchart in Fig. 3

B. Conversion phase

At the end of the auto zero phase, indicated by a transition on v_c, the TCU starts the first integration period of a measurement cycle. During the first integration period, the TCU sets S1 to position 2 (A_0 A_1 = "10") and S2 to position 1 (A_2 A_3 = "01"), thus grounding R_1 and connecting $-V_u$ to R_2. This condition is maintained for a pre-set period of T_1 s. During T_1, a current $i_c = (V_u/R_2)$ is injected into the feedback capacitor C by the opamp OA and C would be charged with a positive polarity on the terminal that is connected to the output of the opamp OA. Hence the opamp output will ramp up with a positive slope (V_u/R_2C), as shown in Fig. 2.At the end of T_1, the integrator output will be positive and the output of the comparator v_c will be "1" as indicated in Fig. 2. At t = T_1, the timing and control unit senses the comparator output v_c. If v_c is high, then the control unit causes S2 to switch to position 2 (A_0 A_1 are set as "10" thus grounding R_2) and sets S1 to position 3(A_2 A_3 are set as "11"). As a result, the capacitor charging current i_c becomes $-(V_d/R_1)$, causing the integrator output to ramp down with a slope (V_d/R_1C) as shown. The time taken for the output of the integrator to reach zero, say, T_2

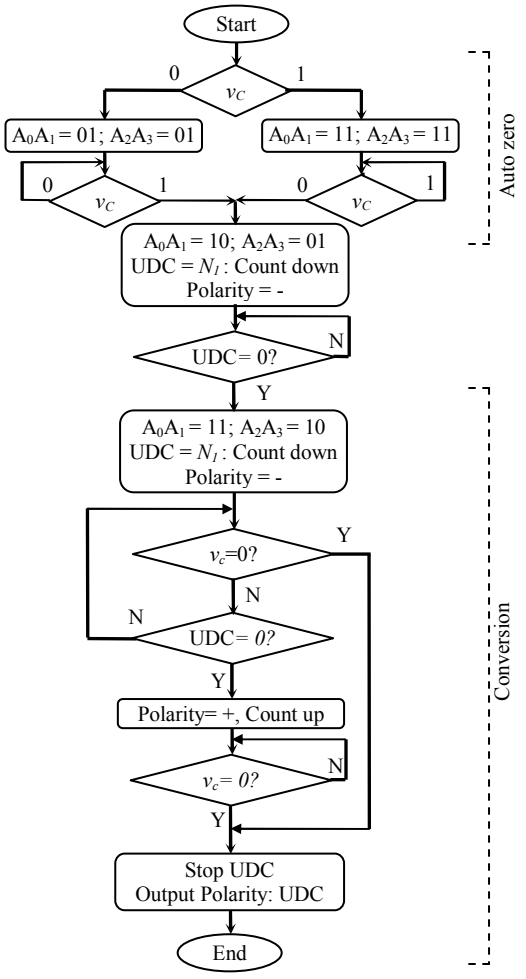

Fig. 3 Flowchart showing the conversion logic of the DSRDC

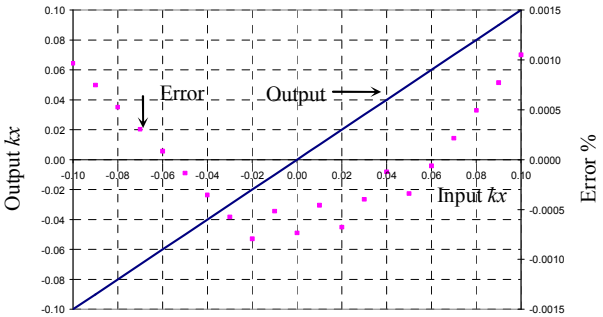

Fig. 4 Results of simulation for a 5000 Ω strain gage

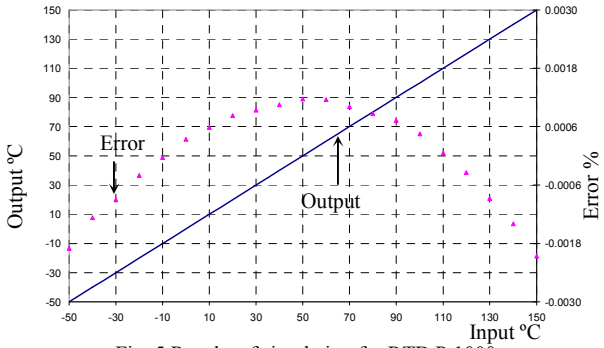

Fig. 5 Results of simulation for RTD Pt1000

is measured. From Fig. 2, we have:

$$\frac{V_u}{R_2 C} T_1 = \frac{V_d}{R_1 C} T_2 \qquad (2)$$

Substituting the values of V_u, V_d, R_1 and R_2 in (2), we get:

$$R_1 T_1 = R_2 T_2 \qquad \Rightarrow \qquad R_0 (1 + kx) T_1 = R_0 T_2$$

Resulting in

$$kx = \frac{T_2 - T_1}{T_1} \qquad (3)$$

From (3), it is easily seen that *kx*, the physical quantity being sensed by the sensor is easily measured in terms of a set time (T_1) and a measured time (T_2) periods. Though (3) involves a subtraction and division, the evaluation of (3) can be easily implemented with simple logic and an up-down counter as shown next. The logic for the conversion phase is also given in the flowchart shown in Fig. 3

III. Results Of Simulation Studies

In order to check the practicality of the DSRDC the proposed scheme shown in Fig. 1 was simulated in PSpice with LF356 serving as the opamp and LM311 as the comparator. The switches were ADG508F. The timing and control unit was implemented utilizing an up-down counter (UDC) and support logic. The clock required for timing was derived from a master clock oscillator with a frequency f_c = 10 MHz. Inititally, the UDC was pre-set in the count down mode, with a convenient number N_1, (say 10,000 for obtaining a 4½ digit output). The first integration period is obtained by making the UDC count down on every clock cycle till the UDC reaches zero, resulting in $T_1 = N_1 T_c$, where $T_c = 1/f_c$. As soon as the UDC reaches zero, the UDC is again pre-loaded with N_1 and the second integration period is commenced, with the polarity of the output taken as negative. If *kx* is negative then $R_1 < R_2$ and hence $T_2 < T_1$ resulting in the transition of v_c occurring before the UDC reaches zero. In such a case, (transition on v_c occurring before UDC reaches zero) the remaining count, say N_0 ($N_0 = N_1 - N_2$, where $T_2 = N_2 T_c$) in the UDC is taken as the output (the polarity is already taken as negative). Then

$$T_c N_0 = N_2 T_c - N_1 T_c = T_2 - T_1$$

On the other hand if the UDC reaches zero before v_c transits from one to zero, immediately (in the same clock period in which zero is reached) the UDC is set to count up and the polarity is set as positive. As soon as v_c transits from one to zero, the UDC is stopped and the content of the UDC is again taken as the output. The entire operational logic of the circuit as illustrated in the flow chart shown in Fig. 3 was implemented using gates and a timer-counter.

Simulations were carried out for strain gage and RTD types of sensors. The strain gage sensor simulated was assumed to have a nominal resistance of 5000 Ω and maximum deviation of ± 10 % ($R_0\, kx_{max}$ = 500 Ω). The output obtained from the simulation and the errors computed therefrom are portrayed in Fig. 4. As expected the errors in the output (after effecting offset and gain compensation) are negligible. Next, a typical RTD sensor with a nominal value of 1000 Ω (Pt1000) was chosen as the sensor and the circuit operation was again simulated. The results for a temperature variation from -50º C to 150 ºC, in steps of 10 ºC are plotted in Fig. 5 and those for the range from 0 ºC to 450 ºC are given in Table 1. Here too, the errors were found to be negligibly small.

IV. Conclusion

A novel dual slope resistance to digital converter (DSRDC) suitable for a single active resistive sensor (such as a strain gage or RTD) is presented in this work. The structure and sequence of integrations of a conventional dual slope ADC are suitably altered so that the ADC accepts the resistive sensor as an integral part of its integrator and provides a linear digital output proportional to the measurand being sensed by the resistive sensor. Since the DSRDC is based on the dual slope principle, all the advantages of the dual slope technique such as high accuracy, tolerance for variations in the parameters of circuit components and immunity to external interference as well as its attendant limitations such as low conversion rate (typically a few conversions to a few hundred conversions per second can be realized) and sensitivity to variations in the reference voltage are applicable to the proposed DSRDC.

TABLE I. RESULTS FOR SIMULATION OF Pt1000

Input (ºC)	T_2 (ms)	Output Temperature (ºC)	Error (%FS)
0	100.032	-0.03	-0.006
50	119.492	49.99	-0.002
100	138.950	100.00	0.000
150	158.407	150.01	0.002
200	177.863	200.01	0.003
250	197.317	250.01	0.003
300	216.770	300.01	0.002
350	236.221	350.00	0.000
400	255.670	399.00	-0.002
450	275.117	449.97	-0.006

Simulation studies on a strain gage sensor and an RTD, namely Pt1000, indicate the practicality of the proposed scheme. The output and the errors obtained through simulation correlate well with the theoretical derivations. Since a couple of dc reference voltages, the value of a fixed resistor and the transformation constant of the sensor are the only parameters that influence the operation of the DSRDC, a high degree of accuracy and linearity is achieved.

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