Modeling Crosstalk Effects in CNT Bus Architectures

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***Abstract*—Carbon nanotubes (CNTs) have been widely proposed as interconnect fabric for nano and very deep submicron (silicon-based) technologies due to their robustness to electromigration. In this paper, issues associated with crosstalk among bus lines implemented by CNTs are investigated in detail. CNT-based interconnects are modeled and the effects of crosstalk on performance and correct operation are evaluated by simulation. Existing models are modified to account for geometries in bus architectures made of parallel single-walled nanotubes and a single multiwalled nanotube. New RLC equivalent circuits are proposed for these bus architectures. A novel bus architecture with low crosstalk features is also proposed. This bus architecture is made of dual-walled nanotubes arranged in parallel. In this architecture, the crosstalk-induced delay and corresponding uncertainty (as well as crosstalk-induced peak voltage) are significantly reduced; a modest area penalty is incurred. Reductions up to 59% for the crosstalk-induced delay and up to 81% for the crosstalk-induced peak voltage are reported. These results confirm that the proposed bus arrangement noticeably improves performance and provides reliable operation.**

***Index Terms*—Bus architecture, carbon nanotube (CNT), crosstalk, fault model, interconnections.**

I. Introduction

GLOBAL interconnects (such as the so-called bus) are widely employed to distribute data, clock, power supply, and ground throughout the entire area of an integrated circuit (IC). At high current density, most materials used in today's interconnects (such as Al and Cu) [1] are affected by electromigration, thus substantially impacting reliability (as measured by the correct operation of the IC). The ITRS Roadmap [2] emphasizes the need for reliable high-speed interconnects for VLSI as well as emerging technologies and suggests the need for innovative materials and process solutions for investigation; moreover, this still remains a very challenging problem due to the tight constraints on the reliable operation and fast operating speed of these ICs. Carbon nanotubes (CNTs) offer unique capabilities due to their conductive, mechanical, and thermal properties [1]. CNTs have been proposed for providing signals for clocking quantum-dot cellular automata (QCA) circuits [3]. These devices can be classified as single-walled nanotubes (SWNTs) and multiwalled nanotubes (MWNTs). SWNTs consist of a single sheet of graphene rolled up into a cylindrical tube that can have a diameter in the nanometer range and a length in the micrometer range [4]. MWNTs consist of two or more SWNTs, which are concentrically wrapped one over the other [4]. Depending on the direction in which they are rolled (referred to as chirality), CNTs can behave either as a semiconductor or a conductor [5]. Semiconductive nanotubes can be employed for the channel of carbon nanotube field-effect transistors (CNFETs) [6]. Conductive (or metallic) nanotubes are envisioned as ideal interconnect devices for emerging technologies at nano scale as well as for today's very deep submicron (silicon-based) electronics [6]–[12].

Despite their potential, only recently research has been reported on nanotube-based interconnects [7]–[10], [12]–[18]. In particular, the problem of possible crosstalk coupling between bus lines has not been analyzed; yet, it is well known that their impact on performance and correct operation is very pronounced. As for conventional interconnects (using materials such as Al and Cu), crosstalk coupling may cause signal delays, speed-ups, and glitches (usually referred to as crosstalk noise) [19]. The delay due to crosstalk negatively impacts performance, while crosstalk noise constitutes a serious problem for reliable operation of an interconnect [20]. Crosstalk can result in a glitch that, depending on its duration and amplitude, may be propagated to the output of a bus receiver, thus causing a logic error at the output of the sampling (receiving) device. Correct operation may then be affected. As for crosstalk coupling, line delay depends on the switching activity of adjacent lines, resulting in a crosstalk-induced delay uncertainty, that also may negatively impact reliability [20].

In this paper, crosstalk effects are initially analyzed for different bus architectures implemented by metallic nanotube-based interconnects. First, we consider SWNT interconnects aligned in parallel to form a standard parallel bus architecture. While research has already been pursued for this type of architecture (e.g., [13] and [14]), no research has been reported on the development of multilevel interconnects. A possible approach could be to use MWNTs, as suggested in [21], because they are stacked SWNTs. However, the coupling between the different shells of a MWNT has not been fully understood. Therefore, we propose a novel electrical model for a MWNT with metallic shells and extend this model to a MWNT-based bus architecture.

The model for a SWNT over a ground plane proposed in [15] is initially considered. This model is then extended to coupled SWNTs over a ground plane and to MWNTs (regarded as stacked SWNTs [4]) by calculating the coupling capacitances between adjacent shells and considering the intershell resistance (to account for tunneling conduction between them). Bus architectures which are implemented using parallel SWNTs and

Manuscript received October 26, 2005; revised November 14, 2006. The review of this paper was arranged by Associate Editor D. Frank.

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Digital Object Identifier 10.1109/TNANO.2007.891814

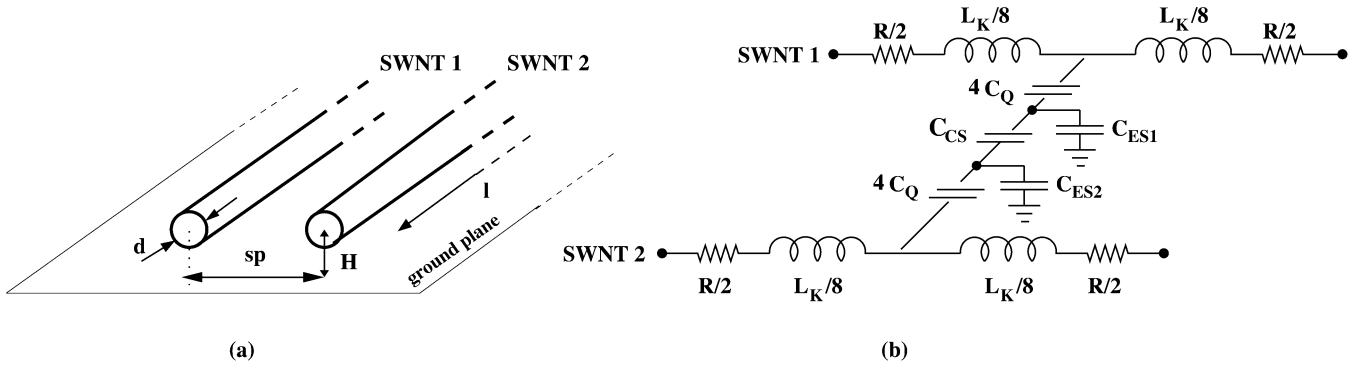

Fig. 1. (a) Geometry of SWNTs in parallel over a ground plane. (b) Equivalent RLC circuit.

single MWNT are analyzed by simulation, using novel RLC equivalent circuits. Finally, a bus architecture made of parallel dual-walled nanotubes (DWNTs) is proposed; a DWNT consists of a MWNT made of two shells. Crosstalk-induced delay, delay uncertainty, and crosstalk-induced peak voltage are significantly reduced (59% for crosstalk-induced delay, and 81% for crosstalk-induced peak voltage) compared with other CNT-based bus architectures.

Similarly to metal-based bus interconnects, also CNT busses may suffer from other sources of noise, such as receiver threshold variation, dc drop, power supply noise, and reflection. In these cases, the analysis requires an accurate modeling of the whole system in which the bus is operational; an appropriate interface to the CNT interconnect must be also provided. However, a model of these types of systems is beyond the scope of this presentation, as this manuscript deals with modeling of crosstalk effects on CNT-based busses.

This paper is organized as follows. In Section II, a brief review of CNT interconnects is presented. The equivalent circuits that are used to model both SWNT and MWNT busses are also presented. Crosstalk effects in CNT-based bus architectures are introduced in Section III. In Sections IV and V, crosstalk effects on bus architectures made of parallel SWNTs and a MWNT are analyzed and simulated. In Section VI, a novel bus architecture is proposed. In Section VII, the proposed bus architecture is compared with other CNT-based bus architectures. Final remarks are given in Section VIII.

II. CNT Interconnects and Models

Next, a brief review of two types of a CNT-based interconnect is presented. Both SWNT and MWNT are considered; interconnect geometries and equivalent circuit models are analyzed in detail.

A. SWNT

Consider initially the bus architecture made of two parallel SWNTs shown in Fig. 1(a), where d denotes the diameter of the nanotubes, sp is the spacing between nanotubes, H is the distance to the ground plane, and l is the length of the nanotube. Its electrical model can be established following the procedure reported in [15] and developed for a SWNT over a ground plane. This procedure results in the RLC equivalent circuit shown in Fig. 1(b).

Consider, next, each element of this RLC equivalent circuit. A resistance per unit length must be taken into account; this has been included in the model as per the method of [23] in which the resistance per unit length was first calculated theoretically and then experimentally validated. This model includes contact resistances (also called quantum mechanical resistances) and has been utilized for the CNT models proposed in [13]–[15]. As reported in [23], for nanotubes of considerable length (such as those employed for global interconnects considered in this paper), both ballistic and nonballistic transport effects must be taken into account. The resistance of each nanotube depends on the nanotube length l and the power supply voltage (V_{dd}) [23].

For $V_{dd} = 0.5$ V [5], R can be modeled [13]–[15], [23] as

$$R = \begin{cases} \frac{h}{4e^2}, & \text{if } l < \lambda_{\text{high}} \\ \frac{h}{4e^2}\left[\frac{l}{0.64(l-\lambda_{\text{high}})+\lambda_{\text{high}}}\right], & \text{if } \lambda_{\text{high}} < l < \lambda_{\text{low}} \\ \frac{h}{4e^2}\left[\frac{l}{0.64(\lambda_{\text{low}}-\lambda_{\text{high}})+\lambda_{\text{high}}}\right], & \text{if } l > \lambda_{\text{low}} \end{cases} \tag{1}$$

where h is Planck's constant, e is the charge of an electron, and λ_{low} ($\sim 1.6\ \mu$m) and λ_{high} (~ 26 nm) [23] are the mean-free paths of backscattering for low and high biases, respectively.

1) At small length, the resistance is length independent (to reflect the ballistic electronic transport phenomena of nanotubes).
2) At large length, the electronic transport is not ballistic; the increase in resistance with length is caused by scattering mechanisms.
3) At low bias, these scattering mechanisms are mostly due to acoustic phonons that infer a low-bias mean-free path equal to λ_{low}.
4) At high bias, the optical phonons and zone boundary scattering become dominant, thus inferring a high-bias mean free path equal to λ_{high}.

The kinetic inductance (L_K) of Fig. 1(b) originates from charge-carrier inertia, because electrons do not instantaneously react to the applied electric field. This phenomenon can be represented in the proposed model by inserting a series inductance that is given in [18] as

$$L_K = \frac{h}{2e^2 v_F} \tag{2}$$

where v_F is the Fermi velocity of a carbon nanotube. By replacing the symbols in (2) with their respective values, $L_K \approx 16$ nH/μm. A nanotube has four copropagating quantum channels, therefore the effective value of the kinetic inductance in the equivalent circuit is given by $L_K/4$ [18]. In

this model [Fig. 1(b)], the magnetic inductance is neglected. This assumption is valid because the kinetic element dominates (as proved in [18]).

For CNT interconnects, two types of capacitance should be considered between nanotubes, or between a nanotube and the ground plane [18], [24]:

1) electrostatic capacitance that represents the electrostatic coupling between lines, or between a line and the ground plane, as occurring in conventional Al- and Cu-based interconnects;
2) quantum capacitance that physically originates by the finite density of states at the Fermi energy, i.e., a finite amount of energy above the Fermi energy is required to add an extra electron to the system [18].

Consider the case of two coupled SWNTs over a ground plane. The charge of a SWNT is imaged onto both the ground plane and the other (coupled) SWNT. Let ρ denote the charge per unit length of a SWNT. This can be expressed by [15]

$$\rho = (C_{\rm ES} + C_{\rm CS})\frac{-U}{e} \tag{3}$$

where $C_{\rm ES}$ is the electrostatic coupling capacitance between one SWNT and the ground plane, $C_{\rm CS}$ is the electrostatic coupling capacitance between the two SWNTs, U is the electrostatic potential energy, and e is the electron charge. Let x be the transport direction; by combining the previous equation with the current continuity equation $(\partial\rho/\partial t) = -(\partial I/\partial x)$, the following equation is obtained:

$$(C_{\rm ES} + C_{\rm CS})\frac{\partial \Psi}{\partial t} = -\frac{\partial I}{\partial x} \tag{4}$$

where the electrostatic potential is defined as $\Psi = -U/e$ [15].

The total charge of the considered SWNT has contributions from both the coupled electrodes (the ground plane and the other SWNT) and must be supplied by the wire by modulating its finite density of states. Following the procedure of [15] and in accordance with the analysis of [24], the quantum capacitance is effectively in series with a parallel combination of $C_{\rm ES}$ and $C_{\rm CS}$. The same considerations are also applicable to the other SWNT; therefore, this procedure leads to the equivalent circuit shown in Fig. 1(b).

The electrostatic capacitance per unit length between a nanotube and the ground plane is given by [18]

$$C_{\rm ES} = \frac{2\pi\epsilon}{\cosh^{-1}\left(\frac{2H}{d}\right)}. \tag{5}$$

For a typical value of H/d, $C_{\rm ES} \approx 50$ aF/μm [18]. Analogously, the electrostatic capacitance per unit length between two parallel nanotubes (Fig. 1) is given by [24]

$$C_{\rm CS} = \frac{\pi\epsilon}{\cosh^{-1}\left(\frac{sp}{d}\right)}. \tag{6}$$

The quantum capacitance per unit length is given by [18]

$$C_Q = \frac{2e^2}{hv_F}. \tag{7}$$

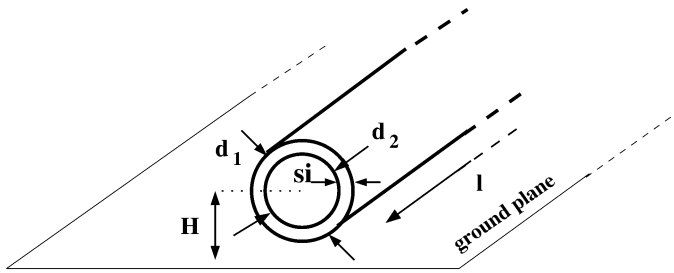

Fig. 2. Geometry of MWNT over a ground plane.

Therefore, $C_Q \approx 100$ aF/μm. A nanotube has four copropagating quantum channels, and the effective value of the quantum capacitance to be considered in the equivalent circuit is $4C_Q$ [18]. For the case of busses made of more than two lines, the coupling capacitance between nonadjacent nanotubes can be neglected [14]. This is valid because the electrostatic coupling between nonadjacent nanotubes is very weak compared to the electrostatic coupling between adjacent nanotubes and dominates when the series quantum capacitance is also considered. Differently from conventional Al and Cu interconnects, there is a quantum capacitance that does not depend on spacing; this considerably reduces the total coupling capacitance between two adjacent nanotubes for small values of spacing.

For simulation purposes, due to the distributed nature of the parameters of the nano interconnect, a classical T model [22] has been employed for the RLC equivalent circuit. As shown in Fig. 1(b), the nanotubes are modeled as parallel coupled nanotransmission lines with distributed resistance R and kinetic inductance $L_k/4$ (in series) divided into two halves (obtaining $R/2$ and $L_k/8$, respectively, as per the T model), with a distributed quantum capacitance $(4C_Q)$, and an electrostatic coupling and bottom capacitance ($C_{\rm CS}$ and $C_{\rm ES}$, respectively).

B. MWNT

Consider the bus architecture implemented by a MWNT over a ground plane, as shown in Fig. 2. d_1 and d_2 denote the diameters of the outer and inner nanotubes, respectively, l is the length, s_i is the intershell spacing, and H is the distance between the center of the MWNT and the ground plane. It is assumed that the distance between each shell is fixed, while the diameter of the outermost nanotube can change over a fixed interval (i.e., a given fabrication process [25] is assumed). For example, in current nanofabrication processes the intershell spacing ($s_i = (1/2)(d_1 - d_2)$ in Fig. 2) is $s_i = 0.34$ nm. So differently from SWNT and current Al or Cu bus architectures, an increase in spacing between adjacent lines cannot be exploited (due to technology limitations) as a possible strategy to reduce crosstalk effects.

Consider the electrical model for MWNT bus architectures. As an MWNT consists of two or more concentric SWNTs (that are geometrically unique and electronically distinguishable from each other [26]), then the model described previously for coupled SWNTs over a ground plane can be also employed for the MWNT structure shown in Fig. 2.

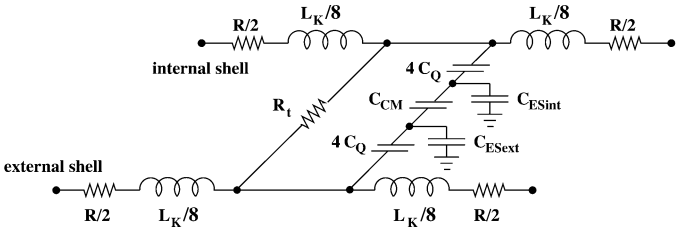

Fig. 3. Equivalent RLC circuit of MWNT geometry of Fig. 2.

Consider the external shell next. It is coupled to both the ground plane and the internal shell. Therefore, following the same procedure as for SWNTs:

$$(C_{\mathrm{ESext}} + C_{\mathrm{CM}})\frac{\partial \Psi}{\partial t} = -\frac{\partial I}{\partial x} \tag{8}$$

where C_{ESext} is the electrostatic coupling capacitance between the external shell of the MWNT and the ground plane, and C_{CM} is the electrostatic coupling capacitance between the two shells. All other parameters are the same as defined previously in (4). Therefore, an analogous equation can be derived for the internal shell. However, the interaction between adjacent shells of an MWNT is different from the one occurring between SWNTs in parallel. There is an intershell resistance between adjacent shells of a MWNT (in addition to a coupling capacitance, electrostatic and quantum), to account for intershell tunnel type transport phenomena [27].

Based on these consideration, and recalling that quantum capacitances are effectively in series with a parallel combination of the electrostatic coupling capacitances versus the ground plane and between the adjacent shells, the RLC equivalent circuit of the MWNT geometry of Fig. 2 is derived, as shown in Fig. 3.

As for the coupling capacitances, it is well known that due to the finite density of states, two-dimensional electron systems cannot completely screen electric fields [28], [29]. However, carbon nanotubes are considered one-dimensional systems [15], [18], [30] and, as shown experimentally in [26], the metallic shells of an MWNT constitute an effective electrostatic shield for the inner shells. The capacitance between the internal shell and the ground plane (C_{ESint} in Fig. 3), or between two nonadjacent shells can be neglected. When considering a metallic MWNT structure, it is therefore assumed that only the outermost nanotube is coupled to the ground plane. The electrostatic capacitance per unit length between the outermost nanotube and the ground plane is given by (5) [18], where d is the diameter of the outermost shell. Similarly to SWNTs, the quantum capacitance is given by (7). As for the electrostatic coupling capacitance between adjacent shells (C_{CM}), its expression is derived from a conventional metallic coaxial configuration [31], i.e.,

$$C_{\mathrm{CM}} = \frac{2\pi\epsilon}{ln\left(\frac{d_1}{d_2}\right)} = \frac{2\pi\epsilon}{ln\left[\frac{d_1}{(d_1-2s_i)}\right]}. \tag{9}$$

The electrostatic and quantum capacitances add inversely, so they are connected in series in the equivalent circuit.

Individual shells are modeled as concentric coupled nanotransmission lines, and for simulation purposes, analogously to the case of SWNTs, a T model has been employed for the RLC equivalent circuit. Each line comprises a distributed kinetic inductance ($L_k/4$) and, as discussed previously, the outermost nanotube presents a distributed (coupling) electrostatic capacitance (C_{ES}) versus the ground plane and a distributed (coupling) electrostatic capacitance (C_{CM}) versus the internal shell. The parallel combination of these two electrostatic capacitances is in series with a quantum capacitance ($4C_Q$). The intershell resistance (R_t) accounts for intershell tunnel transport phenomena [27]. The resistance R and the kinetic inductance L_k are exactly the same as for SWNTs [(1) and (2)]. As for the intershell resistance, it has a typical value of 10 kΩ/μm for intershell spacing values in current technology [27].

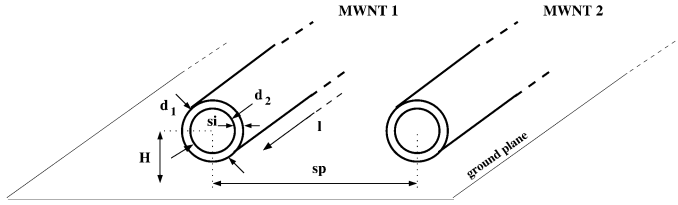

Fig. 4. Geometry of two MWNTs over a ground plane.

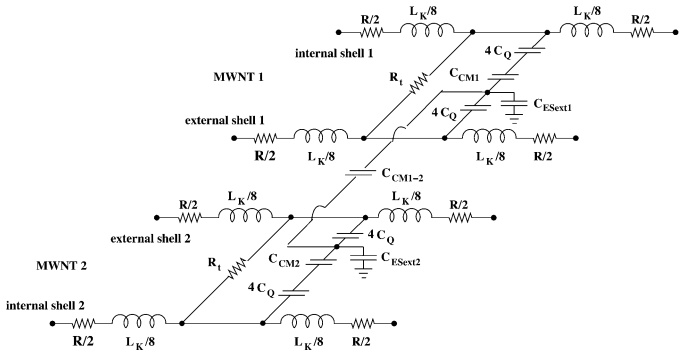

Fig. 5. Equivalent RLC circuit of MWNT geometry of Fig. 4.

Consider now the case of two MWNTs, each made of two shells, over a ground plane (Fig. 4) to derive the equivalent RLC circuit.

As described previously, the metallic shells of an MWNT constitute a very effective electrostatic shield for the inner shells. Therefore, the inner shells of the two MWNTs shown in Fig. 4 can be considered electrostatically coupled only to the respective external shells. Also, coupling capacitances between nonadjacent shells can be neglected. So, consider as an example the external shell of the ith MWNT (for $i = 1, 2$); this is electrostatically coupled to the ground plane (C_{ESexti}), to the internal shell of the ith MWNT (C_{CMi}), and to the external shell of the other MWNT (C_{CM1-2}). Equation (4) can be written as

$$(C_{\mathrm{ESexti}} + C_{CMi} + C_{CM1-2})\frac{\partial \Psi_i}{\partial t} = -\frac{\partial I_i}{\partial x}, \quad i = 1, 2. \tag{10}$$

According to [15], the quantum capacitance ($4C_Q$) of each external shell can be considered coupled with a parallel combination of the three capacitances of (10). The derived RLC equivalent circuit is shown in Fig. 5.

III. Crosstalk Effects in CNT Bus Architectures

It is well known that crosstalk may induce a delay on coupled lines with negative impact on performance. The delay de-

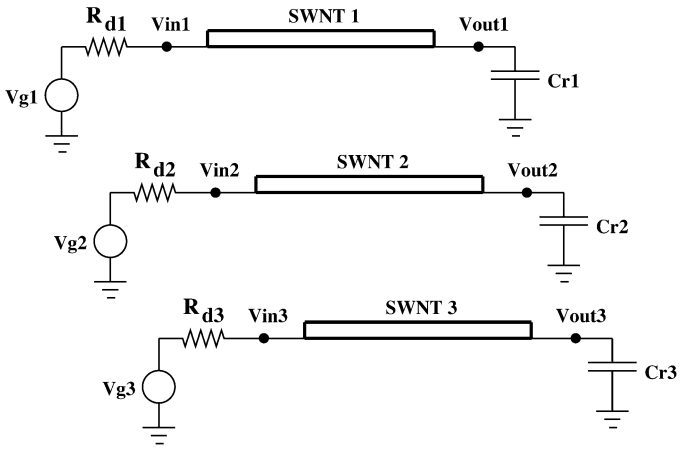

Fig. 6. Three-line bus architecture made of three parallel SWNTs.

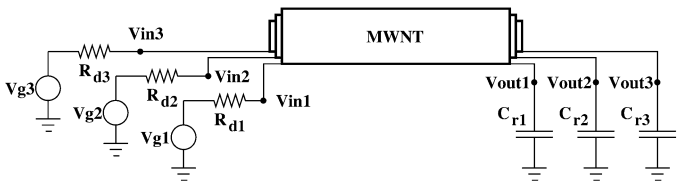

Fig. 7. Three-line bus architecture made of a single MWNT.

pends on several factors, such as the coupling capacitance, the relative strength of the drivers (which may cause different slew rates in the signals), and the relative transition time skew. Moreover, crosstalk may cause an undesired voltage glitch on a bus line (usually referred to as crosstalk noise [32]) due to the transition in one or more adjacent bus lines (the amplitude and duration of this voltage glitch also depend on the factors indicated above). Therefore, crosstalk negatively impacts reliability [20], [32], [33], because the correct operation of the interconnect can be affected.

In the analysis presented in this paper, the simple cases of a three-line bus architecture implemented by parallel SWNTs and a MWNT (as shown in Figs. 6 and 7, respectively) are considered. As detailed in [7], [8], and [34], the implementation of the MWNT parallel bus shown in Fig. 7 is still confronted with technology-related issues, such as the arrangement by which the connection between each shell and the different signals is accomplished. However, it is expected that as CNT technology matures, MWNT busses can be readily implemented, as at least an alternative to SWNT busses in the years ahead.

The following notation and terminology are used: τ_{dw} and τ_{db} denote the worst and best case delay, respectively; $\Delta\tau_d$ denotes the delay uncertainty [20]. The delay uncertainty is defined as the difference between the worst case and the best case delay $(\Delta\tau_d = \tau_{dw} - \tau_{db})$. The worst case delay typically occurs when the aggressors switch in the opposite direction of the victim line; the best case delay typically occurs when the aggressors switch in the same direction as the victim line. Consider the central (victim) line; electrical level simulations have been performed using HSPICE to evaluate the following features:

1) crosstalk-induced delay for different transitions of the two adjacent (aggressor) lines;
2) crosstalk-induced peak voltage for the simultaneous transition of the two adjacent (aggressor) lines when the victim line should be in a steady state.

TABLE I
POSSIBLE SWITCHING CONDITIONS OF AGGRESSORS

	V_{in1}	V_{in2}	V_{in3}	$SF_{1,2}$	$SF_{2,3}$
C. 1	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	0	0
C. 2	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	0 / 1	0	1
C. 3	0 / 1	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	1	0
C. 4	0 / 1	$0 \rightarrow 1$ $(1 \rightarrow 0)$	0 / 1	1	1
C. 5	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$1 \rightarrow 0$ $(0 \rightarrow 1)$	0	2
C. 6	$1 \rightarrow 0$ $(0 \rightarrow 1)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	2	0
C. 7	$1 \rightarrow 0$ $(0 \rightarrow 1)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	0 / 1	2	1
C. 8	0 / 1	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$1 \rightarrow 0$ $(0 \rightarrow 1)$	1	2
C. 9	$1 \rightarrow 0$ $(0 \rightarrow 1)$	$0 \rightarrow 1$ $(1 \rightarrow 0)$	$1 \rightarrow 0$ $(0 \rightarrow 1)$	2	2

The bus line delay has been considered for comparison; in this evaluation, the delay due to the bus drivers has not been considered because it is the same for all architectures, i.e., irrespective of their structure. For simulation, the bus drivers have been modeled as linear devices made of ideal voltage generators with series resistances representing the conductance of each driver (R_{di} in Figs. 6 and 7) [32]. The bus line load capacitances (C_{ri} in Figs. 6 and 7) have been also considered; they represent the input capacitances of the bus receivers. Both drivers and receivers are implemented by carbon nanotube field-effect transistors (CNTFETs) with the following values of resistance (R_{di}), input capacitance (C_{ri}), and power supply voltage (V_{dd}) : $R_{di} = 40$ kΩ, $C_{ri} = 10$ aF, with $i = 1, 2, 3$, $V_{dd} = 0.5$ V. These values have been extracted from the CNT device characteristics given in [5]. Finally, the following assumptions are also applicable.

1) The drivers have the same strength and switch simultaneously.
2) The bus signals have the same slew rate.

As for the crosstalk-induced delay on the victim line, it is possible to identify nine different cases for the transitions of the two aggressors; they differ in the total effective capacitance to be charged (discharged) by the driver of the victim line [35]. Let $C_{\mathrm{Ctot1,2}}$ and $C_{\mathrm{Ctot2,3}}$ denote the physical coupling capacitances between the victim (line 2) and the aggressors (lines 1 and 3), respectively; the values of the effective coupling capacitances to be charged (discharged) by the victim driver are given by: $C^{\mathrm{eff}}_{\mathrm{Ctot1,2}} = SF_{1,2} \times C_{\mathrm{Ctot1,2}}$ and $C^{\mathrm{eff}}_{\mathrm{Ctot2,3}} = SF_{2,3} \times C_{\mathrm{Ctot2,3}}$. The coefficients $SF_{1,2}$ and $SF_{2,3}$ are referred to as the *switching factors* and can take integer values of 0, 1, and 2, depending on the transitions of the lines. The effective coupling capacitance of the victim line to be charged (discharged) by the victim driver corresponds to nine cases, as reported in Table I. Arrows represent transitions between the two logic values, while "0/1" denotes that the line is held steady, with a low or high logic value.

The worst case has been considered for the evaluation of the crosstalk-induced peak voltage. This occurs when both aggressors switch simultaneously in the same direction, while the victim line should be steady.

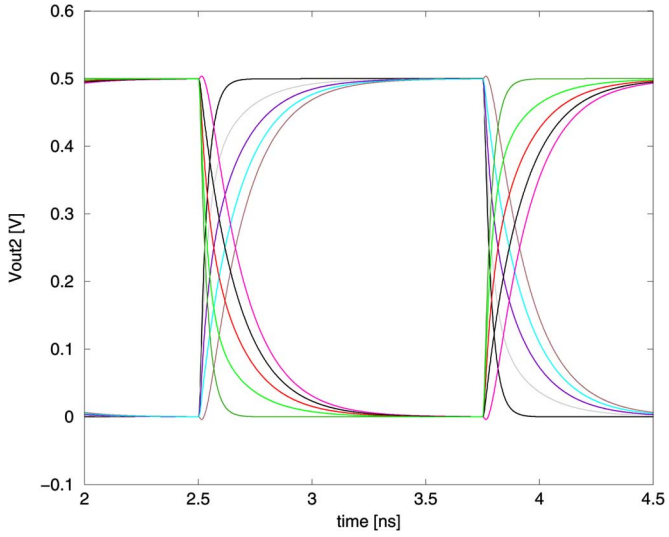

Fig. 8. Eye diagram for three-line bus architecture made of parallel SWNTs.

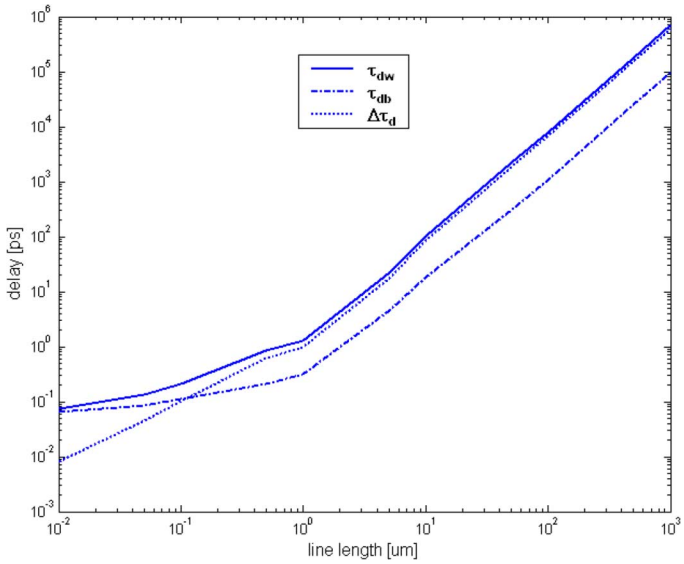

Fig. 9. Crosstalk-induced delay characteristics for three-line bus architecture made of parallel SWNTs, as function of nanotube length.

IV. Crosstalk in Parallel SWNT Bus Architecture

The evaluation of the crosstalk effects in terms of both crosstalk-induced delay and peak voltage is reported for a bus architecture made of three parallel SWNTs (Fig. 6). Simulation has been performed by considering a bus frequency of 800 MHz, a spacing between bus lines of 2 nm, a line length of 10 μm, and a diameter of 1 nm. The latter value represents the smallest SWNT diameter allowed by current nanotechnology [30].

Under these conditions, the nine cases reported in Table I have been verified; simulation has shown that five delay conditions may occur (this number is lower than expected due to the symmetry in the bus architecture). Moreover, these delay conditions are substantially different in the effective coupling capacitance to be charged by the victim line (whose value is affected by the Miller effect [36]); $C^{\text{eff}}_{\text{CtotS}}$ ranges from 0 F (when the victim and the two aggressors switch in the same direction), up to $4C_{\text{CtotS}}$ (when the victim and the aggressors switch in opposite directions). Fig. 8 shows the eye diagram obtained by simulation. The fastest transitions occur for simultaneous switching of the victim and the aggressors in the same direction ($C^{\text{eff}}_{\text{CtotS}} = 0$ F, because the victim driver must charge only the capacitance to the ground plane); the slowest transitions occur in the case of simultaneous and opposite transitions of the victim and both aggressors ($C^{\text{eff}}_{\text{CtotS}} = 4C_{\text{CtotS}}$, because the victim driver must charge the coupling capacitance up to its effective maximum value).

As for the crosstalk-induced delay in the worst and best cases (τ_{dw} and τ_{db}) and the delay uncertainty ($\Delta\tau_d$), the following values were experimentally obtained: $\tau_{dw} = 103.1$ ps, $\tau_{db} = 18.5$ ps, and $\Delta\tau_d = 84.6$ ps. $\Delta\tau_d$ is 82% of τ_{dw}, which indicates a large uncertainty in the signal propagation delay through the simulated bus architecture with negative impact on reliable operation [20]. Fig. 9 shows the variation of τ_{dw}, τ_{db}, and $\Delta\tau_d$, as function of line length l. The slope of the curves changes at $l \simeq 1$ μm; for $l > 1$ μm, the delay starts to noticeably increase as function of line length. This is due to the rapid increase in resistance, kinetic inductance, and coupling capacitances. For example, at $l = 1$ mm, the worst case delay τ_{dw} approximates

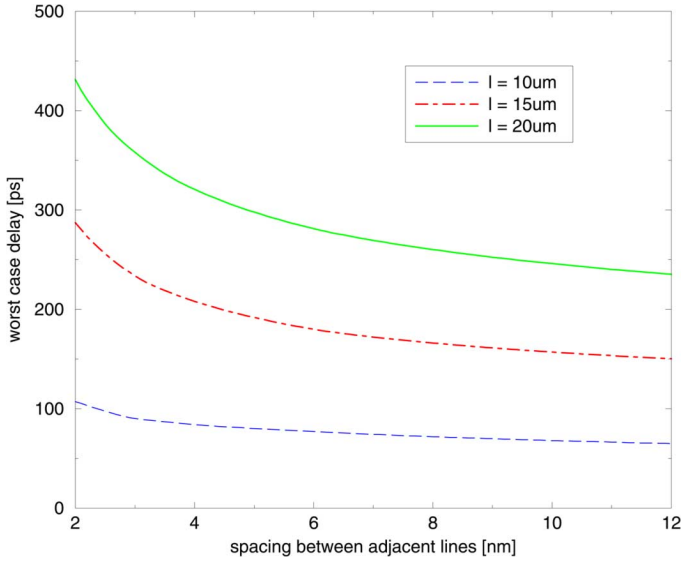

Fig. 10. Crosstalk-induced delay in worst case for three-line bus made of parallel SWNTs, as function of spacing between lines and for different line lengths.

700 ns; this makes it unfeasible to use of this type of bus architecture for long global interconnects in high performance systems. For small values of l, the delay uncertainty $\Delta\tau_d$ is quite low. Due to the difference in effective coupling capacitances, also the delay uncertainty noticeably increases with line length. At $l \geq 1$ μm, it becomes almost equal to the worst case delay and is almost an order of magnitude greater than the best case delay.

Fig. 10 shows the worst case delay (τ_{dw}) as function of spacing (sp) for different values of l. The delay decreases rapidly for spacing values between 2 and 5 nm. For larger spacing, the delay decreases asymptotically to a constant value. Therefore, similarly to Al and Cu interconnects, the delay due to crosstalk can be significantly reduced by properly setting the spacing between adjacent bus lines.

Finally, Fig. 11 shows the peak voltage induced on the victim line (which is supposed to be steady at zero) by the simultaneous

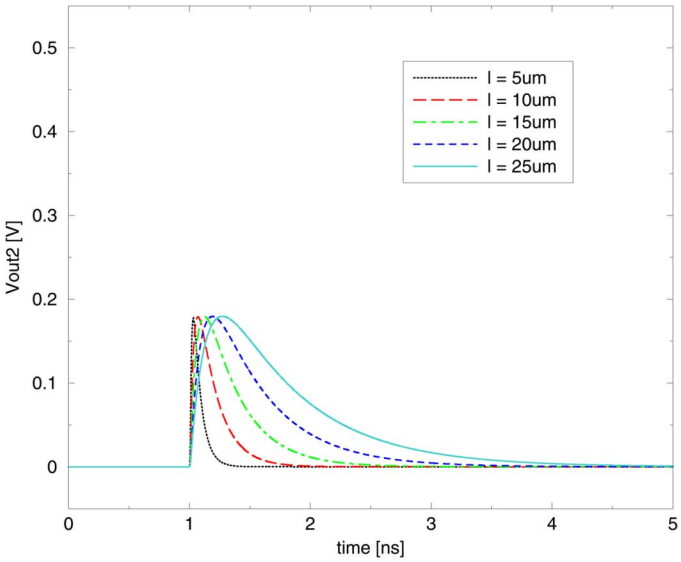

Fig. 11. Crosstalk-induced peak voltage for three-line bus architecture made of parallel SWNTs.

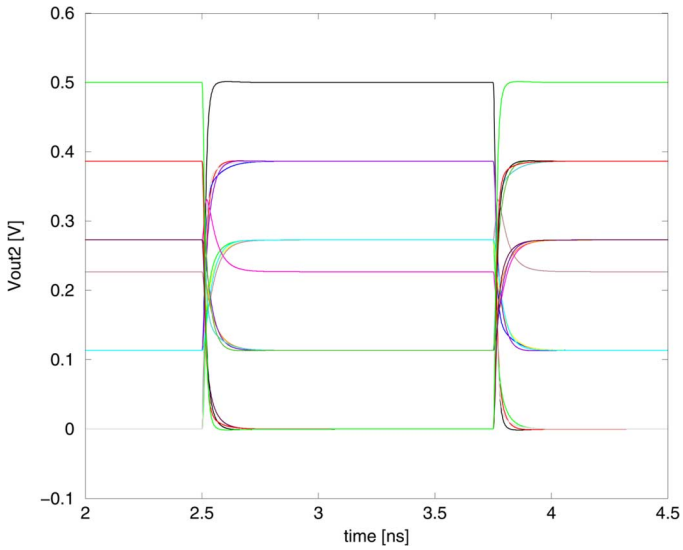

Fig. 12. Eye diagram for three-line bus architecture made of a single MWNT.

switching of the aggressors in the same direction (0→1, in this example), for several values of line length.

By increasing the line length, initially the peak amplitude and duration increase too. For higher values of length, the glitch amplitude saturates at a level slightly below 0.2 V, while an increase in duration is still applicable. Therefore, for the case of symmetric receivers, and sampling elements with a threshold voltage $\simeq V_{dd}/2 = 0.25$ V, the induced peak voltage will never reach the threshold voltage of the receivers. By considering also the receiver filtering ability, the glitch at the output will never reach the logic threshold of the input gates of the sampling elements. Therefore, differently from the case of crosstalk in Al and Cu interconnects, the induced peak voltages will not produce a logic error at the output of the receiver sampling elements. Thus, SWNT bus architectures are more reliable than Al and Cu interconnects, because operation cannot be affected by crosstalk noise.

V. Crosstalk in MWNT Bus Architecture

Consider next a MWNT bus architecture; the MWNT is made of three coaxial SWNTs, as shown in Fig. 7. Both the crosstalk-induced delay and peak voltage have been evaluated by considering the same bus frequency and line length as for the SWNT architecture of the previous section. The diameter of the outermost nanotube has been assumed to be equal to the smallest value as allowed by current nanotechnology, i.e., 2 nm [9].

Under these conditions, the nine cases reported in Table I have been verified through simulation; in this architecture, nine different delay conditions are observed, as well as three different voltage noise margins. This latter condition occurs because, differently from SWNT bus architectures, there is a resistive path between adjacent bus lines that can produce an electrical conflict when these lines present different voltage values. The former condition occurs because, differently from symmetric SWNT bus architectures, the total coupling capacitance between the central line and the outermost line $(C_{\mathrm{CtotM1,2}})$ is greater than the total coupling capacitance between the central line and the innermost line $(C_{\mathrm{CtotM2,3}})$. For example, the case of an aggressor that switches simultaneously in the same direction as the victim line (while the other aggressor line is quiet), results in two different delay conditions (they depend on the switching characteristics of the two aggressors). Despite this asymmetry, the worst case delay and the worst case for voltage margins originate when the outermost and innermost lines switch simultaneously and in opposite direction with respect to the center line (as victim).

All voltage noise margins are different for the number of lines that present a different voltage value from the victim line (i.e., 0, 1, or 2). For the case of aggressors switching in the opposite direction with respect to the victim, noise margins are considerably reduced making it almost impractical for the implementation of an MWNT bus. However, for completeness, the crosstalk analysis is also presented for this type of bus architecture. Therefore, assume also that for the case of reduced noise margins, the receiver can distinguish a high from a low logic voltage.

Then, all analyzed delay conditions are different for the effective coupling capacitance to be charged by the victim line; moreover, its value is considerably affected by the Miller effect [36]. $C^{\mathrm{eff}}_{\mathrm{CtotM}}$ ranges from $0F$ (when the victim line and the aggressors switch in the same direction) up to $(2C_{\mathrm{CtotM1,2}} + 2C_{\mathrm{CtotM2,3}})$, when the victim line and the aggressors switch oppositely. Fig. 12 shows the eye diagram obtained by simulation. The fastest transitions occur due to the simultaneous switching of the victim line and the aggressors in the same direction $\left(C^{\mathrm{eff}}_{\mathrm{CtotM}} = 0\,\mathrm{F}\right)$, while the slowest transitions occur due to the simultaneous and opposite transitions of the victim line and both aggressors $\left(C^{\mathrm{eff}}_{\mathrm{CtotM}} = 2C_{\mathrm{CtotM1,2}} + 2C_{\mathrm{CtotM2,3}}\right)$. For the case of opposite transitions of the victim line and both aggressors, the voltage noise margins are considerably reduced; this negatively impacts reliability.

As for the crosstalk-induced delay in the worst and best cases (τ_{dw} and τ_{db}), and the crosstalk-induced delay uncertainty $(\Delta\tau_d)$, the following values have been found by simulation: $\tau_{dw} = 84.9$ ps, $\tau_{db} = 4.9$ ps and $\Delta\tau_d = 80.0$ ps. $\Delta\tau_d$ is

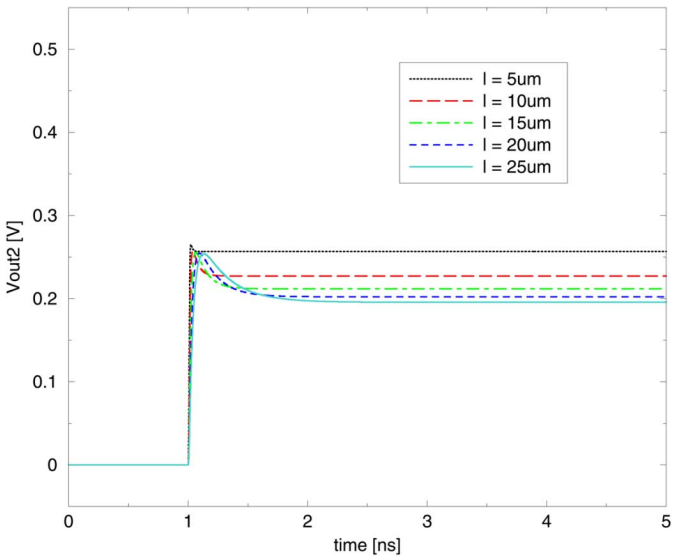

Fig. 13. Crosstalk-induced peak voltage for three-line bus made of a single MWNT.

approximately 94% of τ_{dw}. Therefore, also for this bus architecture, there is a large uncertainty in the signal propagation delay that negatively impacts reliability [20].

Similar to the SWNT case, the delays start to increase noticeably for $l > 1$ μm. However, depending on the length of the lines (ranging from 1 μm to 1 mm), τ_{dw} is 15%–45% lower than the τ_{dw} obtained for the SWNT architecture. In the MWNT bus architecture, $\Delta\tau_d$ represents a greater percentage of τ_{dw} than for SWNT bus architectures. Additionally, the crosstalk-induced delay cannot be reduced by increasing the spacing between bus lines; this is different from SWNT and current Al and Cu interconnects, because, as discussed in previous sections, spacing between adjacent MWNT shells is fixed by process technology.

Fig. 13 shows the voltage induced on the victim line (which is supposed to be steady at zero) by the simultaneous switching of the aggressors in the same direction (0→1, in this example) for several values of nanotube length. A glitch of short duration is now present at the instant of the transition and then, differently from SWNT bus architectures, the line remains constant at a different voltage value due to the intershell resistance. As the line length increases, the peak duration of the glitch increases too, while its amplitude, approximately constant, slightly overcomes 0.25 V.

For the general case of symmetric receivers and receiver sampling elements with a threshold voltage $\simeq V_{dd}/2 = 0.25$ V, the induced constant voltage overcomes the threshold voltage of the receiver for lines shorter than 5 μm, resulting in a logic error at the output of the receiver sampling element. For lines longer than 5 μm, instead, only the glitch produced at the instant of the transition may overcome the threshold voltage of the receiver. So despite the receiver filtering ability, the glitch can be present at its output and can also reach the logic threshold of the input gates of the sampling elements connected to the receiver. Therefore, differently from the case of SWNT bus architectures, the induced peak voltage can result in a logic error at the output of the receiver sampling element. Thus, for crosstalk noise, MWNT architectures (as well as Al and Cu interconnects) are less reliable than SWNT architectures, because in the former architecture incorrect operation can occur.

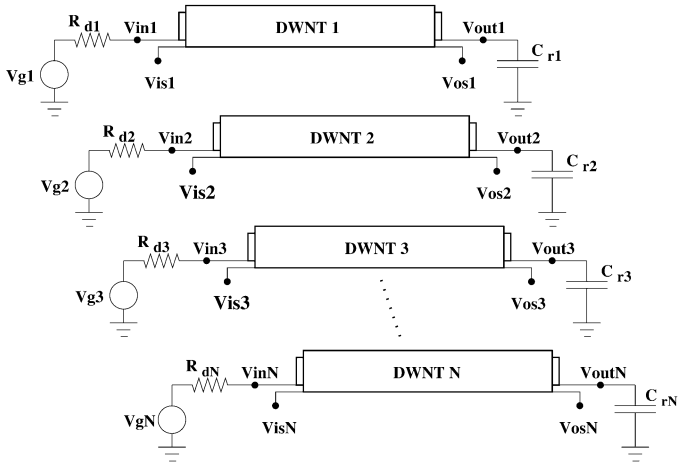

Fig. 14. Proposed DWNT bus architecture.

In summary, due to crosstalk, MWNT bus architectures have a worst case delay that is (15%–45%) lower than SWNT architectures, thus allowing to improve performance. However, there are also significant disadvantages that make this type of multilayer bus implementation not suitable for today's technology, i.e.: 1) the issue of connecting each MWNT shell to different signals has not been fully solved; 2) voltage noise margins are considerably reduced; 3) power consumption is at least twice that for a three-line SWNT bus; 4) the delay uncertainty is increased as a greater percentage of the worst case delay is encountered compared with SWNT architectures; and 5) crosstalk noise and reduced noise margins have negative impacts on reliability.

VI. Proposed Parallel DWNT Bus Architecture

A new bus architecture which reduces the crosstalk effect is proposed (Fig. 14). This architecture consists of N parallel dual-walled nanotubes (DWNTs), and each nanotube carries one bus signal. As DWNTs are MWNTs with two shells, it is assumed that the inner nanotube carries the bus signal (Vin_i), while the outer nanotube is connected to a shielding signal (Vis_i) for crosstalk reduction. Three possible cases are proposed; they differ in the shielding signal, thus allowing different levels of crosstalk reduction but at the expense of bus power consumption and implementation difficulty.

In particular, electrical level simulation has been performed for each of the proposed bus implementations by using HSPICE. As an example, the case of a three-line bus has been considered. For each implementation the crosstalk effects (in terms of both crosstalk-induced delay and peak voltage) have been evaluated. Simulations have been performed at a bus frequency of 800 MHz, a spacing between adjacent DWNTs of 4 nm, and a DWNT length and diameter of 10 μm and 2 nm, respectively (as permitted by current nanotechnology [9]). The total coupling capacitance between the outermost shells of adjacent DWNTs has been modeled as for the SWNT parallel bus (Section II).

A. Case 1

Assume that the shielding signal of each DWNT for the three-line bus is connected to ground. Then, the nine different cases

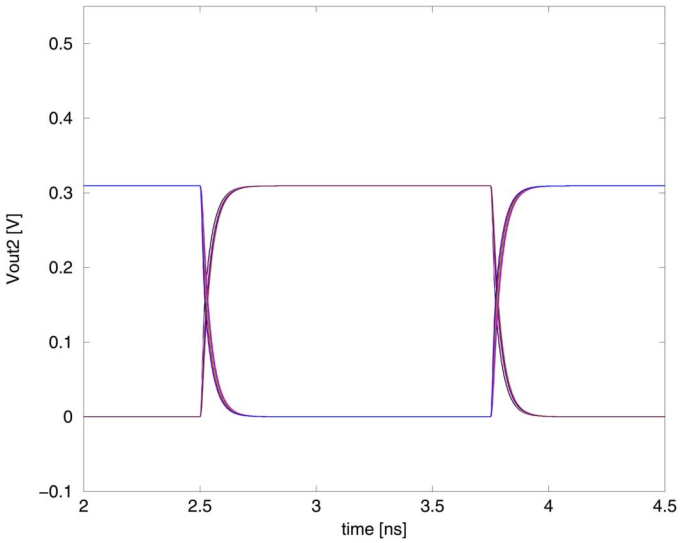

Fig. 15. Eye diagram for three-line DWNT bus for case of shielding signal connected to ground.

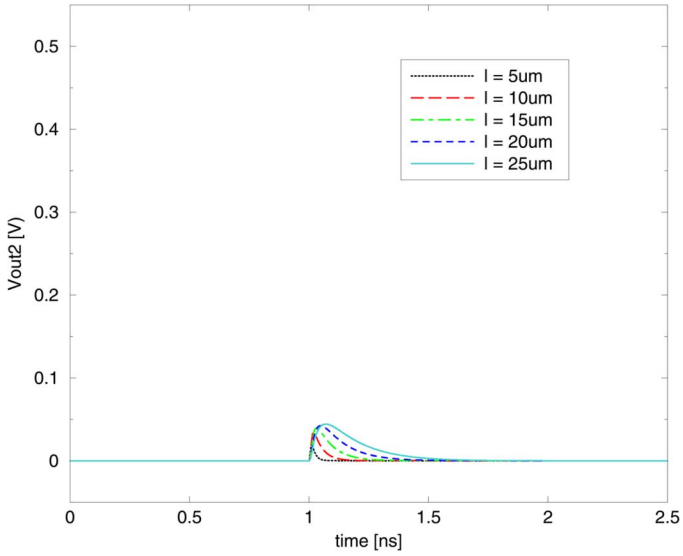

Fig. 16. Crosstalk-induced peak voltage for proposed three-line bus architecture (Case 1).

of Table I result in five different delay conditions; they differ slightly due to line shielding. Fig. 15 shows the eye diagram obtained by simulation. The delay of the victim line is almost equal in all nine cases. This occurs because the external shells shield the inner ones by allowing bus lines to be almost capacitively isolated with other lines. Moreover, due to the intershell resistance, the signal voltage swing is reduced from the expected 0.5 V to only 0.3 V. This implies a voltage noise margin reduction and should be taken into account when designing the receiver to possibly use this bus architecture.

As for the crosstalk-induced delay in the worst and best cases (τ_{dw} and τ_{db}), and the crosstalk-induced delay uncertainty ($\Delta\tau_d$), the following values have been found by simulation: $\tau_{dw} = 55.2$ ps, $\tau_{db} = 45.9$ ps, and $\Delta\tau_d = 9.3$ ps. Therefore, $\Delta\tau_d$ is approximately 17% of τ_{dw}; this indicates a very small uncertainty in the signal propagation delay for this bus architecture (with consequently beneficial effects on the operation of an IC [20]). Also for this bus architecture, the delay starts to significantly increase with line length for $l > 1$ μm. However, depending on the length of the lines (ranging from 1 μm to 1 mm), τ_{dw} is between 1.2 and 3 times shorter than the τ_{dw} obtained for the bus architecture implemented by parallel SWNTs. This allows this bus architecture to operate at frequencies up to three times higher.

Fig. 16 shows the peak voltage induced on the victim line (that is supposed to be steady at zero) by the simultaneous switching of the aggressors in the same direction (0→1, in this example), for several values of nanotube length. As the line length increases, at first the peak amplitude and duration increase too. For longer length, the glitch amplitude saturates at a level slightly below 0.05 V, while the duration continues to increase. Assuming for this case a receiver with voltage threshold equal to half of the line full swing voltage (i.e., 0.15 V), then the induced peak voltage is always below this value. By considering also filtering at the receiver, the glitch at the output of the receiver will never reach the logic threshold of the input gates of the sampling elements connected to the receiver. Therefore, differently from the crosstalk in MWNT

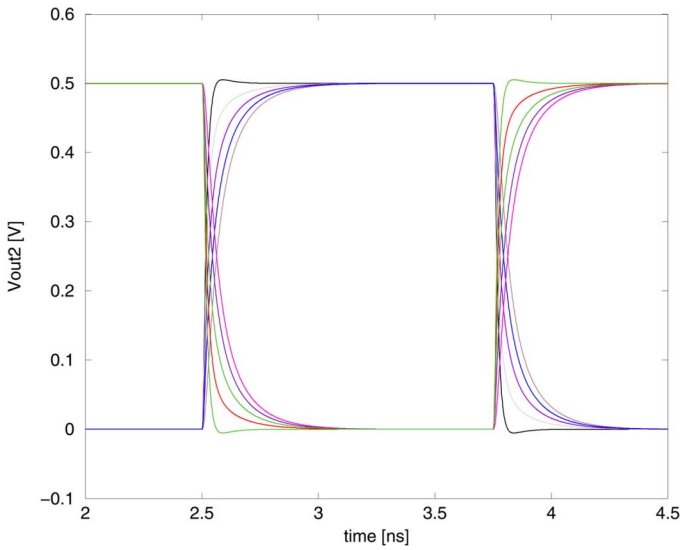

Fig. 17. Eye diagram for three-line DWNT bus for the case of shielding signal connected to a signal replica.

and Al and Cu interconnects, the induced peak voltages will not give rise to a logic error at the output of the receiver sampling element. Thus, by considering crosstalk noise this bus architecture is significantly more reliable than the previous analyzed CNT bus architectures and Al and Cu interconnects. Finally, this bus architecture consumes 44% more power than the SWNT bus.

B. Case 2

Assume that the shielding signal of each DWNT of the three-line bus is connected to a copy of the considered signal, i.e., each bus driver is duplicated and the output is connected to the corresponding shielding signal. Then, the nine different cases of Table I result in five different delay conditions. Fig. 17 shows the eye diagram obtained by simulation. As for the crosstalk-induced delay in the worst and best cases (τ_{dw} and τ_{db}), and the crosstalk-induced delay uncertainty ($\Delta\tau_d$), the following values have been found by simulation: $\tau_{dw} = 42.5$ ps, $\tau_{db} = 7.3$ ps,

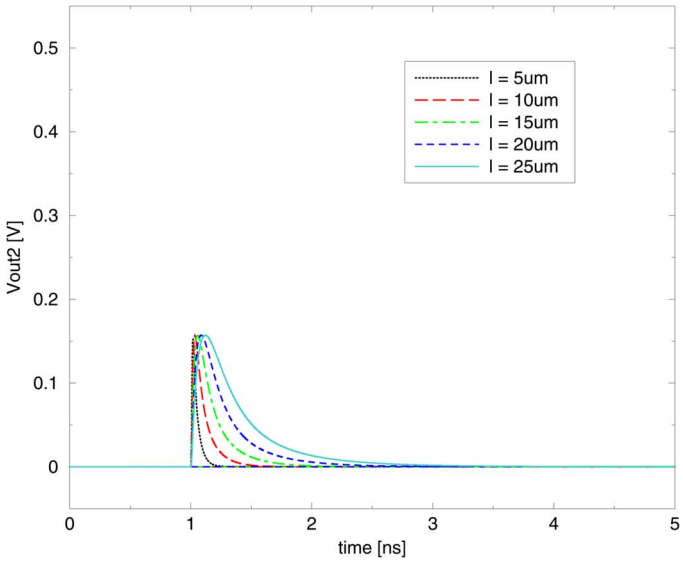

Fig. 18. Crosstalk-induced peak voltage for proposed three-line bus architecture (Case 2).

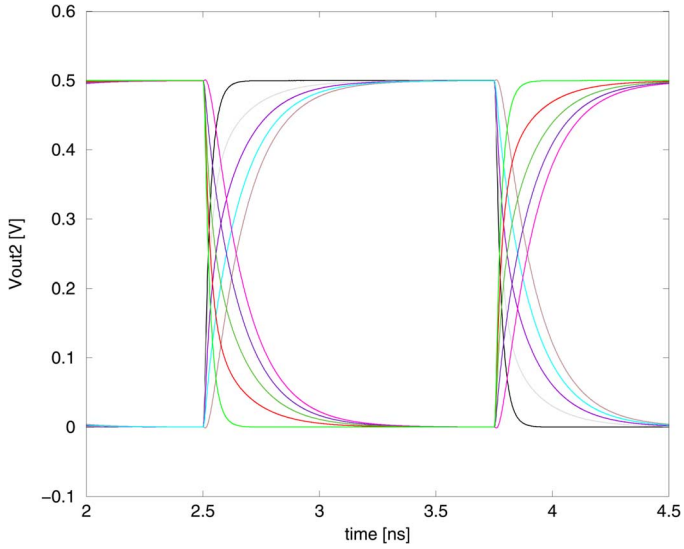

Fig. 19. Eye diagram for three-line DWNT bus for the case of shielding signal connected to input signal by means of a single contact.

and $\Delta\tau_d = 35.2$ ps. Therefore, $\Delta\tau_d$ is approximately 83% of τ_{dw}, which indicates a high uncertainty in the signal propagation delay that negatively impacts reliability. As shown in Fig. 17, the signal voltage swing is not reduced from the expected 0.5 V. Also for this case, the delay starts to significantly increase with line length for $l > 1$ μm. However, depending on the length of the lines (ranging from 1 μm to 1 mm), τ_{dw} is between 1.5 and 3.1 times shorter than the τ_{dw} obtained for the bus architecture implemented by parallel SWNTs. This allows this bus architecture to operate at frequencies up to 3.1 times higher.

Fig. 18 shows the peak voltage induced on the victim line (that is supposed to be steady at zero) by the simultaneous switching of the aggressors in the same direction (0→1, in this example), for several values of nanotube length. As the line length increases, at first the peak amplitude and duration increase too. For longer length, the glitch amplitude saturates at a level slightly above 0.15 V, while the duration continues to increase. This induced peak voltage is therefore 20% lower than for the SWNT bus architecture and always below the threshold voltage of the symmetric receivers ($\simeq V_{dd}/2 = 0.25$ V). Then, the same considerations as for the bus of Case 1 are applicable. Finally, this bus has a power consumption that is only a 9% greater than the SWNT bus.

C. Case 3

Reduced voltage noise margins and increased power consumption with a substantial reduction in crosstalk can be resolved by utilizing the bus implementation of Case 2; however, the difficulty encountered in connecting each shell of the DWNT to different signals still remains [7], [8], [34]. Therefore, assume that it is possible to connect the shielding signal of each DWNT of the three-line bus with the corresponding input signal, i.e., both shells of each DWNT are connected to the same signal by means of a single contact (i.e., $Vin_i = Vis_i$). As proved in [7], [8], and [34], this is possible also in today's technology.

Then, the nine different cases of Table I result in five different delay conditions. Fig. 19 shows the eye diagram obtained by simulation. The following values have been found by simulation

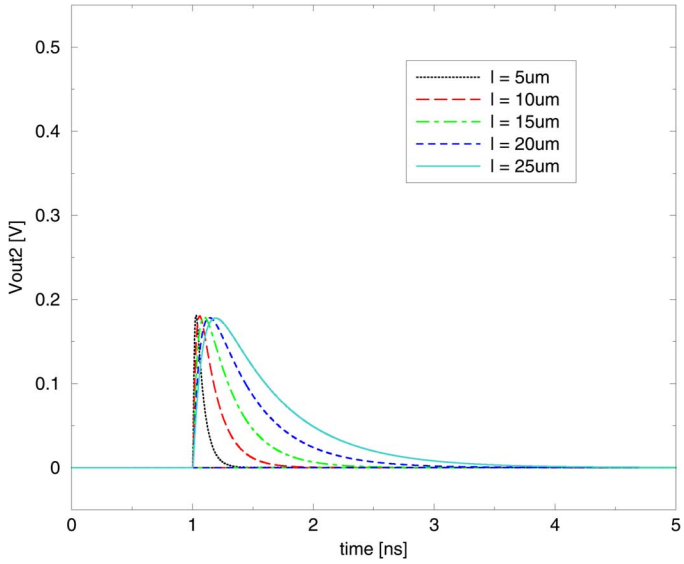

Fig. 20. Crosstalk-induced peak voltage for proposed three-line bus architecture (Case 3).

for the crosstalk-induced delay in the worst and best cases (τ_{dw} and τ_{db}), and the crosstalk-induced delay uncertainty $(\Delta\tau_d)$: $\tau_{dw} = 50.8$ ps, $\tau_{db} = 8.3$ ps, and $\Delta\tau_d = 42.5$ ps. Therefore, $\Delta\tau_d$ is approximately 84% of τ_{dw}, i.e., a high uncertainty is encountered in signal propagation delay. This may negatively impact reliability.

Also in this case, the delay starts to significantly increase with line length of $l > 1$ μm. However, depending on the length of the lines (ranging from 1 μm to 1 mm), τ_{dw} is between 1.6 and 2 times shorter than the τ_{dw} obtained for the bus architecture implemented by parallel SWNTs. This allows this bus architecture to operate at higher frequencies (up to two times).

Fig. 20 shows the peak voltage induced on the victim line (that is supposed to be steady at zero) by the simultaneous switching of the aggressors in the same direction (0→1, in this example), for several values of nanotube length. As the line length increases, at first the peak amplitude and duration increase too. For longer length, the glitch amplitude saturates

TABLE II
COMPARISON BETWEEN BUS ARCHITECTURES

Bus Architecture	Parallel SWNTs	MWNT	Parallel DWNT (Case 1)	Parallel DWNT (Case 2)	Parallel DWNT (Case 3)
Area $[\mu m^2/\mu m]$	0.005	**0.002**	0.01	0.01	0.01
Power Consumption $[nWatts]$	**745**	1583	1075	812	757
τ_{dw} $[ps]$ (for $l = 10\mu m$)	103.1	84.9	55.2	**42.5**	50.8
$\Delta\tau_d$ $[ps]$ (for $l = 10\mu m$)	84.6	80.0	**9.3**	35.2	42.5
Crosstalk-induced peak voltage $[mV]$	182	258	**34**	156	179

at a level slightly above 0.18 V, while the duration continues to increase. This induced peak voltage is slightly lower than for the SWNT bus architecture and always below the threshold voltage of the symmetric receivers ($\simeq V_{dd}/2 = 0.25$ V). Then, considerations similar to those for the busses considered in Case 1 and 2 are applicable. Finally, this bus features a power consumption comparable to the SWNT bus.

VII. COMPARISON OF CNT BUS ARCHITECTURES

A comparison has been performed between all considered and proposed bus architectures. This comparison accounts for area, power consumption, crosstalk-induced delay, delay uncertainty, and crosstalk-induced peak voltage. In the simulations the parameters are the same as those reported in previous sections. Table II summarizes the results (entries in bold identify the best performance). For completeness, we report the results obtained for the MWNT bus, even if, as shown in Section V, its correct operation is not always guaranteed due to the considerably reduced noise margins.

For comparison, the area on the horizontal plane has been considered. From Table II, the proposed bus architecture requires an area which is twice as large as for a bus architecture implemented by parallel SWNTs and five times greater than for a bus architecture implemented by a single MWNT. The advantage in area occupation of the MWNT bus is remarkable; this occurs because only the area of the outermost nanotube is accounted. The significant difference in area between the proposed parallel DWNT and the SWNT bus architectures occurs due to geometry, i.e., the smallest diameters have been considered for both SWNT and MWNT bus architectures (the smallest diameter for a current SWNT fabrication process is equal to 1 nm [30], while for a MWNT it is 2 nm [9]).

For the crosstalk-induced delay, Table II reports the remarkable advantage of the proposed bus architecture over previous ones. The proposed bus architecture features a worst case delay up to 59% (Case 2) shorter than a SWNT bus, and up to 49% (Case 2) shorter than a MWNT bus architecture, allowing to noticeably increase bus speed. As previously introduced, a possible strategy to reduce the crosstalk effects in the SWNT bus is to increase the spacing between adjacent lines. It should be noticed that, by considering the same bus area ($sp = 4.5$ nm for the SWNT bus), the proposed architecture allows a significant reduction (up to 49%) of the worst case delay with respect to the SWNT bus (albeit at a 28% power increase). For the delay uncertainty, the value for the proposed architecture is 17% for Case 1, 83% for Case 2, and 84% for Case 3, of their worst case delay, respectively, while for the SWNT and MWNT buses it is 82% and 94% of their worst case delays, respectively.

Furthermore, from Table II the proposed bus architecture presents a crosstalk-induced peak voltage lower (up to 81%) than for both the SWNT bus and the MWNT bus (for all three cases). Therefore, the probability of crosstalk noise (that may result into logic errors) is much lower in the proposed architecture. Therefore, the proposed bus architecture considerably improves performance and reliable operation of the IC.

VIII. CONCLUSION

The crosstalk effects of different bus architectures implemented by CNT interconnects have been analyzed and evaluated in this paper. An existing model of a SWNT over a ground plane (based on equivalent RLC circuits) has been extended to account for the geometry of different bus architectures. Initially, two bus architectures implemented by parallel SWNTs and a MWNT have been analyzed. We have shown that the MWNT bus architecture has a worst case delay which is 15%–45% lower than the SWNT bus architecture, thus resulting in higher bus performance. However, the MWNT busses may be more difficult to implement due to the still partially resolved issues revolving the connections of the MWNT shells to different signals. Also, voltage noise margins are considerably reduced in this bus architecture and power consumption is more than twice that of a SWNT architecture. As for the delay due to crosstalk, it can be significantly reduced by properly setting the spacing between adjacent lines in a SWNT based bus architecture. By contrast, due to crosstalk noise, the MWNT architecture may result in the generation of logic errors at the output of the sampling elements at the receivers. These logic errors cannot be generated by crosstalk noise in the SWNT bus architecture due to a low induced peak voltage.

A novel bus architecture (with three different implementations) has also been proposed; it consists of DWNTs in parallel. In the proposed architecture, the crosstalk-induced delay and delay uncertainty, as well as the crosstalk-induced peak voltage are significantly reduced (up to 59% for crosstalk-induced delay, and up to 81% for crosstalk-induced peak voltage) compared with previously presented CNT bus architectures. The proposed architecture, however, incurs a modest increase in area.

ACKNOWLEDGMENT

The authors would like to thank the numerous referees involved in the review process; in particular, they deeply acknowledge the detailed comments and analysis that have led to the model introduced in this manuscript. Improvements in technical content and presentation would have not been possible without their dedication.

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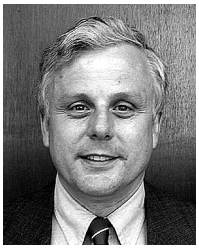

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