A Novel Dual-Slope Resistance-to-Digital Converter

N. Madhu Mohan, *Member, IEEE*, Boby George, and V. Jagadeesh Kumar, *Member, IEEE*

***Abstract*—A dual-slope resistance-to-digital (DSRDC) converter that accepts the resistance of a single-element resistive-type sensor as input and provides a direct digital output proportional to the parameter being sensed by the resistive-type sensor is presented in this paper. A high level of linearity and accuracy is achieved since the output of the DSRDC is dictated only by the magnitudes of a pair of dc reference voltages and the transformation constant of the sensor. Sensitivity analysis shows that the effect of circuit parameter variations on the output is minimal. Simulation studies and test results obtained on a prototype establish the efficacy of the proposed scheme.**

***Index Terms*—Analog-to-digital converter (ADC), dual-slope converter, resistance-to-digital converter (RDC), resistive-type sensor/transducer, single-element sensor.**

I. Introduction

RESISTIVE-TYPE sensors are widely used in the industry for the measurement of temperature, strain, pressure, and displacement. A resistive-type sensor can be of either single-element or differential type. A single-element resistive-type sensor, as the name indicates, is made of only one resistance whose value changes in proportion to the parameter being sensed. Examples are resistive temperature detectors (RTDs), strain gages, and peizoresistive-type sensors. The resistance of a typical linear single-element resistive-type sensor can be expressed as

$$R_x = R_o(1 + kx) \tag{1}$$

where R_x is the value of the sensor's resistance, k is the transformation constant of the sensor, and R_o is the nominal value of the sensor resistance when x, which is the parameter being sensed, is zero. To obtain a measurable voltage or current output from a passive sensor, such as the resistive type, an analog-signal-conditioning circuit is required [1].

Digital instrumentation systems are popular as they provide excellent processing power and user-friendly interfaces when compared with their analog counterparts. To interface a sensor having an analog voltage or current output to a digital instrumentation system, a suitable analog-to-digital converter (ADC) is required. A digital converter that directly accepts the element(s) of a sensor as input(s) and provides a digital output proportional to the physical quantity (measurand) being sensed by the sensor is known as a *direct digital converter*. Such a converter would be more compact and robust as the number of components and, hence, the complexity decreases, resulting in reduced errors and increased reliability. Some of the earlier attempts in this direction resulted in digital converters that are suitable for capacitance-type sensors [2]–[4]. Owen proposed a direct resistance-to-digital converter (RDC) suitable for a differential-type resistive sensor that requires four integration periods, i.e., T_A, T_B, T_C, and T_D [5]. (In his method, T_A and T_C are set, whereas T_B and T_D are measured.) In Owen's method, the final output is computed as $(T_B - T_D)/(T_B + T_D)$. Thus, the output is obtained by subtracting one measured time period from another. Hence, large systematic errors may result, particularly when the difference between the two periods is very small. Improved direct RDCs that avoid subtraction and obtain the final output with only three [6] and two integrations [7] were proposed earlier. All these converters are suitable only for a differential-type resistive sensor. A dual-slope method suitable for a single-element-type resistive sensor employing an up/down counter to implement subtraction has also been presented [8].

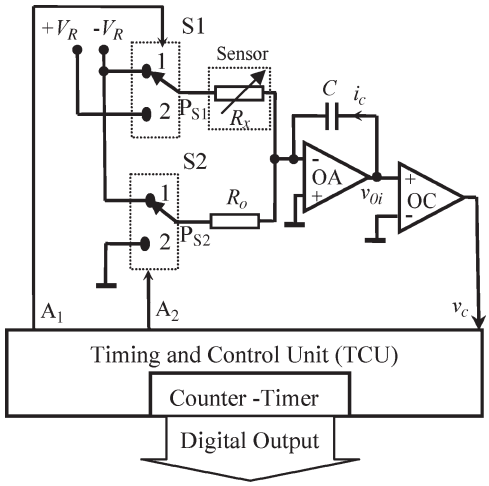

Fig. 1. Block schematic of the proposed DSRDC for a single-element resistive-type sensor.

In this paper, a novel dual-slope RDC (DSRDC) suitable for use with a single-element resistive-type sensor is presented. The proffered method uses only two periods of integration and completely avoids the subtraction of measured quantities.

II. Proposed DSRDC

A schematic of the proposed DSRDC is shown in Fig. 1. As in a conventional dual-slope ADC, the DSRDC consists of an

Manuscript received June 30, 2009; revised October 6, 2009. First published January 8, 2010; current version published April 7, 2010. The Associate Editor coordinating the review process for this paper was Dr. Wendy Van Moer.

N. M. Mohan and V. J. Kumar are with the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai 600036, India (e-mail: vjk@iitm.ac.in).

B. George is with the University of Graz, 8010 Graz, Austria.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIM.2009.2038030

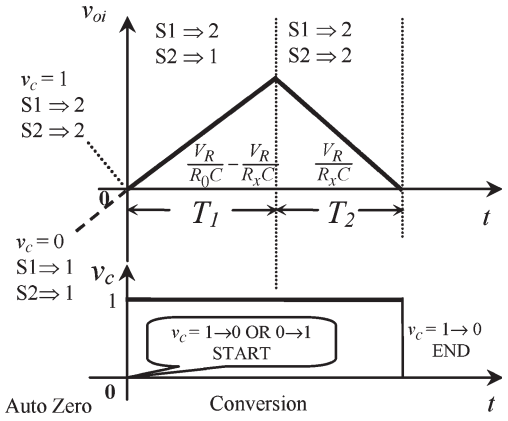

Fig. 2. Waveforms of the integrator output v_{oi} and comparator output v_c for a complete conversion (kx is positive).

integrator, a comparator, and a timing and control unit (TCU) comprising an n-bit or N-digit timer counter and control logic. The single resistance of the integrator in a conventional dual-slope ADC is replaced with two resistances in the proposed DSRDC, as shown in Fig. 1. The sensor resistance R_x becomes one of the resistances of the integrator, which is realized with opamp OA and feedback capacitance C. Thus, the sensor becomes part of the integrator in the DSRDC. The second resistor of the integrator is chosen to be a fixed resistance having a value equal to the nominal value R_o of the resistance of the sensor. One terminal of R_x and another of R_o are tied together, and the common terminal thus formed is connected to the inverting input of opamp OA. The free end of R_x is connected to the output P_{S1} of a single-pole double-throw (SPDT) switch S1. Similarly, the free end of R_o is tied to the output P_{S2} of another SPDT switch S2. Digital control lines A_1 and A_2 control switches S1 and S2, respectively. If A_1 is "1," position 1 is selected on switch S1, and $-V_R$ is applied to R_x. If A_1 is "0," then position 2 is selected, and $+V_R$ is applied to R_x. $-V_R$ is applied to R_o if A_2 is "1," and R_o is grounded if A_2 is "0." The voltages $+V_R$ and $-V_R$ are stable dc reference voltages that are equal in magnitude V_R but of opposite polarities.

The output of the integrator v_{oi} is fed to a comparator OC, which functions as a zero-crossing detector. If the output of the integrator is positive ($v_{oi} \geq 0$), then the comparator output v_c would be "1" (high); else, v_c will be "0" (low). The output of the comparator v_c is fed as input to the TCU. The TCU logic senses v_c and sequences two integrations by suitably controlling switches S1 and S2 through control lines A_1 and A_2. As in a typical dual-slope ADC, here, a conversion is preceded by an "auto-zero phase" as well.

A. Auto-Zero Phase

In the auto-zero phase, the TCU senses the comparator output v_c. If v_c is high, then the feedback capacitor C possesses a charge with a positive polarity on its terminal connected to the output of OA. For this condition, the TCU sets both S1 and S2 in position 2 ($A_1 = A_2 = 0$), connecting $+V_R$ to R_x and grounding R_o. The resulting capacitor current $i_C = -V_R/R_x$ discharges the feedback capacitor and the integrator output ramps down to zero, as shown by the dotted line in Fig. 2. On the other hand, if v_c is initially low, the feedback capacitor possesses a charge with a negative polarity on its terminal connected to the output of OA. For this condition, the TCU sets both S1 and S2 in position 1, connecting $-V_R$ to both R_x and R_o. The resulting capacitor current $i_C = ((V_R/R_o) + (V_R/R_x))$ discharges C, and the integrator output v_{oi} ramps up toward zero (as shown by the dashed lines in Fig. 2). In either case, the integrator becoming zero is indicated to the TCU by a transition (high to low in the former case and low to high in the latter) on v_c, which marks the end of the auto-zero phase. The flowchart of the logic of the auto-zero phase is given in Fig. 3. At the end of the auto-zero phase, a conversion phase is initiated.

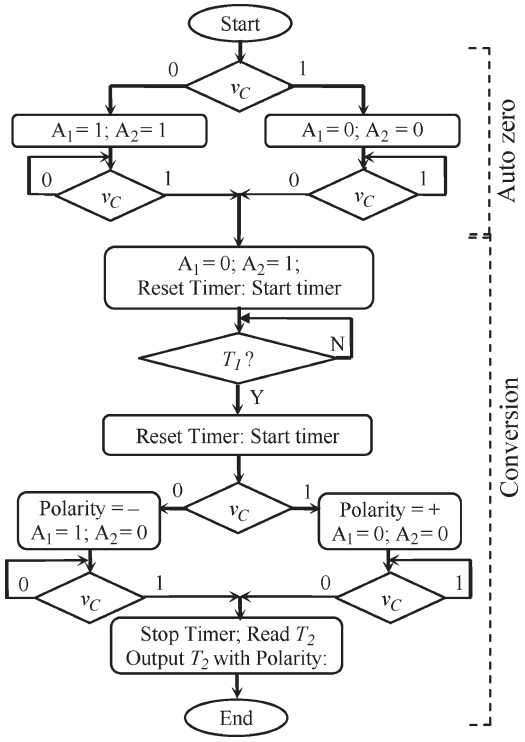

Fig. 3. Flowchart showing the auto-zero and conversion logic of the DSRDC for a single-element resistive-type sensor.

B. Conversion Phase

The conversion phase consists of two integration periods. The first integration period T_1 is a preselected set value, and the second integration period T_2 is measured and taken as the output. The conversion phase (measurement cycle) is started by setting switch S1 in position 2 and S2 in position 1, thus connecting $+V_R$ to R_x and $-V_R$ to R_o. Simultaneously, the TCU starts an internal timer to realize the first integration period T_1. The resulting capacitor current $i_C = ((V_R/R_o) - (V_R/R_x))$ is injected into the feedback capacitor C by the opamp OA.

If kx is positive, then i_C will be positive, and C would be charged with a positive polarity on its terminal that is connected to the output of the opamp OA. The opamp output will therefore ramp up with a positive slope $((V_R/R_oC) - (V_R/R_xC))$, as

shown in Fig. 2. Hence, at the end of T_1, the integrator output will be positive, and the output of the comparator v_c will be "1." At the end of T_1, the TCU restarts the internal timer to measure the elapsed time period T_2. Since v_c is high, the polarity of kx is taken as positive, and the TCU sets both S1 and S2 in position 2 (connecting $+V_R$ to R_x and grounding R_o). As a result, the charging current $i_C = -V_R/R_x$ flows into C and causes the integrator output to ramp down with a slope $V_R/(R_xC)$, which reaches zero, as shown in Fig. 2.

If kx is negative, then, during T_1, the integrator output ramps down. At the end of T_1, the TCU senses v_c to be "0" and hence 1) sets the polarity to be negative and 2) sets switch S1 to position 1 and S2 to position 2. Under this condition, the capacitor current $i_C = V_R/R_x$ forces the output of the integrator to ramp up and reach zero. The voltage waveforms in this case would be similar to Fig. 2 but inverted.

As soon as v_{oi} reaches zero, which is indicated to the TCU by a transition in v_c, the TCU stops the counter timer and reads the time taken for the output of the integrator to reach zero (T_2) and outputs T_2, along with the polarity. The logic for the auto-zero and conversion phases is shown in Fig. 3. Since the charge acquired by the capacitor C over the conversion cycle $(T_1 + T_2)$ is zero, we get

$$\left(\frac{V_R}{R_oC} - \frac{V_R}{R_xC}\right) T_1 = \left(\frac{V_R}{R_xC}\right) T_2. \tag{2}$$

Rearrangement of (2) results in

$$\frac{R_x - R_o}{R_o} = \frac{T_2}{T_1}. \tag{3}$$

Substituting the expression for R_x, as given by (1) in (3), we get

$$kx = \frac{1}{T_1} T_2. \tag{4}$$

Since T_1 is a preset constant and k, which is the transformation factor of the sensor, is also a constant, the measured time T_2 directly indicates x, which is the measurand.

The derivation of (4) assumed ideal conditions and components. Deviations from ideal conditions and nonidealities of components in a practical implementation of the proposed scheme will introduce errors in the output. These errors are analyzed next, and the results of simulations and experimentation conducted to validate the practicality of the proposed scheme are given in the sequel.

III. Analysis of the DSRDC

A. Effect Due to the 'ON' Resistances of the Switches on the Output

In deriving (3), it was assumed that the switches employed in the DSRDC were ideal, possessing zero 'ON' resistances. In reality, practical switches possess finite 'ON' resistances, which would appear in series with the resistances R_x and R_o. Hence, for a practical case, (3) gets modified as $((R_x + r_1) - (R_o + r_2)/(R_o + r_2)) = (T_2/T_1)$, where r_1 and r_2 are the 'ON' resistances of switches S1 and S2, respectively. On simplification, we get

$$kx = \frac{1}{T_1}\left(1 + \frac{r_2}{R_o}\right) \quad T_2 + \frac{(r_2 - r_1)}{R_o}. \tag{5}$$

A comparison of (5) and (4) shows that the 'ON' resistances of the switches introduce a gain error and an offset in the output. The gain error due to the 'ON' resistances of the switches can be kept insignificant if the ratio r_2/R_o is chosen to be very small, which is a condition easily met with most modern-day switches, possessing 'ON' resistances of as low as 1.25 Ω [9]. Employing two identical switches $(r_1 = r_2)$, the offset can be eliminated. The effect of the 'ON' resistances of the switches can also be eliminated by using unity gain buffers at the outputs P_{S1} and P_{S2} of the switches S1 and S2.

B. Effect of Deviation of the Fixed Resistance From Its Expected Value R_o

Equation (3) is based on the assumption that the fixed resistance has a value that is exactly equal to the nominal value R_o of the sensor. In practice, the value of the fixed resistance may deviate from the expected value, and (3) becomes

$$\left(\frac{R_x - R'_o}{R'_o}\right) = \frac{T_2}{T_1} \tag{6}$$

where R'_0 is the value of the fixed resistance. If the ratio R_o/R'_o is taken as α, (6) simplifies to

$$kx = \frac{1}{T_1} T_2 \left(\frac{1}{\alpha}\right) + \left(\frac{1}{\alpha} - 1\right). \tag{7}$$

A comparison of (7) and (4) indicates that the deviation in the value of the fixed resistance from the expected nominal value of the sensor resistance also introduces a gain error and an offset.

C. Effect of Reference Voltage Mismatch and OPAMP Offset Voltage

Equation (2) assumes that the reference voltages $-V_R$ and $+V_R$ are of equal magnitude. Practically, $-V_R$ is obtained by inverting the positive reference voltage. Hence, the degree of match of the magnitudes of the two voltages depends on the precision with which the inversion is performed. Any offset voltage in the integrator opamp, if present, also manifests as a mismatch between the reference voltages. Whatever the reason for the mismatch, (2) will have to suitably be modified. If the ratio $(|-V_R|/|+V_R|$ is taken as β, then, for positive kx, (2) becomes

$$\left(\frac{\beta V_R}{R_oC} - \frac{V_R}{R_xC}\right) T_1 = \left(\frac{V_R}{R_xC}\right) T_2.$$

On simplification, we get

$$kx = \frac{1}{T_1} T_2 \left(\frac{1}{\beta}\right) + \left(\frac{1}{\beta} - 1\right). \tag{8}$$

On the other hand, for negative kx, $((\beta V_R/R_oC) - (V_R/R_xC))T_1 = (\beta V_R/R_xC)T_2$, resulting in

$$kx = \frac{1}{T_1}T_2 + \left(\frac{1}{\beta} - 1\right). \quad (9)$$

A comparison of (8), (9) and (4) implies that, if the measurand is positive, the mismatch in the two reference voltages introduces a gain error and an offset, whereas it causes only an offset if the measurand has a negative polarity.

It is seen that all the nonidealities, i.e., the 'ON' resistances of switches, mismatch between the fixed resistance and the nominal resistance values, mismatch in the reference voltage magnitudes, and opamp offset voltage, introduce a gain error and an offset. The gain error and the offset can easily be compensated by gain correction and offset nulling.

D. Errors Due to the Delays Caused by the Comparator, Control Circuit, and the Switches

While discussing the operation of the proposed DSRDC, it was assumed that the circuit was ideal in that the comparator perfectly detected the zero crossing of the output of the integrator and that it also instantaneously indicated the zero crossing to the TCU. In practice, the comparator will possess an offset and a delay. The offset will result in detecting the "zero" at the offset voltage, instead of at the actual zero. It is easily seen that the presence of offset in the comparator shifts the baseline of comparison shown in Fig. 2 up or down, depending on the polarity, by an amount equal to the magnitude of the offset voltage. As long as the offset is constant within one conversion cycle (the offset drift is zero), this shift in baseline does not alter T_1 or T_2. Hence, the offset of the comparator does not affect the functioning of the DSRDC. The comparator delay is normally small (200 ns for the LM311 used in the prototype), compared with the period of the clock of the TCU. Hence, the delay of the comparator has negligible effect on the performance of the DSRDC. Although the delay introduced by the switches is a few hundred nanoseconds, it is very small, compared with T_1 and T_2 (in milliseconds), and hence does not significantly affect the performance of the DSRDC.

The uncertainties arising out of clock jitter, integrator nonlinearity, and switching and circuit noise, which are applicable to a dual-slope-type ADC, are well documented [12]. All these uncertainties are applicable to the proposed DSRDC as well.

IV. Simulation Studies

To test the efficacy of the proposed method, the DSRDC was simulated using OrCAD-PSpice (version 16.2) from M/s Cadence Corporation. Since the PSpice model of the CD4052 proposed to be used for the switches was not available, it was decided to simulate the DSRDC using the ADG508 octal switch from Analog Devices. The OP07 was used as the opamp, and the LM311 was used as the comparator. The TCU was implemented using simple logic gates and an NE555 timer.

Simulations were carried out for RTD types of sensors. A typical RTD sensor with a nominal value of 10 000 Ω (Pt10 000) was chosen as the sensor, and the circuit operation was simulated. The time taken for the integrator output voltage to return to zero T_2 was measured for each run of the simulation. The measured T_2 was then used to calculate the temperature employing the coefficients provided by M/s Heraeus Sensor-Technology, Kleinostheim, Germany, which is a manufacturer of the sensor used in prototyping the circuit. Various likely sources of error, such as the comparator and switch delay, opamp and comparator offset voltage, 'ON' resistance of the switches, and change in the nominal value of the fixed resistance, were incorporated into the model of the circuit utilized for simulation to determine the worst case performance. The simulation was run for temperature ranging from -50 °C to 150 °C, in steps of 10 °C, the results of which are shown in Fig. 4. The errors in the output were found to be less than $\pm 0.03\%$, and the output was highly linear.

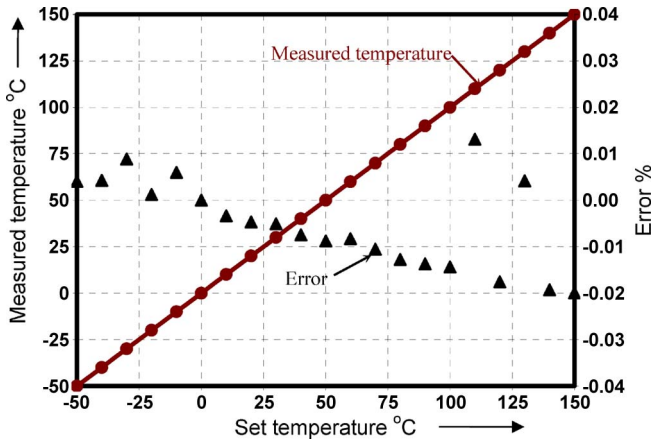

Fig. 4. Performance of the DSRDC obtained through simulation in the temperature range of -50°C–150 °C.

The magnitudes of the reference voltages were then altered to have a difference of 1%, and the simulation was run again. There was deterioration in the circuit performance as expected, and the full-scale error went up, by an order of magnitude, to $\pm 0.35\%$. In fact, it was found from the simulation study that the mismatch in the magnitudes of the positive and negative reference voltages was the major and only significant source of error in the circuit.

V. Experimental Setup

The circuit depicted in Fig. 1 and the control logic illustrated by the flowchart of Fig. 3 were implemented and tested. The OP97 was the opamp of choice for the integrator, whereas the LM311 was employed for use as the comparator. The comparatively high input offset voltage of the LM311 (30 mV maximum) was moderated by making use of the fact that it is the transition of the integrator output that is of significance rather than the magnitude of the voltages themselves. Therefore, the output of the integrator was amplified by a factor of 100 before being used with the comparator, due to which the comparator could detect the zero crossing of the integrator output voltage within ± 300 μV. The positive reference voltage $+V_R$ was obtained using an LM385-1.2 voltage reference diode. The negative reference voltage $-V_R$ was derived from $+V_R$ using an opamp inverter realized with an OP97. The magnitudes

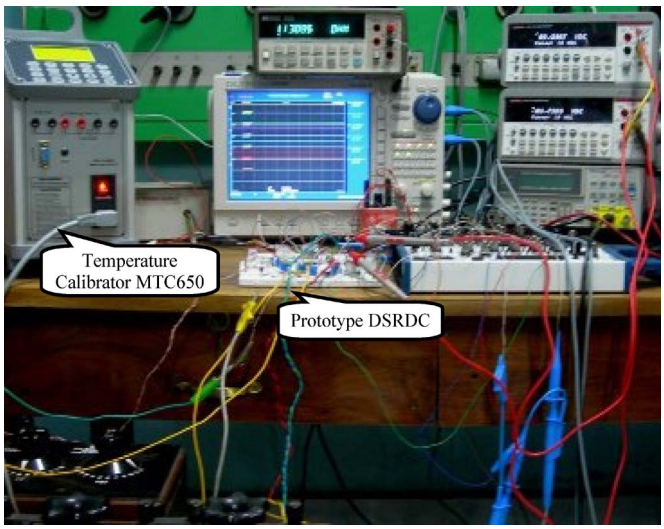

Fig. 5. Experimental setup for the DSRDC.

of the reference voltages were continuously monitored using two 6 1/2-digit multimeters from M/s Keithley (Model 2100) and were matched to ± 10 μV by making use of precision variable resistances from Otto Wolff, Berlin, Germany. The HCF4052 containing dual quad-channel switches was used for switching appropriate reference voltages to the sensor R_x and the fixed value resistor R_o. The entire circuit was powered by a $\pm$5-V/1.5-A dc/dc converter (AEE01AA18-L) from M/s Astec Power, CA, USA. The sensor R_x used was a Pt 10 000 RTD sensor from M/s Heraeus Sensor-Technology. It was first calibrated using the MP40R and MTC650 temperature calibrators from M/s Nagman Instruments, Chennai, India, for the range of 0 °C–600 °C, in steps of 10 °C. The resistance of the RTD at the various temperatures was carefully measured using the 34401A 6 1/2-digit multimeter from Hewlett-Packard.

The control and timing logic was implemented on a virtual instrument platform to bring in flexibility, modularity, and easy scalability. The NI USB-6251 universal series bus (USB)-based hardware from M/s National Instruments [10] formed the core of the control and logic unit, with the control logic being implemented in LabVIEW. The digital input and output lines and the two 32-bit general-purpose counter timers of the USB-6251 formed the heart of the control and logic system. The NI USB-6251 was interfaced to the switches and the comparator through the BNC-2120 termination board. Two of the digital output lines of the USB-6251 served as the control lines A_1 and A_2 for the HCF4052. The comparator output was made transistor–transistor-logic compatible and tied to a digital input line of the NI USB-6251. Fig. 5 shows the entire experimental setup.

The auto-zero and conversion logic was realized by a suitable program written in LabVIEW. The program makes use of one of the counters in the USB-6251 to generate a precise pulse train of the required frequency $1/T_1$. This frequency can be controlled from the software, and hence, T_1 can be modified to suit different combinations of R_o and C. At the beginning of T_1, the digital lines controlling the switch cause the resistive sensor R_x and the standard resistance R_o to be switched to the respective reference voltages. The rising edge of the counter output of the

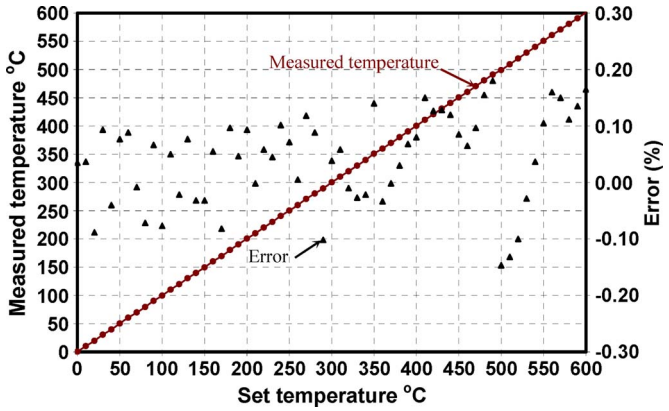

Fig. 6. Output and error from the prototype DSRDC.

USB-6251 at the end of T_1 switches the sensor resistance R_x to the positive reference voltage while the fixed resistance R_o is grounded. The instant the integrator output voltage reaches zero, the output of the comparator toggles, indicating the end of T_2 and, thereby, the end of the measurement cycle. The start of T_2 (end of T_1) and the change in the comparator output at the end of T_2 serve as markers for another USB-6251 counter and hence is made to accurately measure the time period T_2.

The value to be selected for the first integration time T_1 is dictated by two conflicting criteria, i.e., conversion speed (samples per second) and resolution (coupled with noise immunity). While T_1 should be as small as possible for obtaining the maximum rate of conversion, it should be as large as possible for realizing the maximum resolution (and, hence, optimal noise immunity). In the experimental setup, T_1 was set at 100 ms (to cancel out 50-Hz interference), and measurements were made over the range of temperature of 0 °C–600 °C. Over the temperature range of interest, T_2 was found to vary between 150 μs and 231 ms. It has to be mentioned here that a value of 2 s provided greater resolution and accuracy in the measurement of T_2 at the lower end of the temperature scale.

Each measurement was repeated 25 times to average out any random errors, and the resulting value of T_2 was used to calculate the deviation kx. The calculated value of kx was utilized to determine the temperature in accordance with the IEC60751 Standard [11] and the associated coefficients for a Platinum RTD (Pt 10 000). The measured temperature is plotted against the set temperature on the calibrator for the range of 0 °C–600 °C in Fig. 6, along with the corresponding errors for the different measurements. As can be seen, the prototype exhibits excellent linearity over the entire range of measurement, with a maximum error of less than $\pm 0.2\%$.

VI. Conclusion

A novel direct digital converter for obtaining a digital output directly from a single-element-type resistive sensor and incorporating the dual-slope topology has been presented in this paper. The RDC presented in this paper has all the advantages of the dual-slope technique (such as good resolution, accuracy, and tolerance to component variations) and the attendant limitation of the technique, i.e., low conversion speed. A conversion speed of a few conversions to a few hundred conversions per

second is achievable. This speed is quite adequate for most applications involving resistive-type sensors. Analysis of the proposed method for possible sources of errors indicates that most of the nonidealities introduce a gain error and an offset, which can easily be canceled by employing gain correction and offset compensation. The results obtained on the prototype presented here establish the efficacy of the proposed method and justify the inferences drawn through analysis.

REFERENCES

[1] E. O. Doebelin, *Measurement Systems—Application and Design,* 5th ed. New York: McGraw-Hill, 2004.

[2] B. Wang, T. Kajita, T. Sun, and G. C. Temes, "High-accuracy circuits for on-chip capacitive ratio testing and sensor readout," *IEEE Trans. Instrum. Meas.*, vol. 47, no. 1, pp. 16–20, Feb. 1998.

[3] B. George and V. J. Kumar, "Switched capacitor triple slope capacitance to digital converter," *Proc. Inst. Elect. Eng.—Circuits, Devices Syst.*, vol. 153, no. 2, pp. 148–152, Apr. 2006.

[4] B. George and V. J. Kumar, "Novel switched-capacitor dual slope capacitance to digital converter for differential capacitive sensors," in *Proc. IEEE I2MTC*, Singapore, 2009, pp. 1–4.

[5] E. W. Owen, "An integrating analog to digital converter for differential transducers," *IEEE Trans. Instrum. Meas.*, vol. IM-28, no. 3, pp. 216–220, Sep. 1979.

[6] V. J. Kumar, N. M. Mohan, and V. G. K. Murti, "Digital converter for push–pull type resistive transducers," in *Proc. IEEE IMTC*, Ottawa, ON, Canada, 2005, pp. 422–425.

[7] N. M. Mohan, V. J. Kumar, and B. George, "Dual-slope resistance-to-digital converter," in *Proc. IEEE IMTC*, Warsaw, Poland, 2007, pp. 1–5.

[8] N. M. Mohan and V. J. Kumar, "Direct digital converter for a single, active element resistive sensor," in *Proc. IEEE I2MTC*, Singapore, 2009, pp. 828–831.

[9] "Data Sheet—MAX4680," 1.25 Ohm, Dual SPST, CMOS Analog Switches, Maxim Corp. [Online]. Available: http://datasheets.maxim-ic.com/en/ds/MAX4680-MAX4700.pdf

[10] "USB-6251—User Manual," 16-Bit, 8-Channel, 1.25MSa/s Data Acquisition Device: National Instruments. [Online]. Available: http://www.ni.com/pdf/manuals/371291g.pdf

[11] *Industrial Platinum Resistance Thermometers and Platinum Temperature Sensors*, IEC60751 Standard, 2008.

[12] E. R. Hnatek, *A User's Handbook of D/A and A/D Converters*. Melbourne, FL: Krieger, 1988.

N. Madhu Mohan (S'99–M'10) was born in Coimbatore, India, on March 21, 1970. He received the Bachelor's degree in electronics and communication engineering from the University of Calicut, Kerala, India, in 1991 and M.S. degree (by research), in 2003, from Indian Institute of Technology Madras, Chennai, India, where he is currently working toward the Ph.D.degree in bio-medical instrumentation with the Measurements and Instrumentation Laboratory, Department of Electrical Engineering.

His research interests are measurements, bio-medical instrumentation, and virtual instrumentation.

Boby George was born in Kannur, Kerala, India, on April 30, 1977. He received the Bachelor's degree from the Institution of Engineers, Kolkatta, India, in 2001 and the M.Tech and Ph.D. degrees from Indian Institute of Technology Madras, Chennai, India, in 2003 and 2007, respectively, all in electrical engineering.

He is currently a Postdoctoral Fellow with the University of Graz, Graz, Austria. His research interests are measurements, instrumentation. and virtual instrumentation.

V. Jagadeesh Kumar (M'96) was born in Madras, India, on July 21, 1956. He received the B.E. degree in electronics and telecommunication engineering from the University of Madras, Madras, India, in 1978 and the M.Tech. and Ph.D. degrees in electrical engineering from Indian Institute of Technology Madras (IIT Madras), Chennai, India, in 1980 and 1986, respectively.

He is currently the Head of the Department of Electrical Engineering, IIT Madras. He was a BOYSCAST Fellow with King's College, London, U.K., during 1987–1988, and a DAAD Fellow with the Technical University of Braunschweig, Braunschweig, Germany, during 1997. He was a Visiting Scientist with the Technical University of Aachen, Aachen, Germany, during 1999. He taught for a term at the Asian Institute of Technology, Bangkok, Thailand, in the summer of 1999. He has published more than 40 papers in international journals and presented more than 60 papers at various conferences. He is the holder of six patents. His teaching and research interests are measurements, instrumentation, and signal processing.