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Procedia Environmental Sciences 11 (2011) 339 – 345

Procedia Environmental Sciences

Adiabatic Two-Phase CPAL Flip-Flops Operating on Near-Threshold and Super-Threshold Regions

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Abstract

Low-power adiabatic flip-flops operating on near-threshold and super-threshold regions are investigated in this paper. The flip-flops are realized using two-phase CPAL (complementary pass-transistor adiabatic logic) circuits. A traffic light controller operating on near-threshold and super- threshold regions is verified. All circuits are simulated using NCSU PDK 45nm technology by varying supply voltage from 0.4V to 0.9V with 0.1V steps. Based on the HSPICE simulation results, the energy consumption of the medium-voltage adiabatic flip-flops using two-phase CPAL circuits can be greatly reduced with reasonable speed.

*Keywords:*Flip-flop; Near-threshold; Medium-voltage circuits; Adiabatic circuits

1. Introduction

As the density and size of the VLSI chips continue to increase, the power consumption has become a critical concern. CMOS circuits using the nominal source voltage can reach high operation frequencies with large energy consumptions. The energy consumption in VLSI circuits has two components: dynamic energy and leakage energy. Dynamic energy includes two components: switching energy due to charging and discharging of load capacitances, and short energy due to a direct-path from supply voltage to the ground. The short energy represents a small percentage in the total energy consumption, thus it can be ignored. Static energy dissipation is caused by leakage currents of MOS devices. The total energy consumption (E_{total}) per cycle are expressed as [1]

$$E_{total} = E_{dyn} + E_{leakage} = C_L V_{DD}^{\ 2} + V_{DD} I_{leakage} T \quad (1)$$

where C_L is the load capacitance, V_{DD} is source voltage, T is operation cycle, and $I_{leakage}$ is leakage current. As supply voltage scales down, dynamic energy scales quadratically, while leakage energy is reduced linearly. Therefore, a direct solution for reducing energy consumption is to scale down supply voltage [2].

Scaling supply voltage to sub-threshold region can reach minimum energy consumption but only suits for ultra low power design (f=10KHz to 5MHz) [3]. In order to attain more extensive application, scaling supply voltage to medium-voltage region is an attractive approach especially suiting for mid performances (f=5MHz to 100MHz) [3]. Low supply voltage near the threshold voltage is called near threshold circuits [4]. For many applications, the performance penalty of the near-threshold logic circuits can be tolerable [4].

Adiabatic logic utilizes AC power-clock to recover effectively the charge delivered, resulting in lower dynamic power, thus the energy consumption is much smaller than that of the conventional CMOS [5, 6]. The previously proposed adiabatic logic families focus mainly on nominal voltage circuits. Presently, several investigations for adiabatic circuits such as PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) and CAL (clocked adiabatic logic) operating on medium-voltage region have been reported in [7, 8]. The results shown that adiabatic circuits that operating on medium-voltage region can greatly reduce energy consumptions with reasonable speed.

doi:10.1016/j.proenv.2011.12.054

This paper proposes adiabatic flip-flops operating on near-threshold and super-threshold regions, which are realized using two-phase CPAL (complementary pass-transistor adiabatic logic) circuits. A traffic light controller using two-phase CPAL is demonstrated at 45nm CMOS process. All circuits are simulated using HSPICE. Simulation results show that the energy consumption of the medium-voltage traffic light controller using two-phase CPAL circuits can be greatly reduced with reasonable speed.

2. Review of Two Phase CPAL Flip-Flops

Two-phase CPAL circuits have been reported in [6], as shown in Fig. 1. It is mainly composed of two parts: logic function circuit that consists of four NMOS transistors (N5-N8) with complementary pass-transistor logic (CPL) function block, and the load drive circuit that consists of a pair of transmission gates (N1, P1 and N2, P2). The clamp transistors (N3 and N4) ensure stable operation by preventing from floating of output nodes. Its simulated waveforms and two-phase power clocks are also shown in Fig. 1.

The CPAL gates, such as two-input AND/NAND gate, OR/NOR gate, XOR/XNOR gate, and multiplexer can be realized by using CPL function blocks to replace the transistors (N5-N8) of the CPAL buffer, as shown in Fig. 2 [4, 5]. The two-phase CPAL D and *T* flip-flop with the pre-settable line (*Reset*) is shown in Fig. 3.

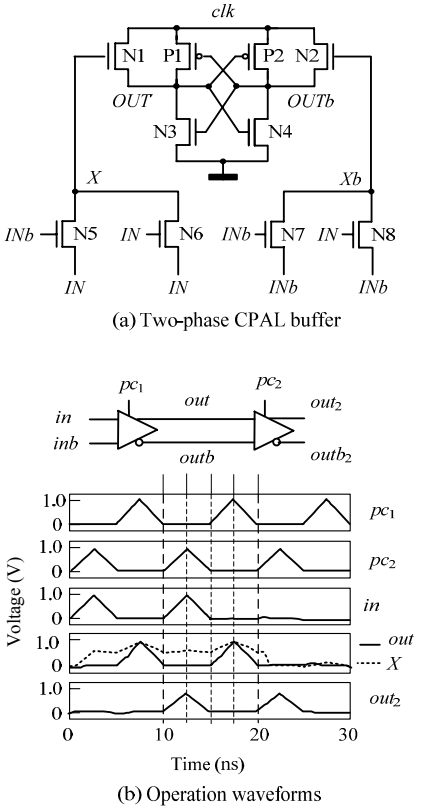

Figure 1. CPAL buffer using two-phase power clocks.

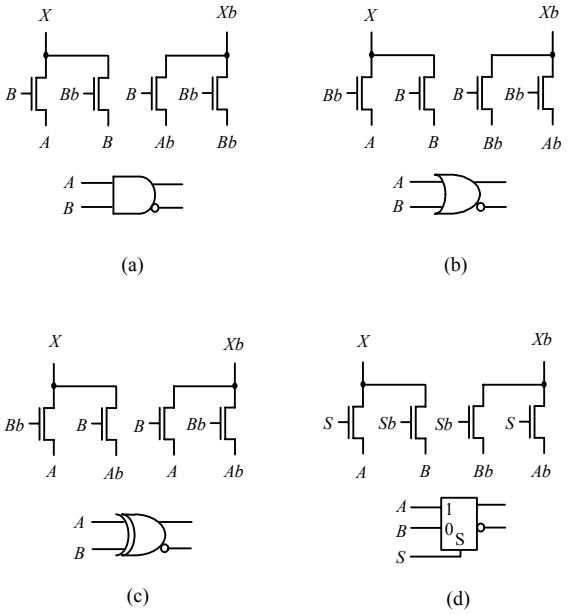

Figure 2. Two-phase CPAL gates. (a) AND/NAND, (b) OR/NOR, (c) XOR/XNOR, and (d) multiplexer.

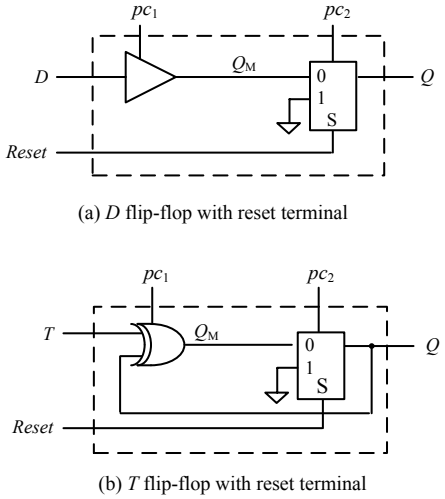

Figure 3. Adiabatic flip-flops with reset terminal based on two-phase CPAL.

3. Voltage Scaling for Two-Phase CPAL Circuits

The total energy dissipation per cycle of the CPAL buffer operating in near-threshold and super-threshold regions can be expressed as

$$E_{total} = 8\frac{RC_L}{T}C_L V_{DD}^2 + a\frac{1}{2}C_{boot}(V_{DD} - V_{TN})^2 + \frac{1}{4}V_{DD}I_{Leak}T, \quad (2)$$

where R is turn-on resistance of the transmission gates (P1 and N1 or P2, and N2) that is approximately inversely proportional to the source voltage (V_{DD}), C_L is load capacitances of the CPAL buffer, V_{DD} is peak-peak voltage of power clocks, T is period of the power-clock, a is signal active ratio, C_{boot} is the capacitance of the bootstrapping node X or Xb, V_{TN} is threshold voltage of NMOS transistors, and I_{Leak} is average leakage current of the CPAL buffer, respectively.

In (2), the first and second terms are adiabatic and non-adiabatic energy dissipations that scale down quadratically with the supply voltage for a given frequency, and the third term is leakage energy dissipation caused by leakage current (I_{Leak}).

In current CMOS technologies, the total leakage current of MOS transistors is mostly composed of the sub-threshold leakage, which is independent of the power source for near-threshold and super-threshold regions [2]. Therefore, the leakage dissipation of the two-phase CPAL circuits is approximately proportional to source voltage for a given frequency. From (2), the total energy consumption of the CPAL circuits would be cut down quadratically with the supply voltage for a given frequency.

In order to investigate the performances of the CPAL circuits in near-threshold and super-threshold regions, the CPAL buffer chain is simulated by varying the source voltage (V_{DD}) from 0.2V to 1.0V with 0.1V step using PTM (Predictive Technology Model) 45nm process [9]. The energy dissipations of the CPAL buffer in different supply voltages are shown in Fig. 4 at 1MHz. As shown in Fig. 4, for a given frequency, the total energy loss is quadratically reduced approximately as supply voltage scales down.

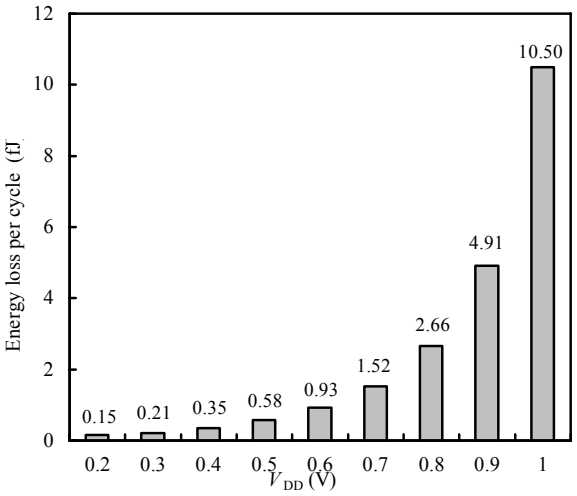

Figure 4. Energy dissipations of the CPAL buffer chain in different voltages at 5MHz.

4. Two-Phase CPAL Sequential Circuits

Taken as an example, a traffic light controller has been verified using two-phase CPAL circuits operating on near-threshold and super-threshold regions, as shown in Fig. 5. The entire circuit is cascaded by four *T* flip-flops based on two-phase CPAL circuits. In order to facilitate proper function of the circuit, a reset line is added for the XOR gate by using a multiplexer. R_1 and R_2 generated from timing clear circuit shown in Fig. 5 are the reset signals of the traffic light controller.

The timing clear circuit consists of an irregular mode-three counter based on two-phase CPAL with power-gating scheme. When the Boolean signals of $Q_3 - Q_0$ are given '0001', the clock signal *pc* is set '1' and the mode-three counter works.

All circuits are simulated using HSPICE. The simulated waveforms of the traffic light controller using 45nm CMOS process is shown in Fig. 6.

The traffic light controller based on two-phase CPAL circuits has been simulated at different source voltage V_{DD}. At each supply voltage. The maximum operating frequency is obtained, where the traffic light controller has correct logic function. The maximum operating frequency at different source voltage is shown in Fig. 7.

The energy consumption per cycle of the traffic light controller at maximum operating frequency is shown in Fig. 8. Compared with the nominal supply voltage operation, the energy consumption of the traffic light controller saves about 65% at 0.7V supply voltage.

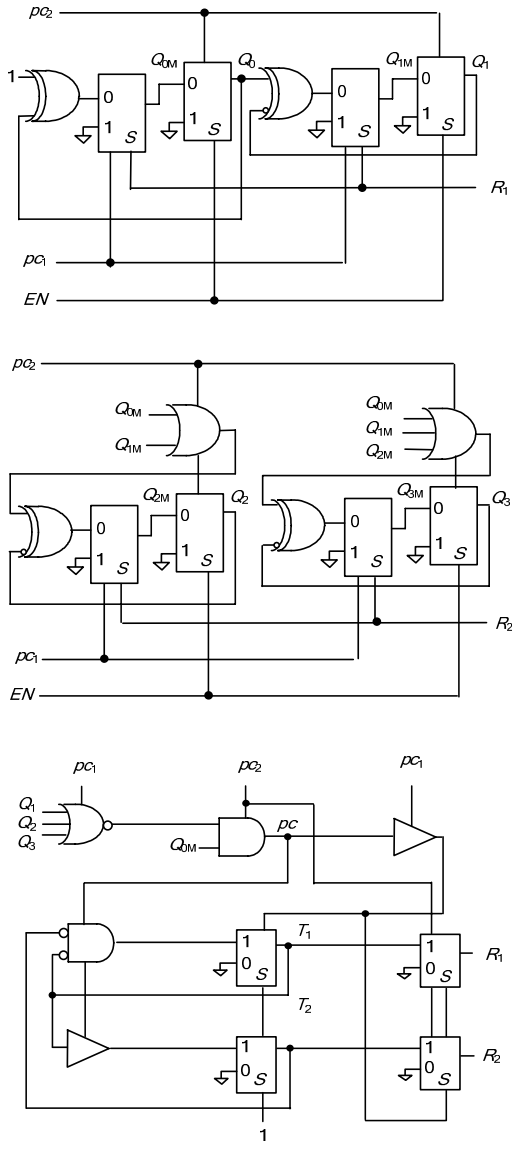

Figure 5. Traffic light controller based on two-phase CPAL circuits.

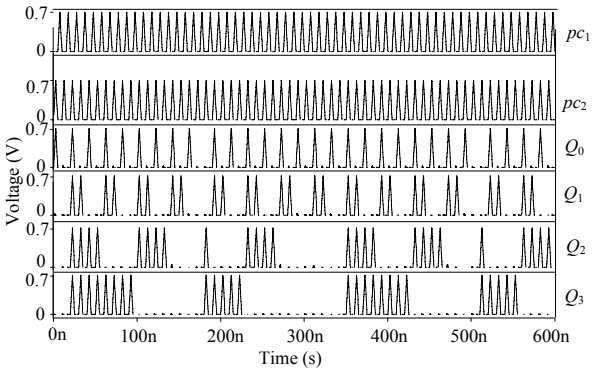

Figure 6. The simulated waveform of the traffic light controller operating on near-threshold region.

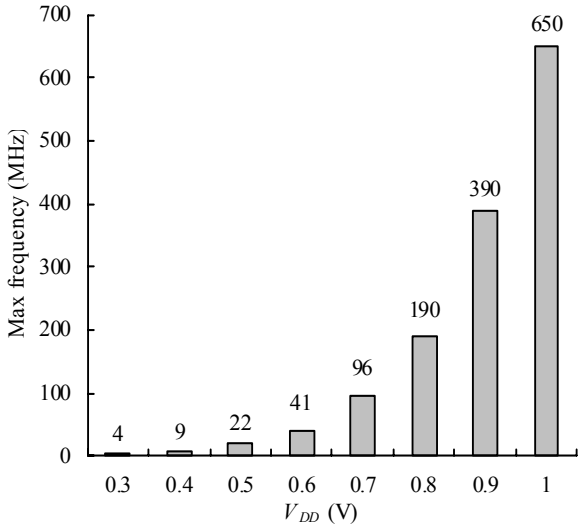

Figure 7. Max operating frequency of the traffic light controller in different voltages.

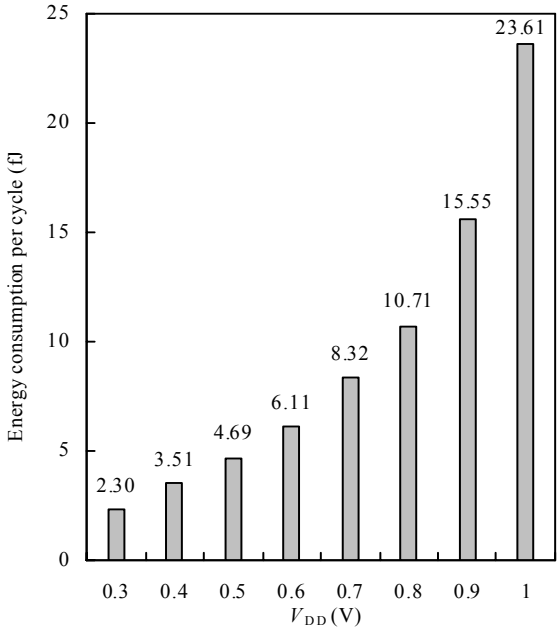

Figure 8. Energy consumption per cycle at max operating frequency for various supply voltage.

This example shows that the energy consumption of the medium-voltage traffic light controller using two-phase CPAL circuits can be greatly reduced with reasonable speed.

5. Conclusion

This paper focuses on the near-threshold and super-threshold adiabatic flip-flops and sequential circuits. The near-threshold adiabatic flip-flops are realized with two-phase CPAL (complementary pass-transistor adiabatic logic) circuits. A traffic light controller operating on near-threshold and super- threshold regions has been verified. All circuits are simulated using NCSU PDK 45nm technology by varying supply voltage from 0.3V to 1.0V with 0.1V steps. Based on the HSPICE simulation results, the energy consumption of the medium-voltage adiabatic flip-flops using two-phase CPAL circuits can be greatly reduced with reasonable speed.

6. Acknowledgment

Project is supported by National Natural Science Foundation of China (No. 61071049), Zhejiang Science and Technology Project of China (No. 2010C31116), Scientific Research Fund of Zhejiang Provincial Education Department (No. Z200908632), and Ningbo Natural Science Foundation (No. 2009A610066).

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