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High-speed low-power comparator for analog to digital converters

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ABSTRACT

A low-power high-speed two-stage dynamic comparator is presented. In this circuit, the voltage swing of the first stage of the comparator, *pre-amplifier stage*, is limited to *Vdd/2* in order to reduce the first stage power consumption. Also, this voltage swing limitation provides a strong drive at the evaluation phase for the second stage to enhance the comparison speed. Analytical derivations along with post layout simulation results prove that the proposed method speeds up the conventional circuit by a factor of two in the same budget of power consumption and offset voltage. Furthermore, the proposed circuit offers a wide input common mode range as large as the supply voltage while employing PMOS transistors at the input of the comparator.

1. Introduction

Low-power high-speed ADCs are natural candidates for portable electronic devices [1–19]. Comparators play an important role in efficiency of commonly used ADCs, such as Flash and SAR ADCs [5–8,16–19]. Static comparators have been used in the past, however, they are impractical for portable applications because of their limited speed and significant amounts of power consumption [1]. One-stage dynamic comparators were proposed to reduce the power consumption and improve the speed [2]. These comparators, however, suffer from an inherent trade-off between the power consumption and offset voltage [3]. Moreover, one-stage dynamic comparators suffer from kick-back noise caused through the capacitive path from the output nodes to the input nodes of the comparator [3]. Two-stage dynamic comparators were proposed to mitigate the kickback noise and decouple the offset versus speed trade-off of the single-stage dynamic comparators [4].

In the two-stage dynamic comparators, the input transistors are chosen large enough to achieve a given offset voltage. In fact, the overall offset of the comparator is almost dominated by the first stage [1]. Using large transistors at the input leads to large parasitic capacitors at the output of the first stage of the comparator. Consequently, there is an inherent trade-off between power consumption and offset voltage. Recently some methods are reported to enhance the speed and reduce power consumption, or offset voltage. These methods have their own advantages and disadvantages which are briefly described as follows.

In [5], a two stage comparator is presented working with only *one* clock phase to reduce the complexity and power consumption. In this comparator, a time domain bulk tuned offset cancelation is used to achieve a low offset voltage. With lower offset voltage smaller transistors can be employed resulting in a lower power consumption. However, this offset cancelation method limits the speed significantly. In [6], another structure for a two-stage comparator is presented which achieves a higher speed at the expense of higher power consumption. The circuit of [7] presents a high-speed input common mode voltage (V_{cm}) insensitive comparator. In this comparator, there is a capacitive path from the output to the input which leads to a large kickback noise. The comparator of [8] uses a delayed clock signal to reduce power consumption and enhance the speed. In this circuit, the delayed clock signal helps increasing the preamplifier gain and reducing the delay of the latch circuit, however, this circuit suffers from kickback noise. Since the latch and preamplifier stages are coupled together, this circuit is not a good choice for high precision applications. In fact, the large sizing of both preamplifier and latch stages (to achieve a low offset voltage) results in a higher power consumption.

In the proposed comparator, the voltage variation of the first stage is minimized to achieve a high-speed low-power comparator with an acceptable offset voltage. Moreover, the proposed circuit improves the input common mode range, as the latch stage is activated stronger than the conventional circuit. Analytical derivations are presented which verify the benefits of the proposed comparator and predict its delay precisely. Section 2 presents the circuit of the conventional and proposed comparator. In Section 3, analytical derivations are discussed. In Section 4, V_{cm} generation is discussed. Section 5 presents the schematic and post layout simulation results. Section 6 concludes the paper.

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2. Comparator circuits

2.1. Conventional two-stage dynamic comparator

The conventional two-stage dynamic comparator is shown in Fig. 1. This comparator is comprised of two stages: the *pre-amplifier stage* (first stage) and the *latch stage* (second stage). The operation of this circuit is briefly described as follows.

Before the comparison is made, the comparator state is reset (*clk* = "*1*", *clkn* = "*0*") to discharge the output nodes of the first stage to *Gnd* and charge the output nodes of the second stage to *Vdd*. In the next phase, the *evaluation phase*, "*clk*" and "*clkn*" goes to "*0*" and "*1*", respectively, to start the comparison. Then, the output voltages of the first stage (V_{O1+}, V_{O1-}) start to grow gradually. The growth rate depends on the magnitude of the input differential voltage ($V_{in+} - V_{in-}$). Gradually, a differential voltage appears at the output nodes of the first stage (*i.e.*, $V_{O1+} - V_{O1-}$). When the output voltages of the first stage approach the threshold voltage of an NMOS transistor (M10, M11), the second stage (latch) is activated. Hence, the positive feedback nature of the latch amplifies the differential voltage until the latch is locked. Consequently, the voltage of one of the output nodes of the latch stage settles at *Gnd* and the other one settles at *Vdd* while the output voltages of the first stage both reach *Vdd*.

For high resolution applications the size of the input transistors (M3, M4) are chosen large to achieve a low offset voltage. As discussed earlier, the output nodes of the first stage are discharged to the ground during the *reset phase* and charged toward *Vdd* during the *evaluation phase*. As a result, a low offset criterion demands for a large first stage transistor sizing, thus causes significant amounts of power consumption. This trade-off makes the conventional comparator an unsuitable choice for low-power high-resolution applications.

2.2. Proposed comparator

The proposed comparator is shown in Fig. 2. At the *reset phase*, the node voltages of the first stage are discharged to V_S (*Vdd/2*) which is large enough to keep the second stage active. In order to avoid a DC power consumption in the second stage, *M14* is placed to cut the path from *Vdd* to *Gnd* during the *reset phase*. A simple method of V_S generation is discussed in Section 4.

The voltage swing of the first stage of the comparator is limited to *Vdd/2*. As a result, the power consumption of the first stage which is the dominant part of total power consumption is reduced by a factor of *two* compared to the conventional comparator. The smaller gate-source voltage reduces the drive current of M1 and M2 and it does not reduce the speed; since it only affects the reset phase and has no effect during the evaluation phase. Moreover, due to the proposed method there is no delay time to charge the output voltages of the first stage to the level of an NMOS voltage threshold to activate the latch stage. The latch speed enhancement because of the large common mode voltage at the input of the latch (>VDD/2) enhances the speed considerably as discussed in Section 3. In fact, at the beginning of the *evaluation phase*, the output voltage of the first stage is large enough to strongly activate the second stage. This strong activation enhances the speed of the latch stage significantly. Totally, the pre-amplifier and the latch delay enhancement speeds up the comparator significantly compared to the conventional comparator.

The lower power consumption can address the offset concerns of the comparator. In order to keep the offset of the comparator under control, the size of the input transistors of the two stages (*i.e., M3, M4, M10* and *M11*) is designed carefully. Fortunately, since the proposed comparator improves the speed and reduces the power consumption, the size of these transistors can be designed large enough to reduce the overall input transferred offset voltage of the comparator.

3. Analytical derivations of speed

In this section, the high speed benefit of the proposed comparator is verified analytically. Then, a model is presented to calculate the delay. To predict the comparator delay precisely, the analytical formulas are derived for three different ranges of the input common-mode voltage of the comparator (input V_{cm}).

The delay of the comparator of Fig. 1 is comprised of two terms as the following equation.

$$T_{comp} = T_{pre-amp} + T_{latch} \tag{1}$$

$T_{pre-amp}$ which is the time required to charge the *O1+* and *O1−* parasitic capacitors to V_{thn} (voltage threshold of M10 and M11), is calculated as follows.

$$T_{pre-amp} = \frac{C_{O1+} + C_{O1-}}{I_{M5}} \times V_{thn} \tag{2}$$

Fig. 3(a) presents the schematic simulation results of $T_{pre-amp}$ for a typical conventional comparator. This delay goes ∞ as V_{cm} goes to *Vdd* because M3 and M4 work in the sub-threshold region, therefore, the drain current of *M5* approaches zero. In the proposed comparator $T_{pre-amp} = 0$, since at the beginning of the evaluation phase the output voltages of the pre-amplifier stage are larger than V_{thn} (*Vdd*/2).

There are some methods which provide an accurate model of the delay, such as the method proposed in [8–10]. Here, a simple,

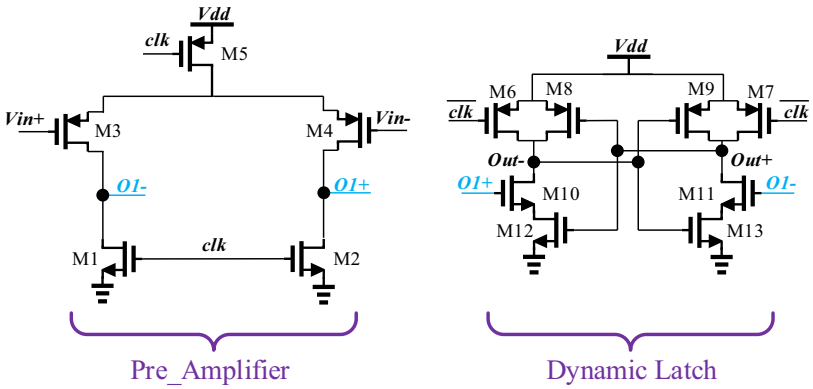

Fig. 1. Pre-amplifier and the latch stages of the conventional two-stage dynamic comparator.

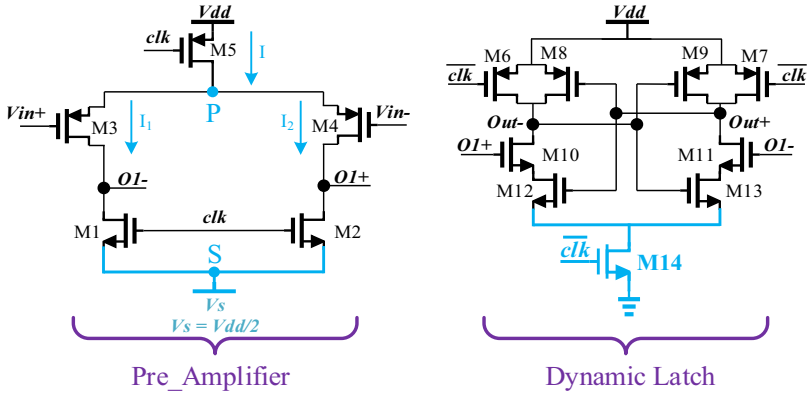

Fig. 2. Proposed two-stage dynamic comparator and its difference in comparison to the conventional comparator.

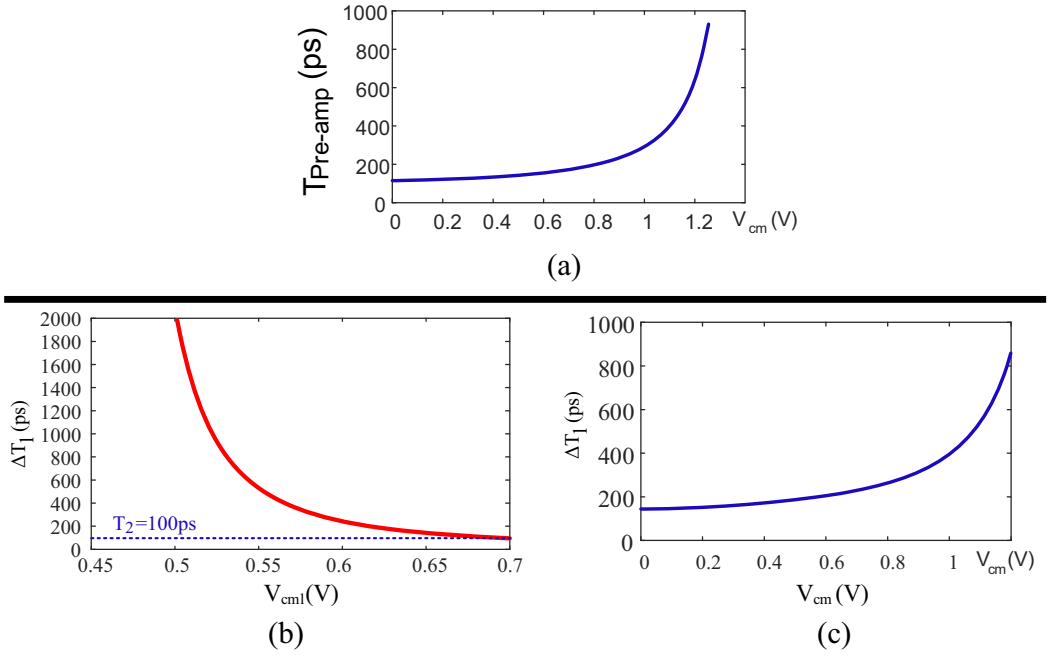

Fig. 3. (a) Simulation result of $T_{\text{pre-amp}}$, (b) simulation result of ΔT_1 versus input common mode voltage of the latch (V_{cm}), (c) simulation result of ΔT_1 versus input common mode voltage of the comparator (V_{cm}).

yet almost accurate model is considered then is modified to predict the delay more precisely. In fact, a straight-forward accurate model is derived to present closed form equations for the delay. Based on the analytical derivations reported in [10], the following equation presents an acceptable prediction of the delay of a back-to-back inverter latch.

$$T_{latch} = \tau \times \ln\left(\frac{0.5(VDD - GND)}{\Delta V_{in}}\right), \quad \tau = \frac{C_L}{G_{M_{PMOS}} + G_{M_{NMOS}}} \tag{3}$$

Based on the Appendix 1, we modify (3) as the following equation to predict the delay more precisely.

$$T_{latch} = T_1 + \tau \times \ln\left(\frac{0.5(VDD - GND)}{\Delta V_{in}}\right) \tag{4}$$

$$T_1 = \frac{C \times V_{thp}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{10,11}(V_{cml} - V_{thn})^2} \tag{5}$$

where V_{cml} represents the input common mode voltage of the latch stage, and V_{thn} and V_{thp} are the threshold voltage of NMOS and PMOS transistors, respectively. In the proposed circuit, V_{cml} is larger as large as $Vdd/2$ compared to the conventional circuit. To make a comparison between the proposed and conventional comparators about their first part of T_{latch} (T_1), ΔT_1 is defined and calculated as follows.

$$\Delta T_1 = T_{1_{conventional}} - T_{1_{proposed}} \tag{6}$$

$$\Delta T_1 = \frac{C \times V_{thp}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{10,11}}\left(\frac{1}{(V_{cml} - V_{thn})^2} - \frac{1}{(V_{cml} + Vdd/2 - V_{thn})^2}\right) \tag{7}$$

This equation leads to 250 ps for typical values of the circuit parameters in 0.18 um *CMOS* technology. Fig. 3(b) presents simulation result of ΔT_1 versus input common mode voltage of the latch stage (V_{cml}). This figure reveals two instructive points of view.

Firstly, even for large values of V_{cml} there is a considerable difference of 100 ps between the delay of the proposed and the conventional comparators. In fact, the stronger drive of the proposed circuit results in a speed privilege compared to the conventional comparator. Secondly, for low values of V_{cml} close to V_{thn} the difference goes to ∞, since NMOS input transistors of the latch stage goes to sub-threshold region. This situation happens when V_{cm} is large enough to push the input transistors (M3, M4) into *sub-threshold* region, therefore, the drain current of M5 is too low to charge the parasitic capacitors at the $O1+$ and $O1-$ nodes to V_{thn}. Fig. 3(c) presents the schematic simulation results of a typical conventional comparator of ΔT_1 versus V_{Cm}. As expected, for low values of V_{cm} the difference is upper than 160 ps. As V_{cm} increases, the difference increases linearly until $V_{cm} \cong 1$ V, then at $V_{cm} > 1.2$ V the difference tends to infinity. In fact, in the conventional comparator $V_{cm} = 1.2$ V is large enough to reduce the drain current of M5 significantly and increase $T_{pre-amp}$ as it is shown in Fig. 3(a). However, in the proposed method the latch stage remains on during pre-amplification time even when the drain current of M5 reduces significantly.

In the proposed comparator $T_{pre-amp} = 0$ and the first part of the latch delay is better than the conventional one, since the latch stage is activated with a higher V_{cml}. Fig. 4 presents the summation of these two effects along with the real simulated difference. The real simulated difference follows the summation with a fixed error of 180 ps. In the proposed comparator, during the evaluation phase the differential signal at the inputs of the latch stage is smaller than the conventional circuit and (4) predicts this 180 ps difference due to a smaller ΔV_{in}. Nonetheless, the speed of the proposed comparator is better than the conventional comparator. Fortunately, the proposed method is applicable to all kinds of two-stage dynamic comparators to speed up the comparison process, such as the conventional two-stage comparator with NMOS transistors at the input of the preamplifier stage.

In this part, the delay of the proposed comparator is calculated analytically. The working-region of the comparator transistors changes as $V_{cm}[V_{cm} = 0.5(V_{in+} + V_{in-})]$ varies from *Gnd* to *Vdd*. As stated before, to predict the delay precisely, the delay is studied separately for three different ranges of V_{cm}. These ranges are 0–0.7 V, 0.7–1.2 V, and 1.2–1.8 V. In each of these ranges, the input common mode (V_{cml}) and input differential (V_{idl}) voltage of the latch stage are calculated analytically based on the input V_{cm} and V_{id} of the comparator. Finally, analytical equations of V_{cml} and V_{idl} are used in (2), (4), and (1) to calculate the delay.

At the first scenario ($0V < V_{cm} < 0.7V$), M3, M4, and M5 work in the *triode region* during the evaluation phase. In this scenario, the average value of V_p is calculated to derive a simple closed form equation for the delay. At the beginning of the evaluation phase when $V_{O1+,O1-} = 0.5Vdd$, V_p is calculated as follows by employing Kirchhoff Current Law (KCL) at node p [12].

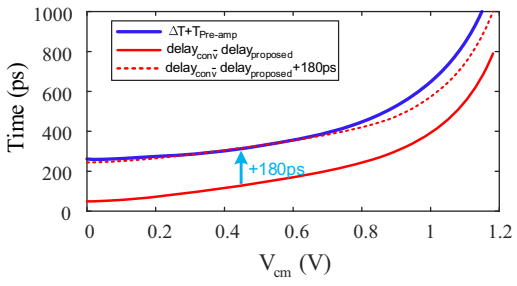

Fig. 4. The difference between simulation results of the delay and the analytical predictions.

$$I = I_1 + I_2$$
$$\mu_p C_{ox}\left(\frac{W}{L}\right)_5\left((\mathrm{Vdd}-\mathrm{V_{th5}})(\mathrm{Vdd}-\mathrm{V_P})-\frac{(\mathrm{VDD}-\mathrm{V_p})^2}{2}\right)$$
$$= \mu C_{ox}\left(\frac{W}{L}\right)_3\left((\mathrm{V_P}-\mathrm{V_{in+}}-\mathrm{V_{th3}})(\mathrm{V_P}-0.5Vdd)-\frac{(\mathrm{V_P}-0.5Vdd)^2}{2}\right)$$
$$+\mu C_{ox}\left(\frac{W}{L}\right)_4\left((\mathrm{V_P}-\mathrm{V_{in-}}-\mathrm{V_{th4}})(\mathrm{V_P}-0.5Vdd)-\frac{(\mathrm{V_P}-0.5Vdd)^2}{2}\right) \quad (8)$$

$V_p(0^+)$ is calculated numerically. During the *evaluation phase*, V_p is charged from its initial value to *Vdd* gradually. Therefore, V_{p-ave} is calculated as follows.

$$V_{p-ave} = 0.5 \times (V_P(0^+) + Vdd) \quad (9)$$

V_{p-ave} is used to approximate the drain current of M3, M4, and M5 during the *evaluation phase*. V_{cml} and V_{idl} are calculated as the following equation. In fact, parasitic capacitors at the output of the first stage of the comparator, C, are charged by I_1 and I_2 currents.

$$V_{cml} = 0.5 \times \left(\frac{I_1}{C}\mathrm{T_1} + \frac{I_2}{C}\mathrm{T_1}\right) + \frac{Vdd}{2} = 0.5 \times \frac{(I_1+I_2)}{C}T_1 = \frac{I}{2C}T_1 + \frac{Vdd}{2} \quad (10)$$

$$V_{idl} = \frac{I_2}{C}\mathrm{T_1} - \frac{I_1}{C}\mathrm{T_1} = \frac{(I_2 - I_1)}{C}\mathrm{T_1} \quad (11)$$

As discussed earlier about (4), T_1 is the time that is required for a latch to be activated and depends on the average value of V_P and V_{cml}. Finally, (10) and (11) are used to calculate the delay.

At the second scenario ($0.7V < V_{cm} < 1.2V$), M3 and M4 work in the saturation-region. M5 works deeply in the triode region so $V_P \cong Vdd$. In this case, the time-domain equations of V_{O1+} and V_{O1-} are derived, then V_{cml} and V_{idl} are calculated at the end of T1. The following differential equation governs the output voltages of the first stage.

$$I_1 = C\frac{dV_{O1+}}{dt} \Rightarrow k_3(Vdd - V_{in+} - V_{th3})^2(1 - \lambda(Vdd - V_{O1+})) = C\frac{dV_{O1+}}{dt} \quad (12)$$

$$I_2 = C\frac{dV_{O1-}}{dt} \Rightarrow k_4(Vdd - V_{in-} - V_{th4})^2(1 - \lambda(Vdd - V_{O1-})) = C\frac{dV_{O1-}}{dt} \quad (13)$$

In which k_i represents $\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_i$. Solving the above equations and substituting initial conditions, V_{O1+} and V_{O1-} are calculated as follows.

$$V_{O1+}(t) = \frac{Vdd}{2} + \left(1 - e^{\left(-\frac{k_3}{C}(Vdd - V_{in+} - V_{th3})^2 \times \lambda \times t\right)}\right) \times \frac{Vdd}{2} \quad (14)$$

$$V_{O1-}(t) = \frac{Vdd}{2} + \left(1 - e^{\left(-\frac{k_4}{C}(Vdd - V_{in-} - V_{th4})^2 \times \lambda \times t\right)}\right) \times \frac{Vdd}{2} \quad (15)$$

In this case, V_{cml} and V_{idl} are calculated as follows.

$$V_{cml} = 0.5(V_{O1+}(T_1) + V_{O1-}(T_1)) \quad (16)$$

$$V_{idl} = V_{O1-}(T_1) - V_{O1+}(T_1) \quad (17)$$

At the last scenario ($1.2 < V_{cm} < 1.8$), M3 and M4 work in the sub-threshold region and M5 is deeply triode again ($V_P \cong Vdd$). The drain current of a MOS transistor which works in the *sub-threshold* region is modeled using the following equation [12].

$$I = I_0 e^{\left(\frac{V_{GS}}{\eta V_T}\right)} \times (1 + kV_{DS}) \quad (18)$$

In this case, the current drown from *Vdd* is very low, therefore, at the end of the evaluation phase $V_{cml} \cong VDD/2$. In fact, the common mode voltage at the output of the first stage remains almost unchanged. As a result, the average V_{DS} of M3 and M4 is almost *Vdd/2*. Therefore, the following equations present precise predictions of the current of the M3 and M4 transistors.

$$I_1 = I_0 e^{\left(\frac{Vdd - V_{in+}}{\eta V_T}\right)} \times \left(1 + k\frac{Vdd}{2}\right) \quad (19)$$

$$I_2 = I_0 e^{\left(\frac{Vdd - V_{in-}}{\eta V_T}\right)} \times \left(1 + k\frac{Vdd}{2}\right) \quad (20)$$

Likewise the previous derivations, V_{idl} is calculated as (21) in which T_1 is calculated using (5) considering $V_{cml} \cong VDD/2$.

$$V_{idl} = \frac{(I_2 - I_1)}{C} \times T_1 \quad (21)$$

To verify the analytical derivations of the delay a comparator is designed in 0.18 um *CMOS* technology. The delay of this comparator is simulated using specter cadence simulator for different values of V_{cm} and V_{id}. Fig. 5 presents the simulation results versus analytical derivations. Obviously, the proposed derivations predict the delay precisely. In Fig. 5(a), as V_{cm} gets closer to the edges of the V_{cm} ranges, the error increases, since the working region of the transistors changes gradually. In Fig. 5(b), the delay of the proposed comparator versus V_{id} is presented.

4. V_{cm} generation

Usually, *Vdd/2* voltage is available in the SAR ADCs [13,15]. If *Vdd/2* is not available in a ADC, another solution is used without imposing power consumption to the original comparator. The key function of *Vs* is to reduce the voltage swing of the first stage. The *Vs* voltage, as a voltage limiter, prevents the output parasitic capacitors of the first stage of the comparator to be discharged to a level lower than *Vdd/2*. Thus, the *Vs* voltage can be implemented using on-chip devices without power consumption, since it sinks current (power). The precision of *Vs* is not important, since it slightly affects the characteristics of the comparator. In fact, *Vs* affects the comparator only at the Reset phase and has a less effect on the evaluation phase. As a result, in the simplest form, a diode or a diode-connected MOS transistor can be used as shown in Fig. 6. This devise prevents the output parasitic capacitors of the comparator to be discharged to lower than a level which can be designed to be *Vdd/2*.

The diode connected NMOS voltage limiter is not an ideal voltage limiter and its current sink capability varies with the drain voltage. Based on the analytical derivations of Section 3, the steady-state output voltage of the pre-amplifier stage at the end of the reset phase is a function of the input V_{cm}. In fact, the voltage at the output nodes of the comparator at the end of the evaluation phase depends on the input V_{cm}. As a results, the limited voltage caused by the diode connected NMOS device is a function of the input V_{cm}. Fig. 7 presents the function for the different size of the diode connected NMOS transistor. As discussed earlier, the variation of the voltage level of the voltage limiter slightly affects the

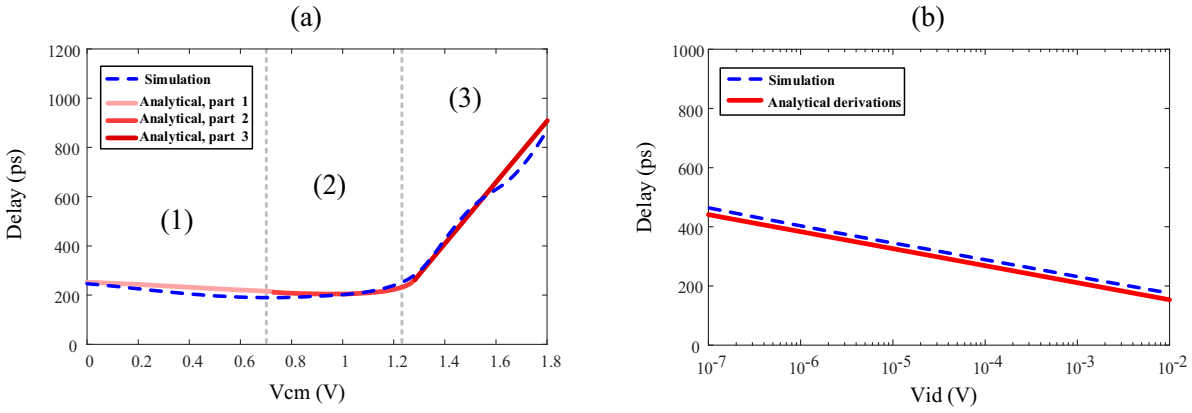

Fig. 5. Analytical derivations versus schematic simulation results of delay-V_{id} and delay-V_{cm} characteristics.

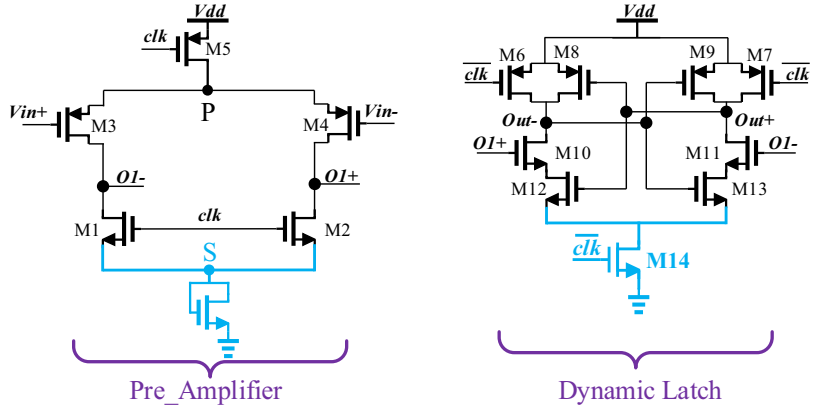

Fig. 6. The proposed two-stage dynamic comparator with a diode connected NMOS as the voltage limiter.

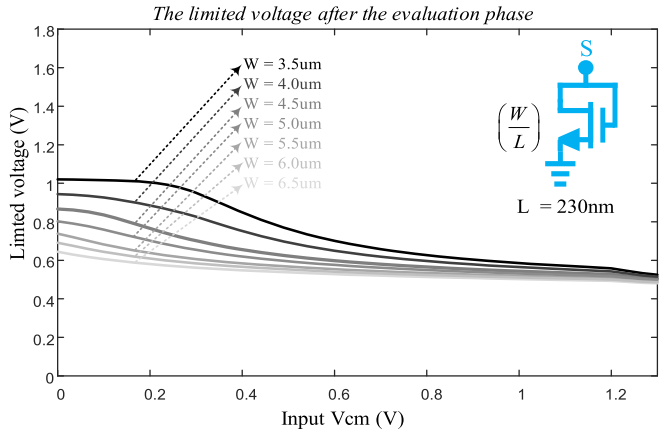

Fig. 7. The voltage variation of the diode connected NMOS voltage limiter.

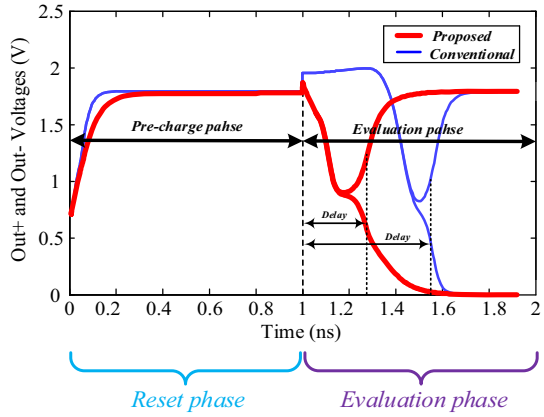

Fig. 8. A comparison between the output voltages of the latch stage in the proposed and the conventional comparators considering a V_{id} of 1 mV.

power consumption and has no effect on the precision, thus, W = 3.5 um seems an acceptable value for diode connected NMOS transistor. Based on the simulation results of Section 5, the area of the diode connected device is less than 3% of the total area of the comparator.

5. Simulation results

Comparators are known as mixed-mode circuits (analog–digital). Therefore, their specifications heavily depend on the in use technology. In order to draw a fair comparison, the proposed and other circuits are carefully designed in 0.18 um CMOS technology. These circuits are designed for similar 2.5 mV input transferred offset voltage and 420 uW power consumption at 500 MHz clock frequency except for the circuits of [6,14]. Those circuits consume significant amounts of power which is not adjustable. Fig. 8 presents the output voltage of the proposed and the conventional comparators during the pre-charge and evaluation phases considering V_{id} = 1 mV. This figure shows that the proposed comparator is faster than the conventional comparator with a factor of two.

Fig. 9(a) presents the delay of all circuits versus V_{id}. As predicted by the analytical derivations, the delay curve is a linear function of the logarithmic scaled input V_{id}. In Fig. 9, the proposed circuit using diode connected NMOS transistors are presented using gray color. Obviously, the delay of the proposed comparator using ideal voltage source of *Vdd/2* and using a diode connected device are almost the same. In all circuits, V_{cm} for those circuits in which the input transistors are *NMOS* and *PMOS* is considered 0.7 V and 1.1 V, respectively. The proposed circuit is faster than other circuits by more than 200 ps. Fig. 9(b) presents the delay versus V_{cm} assuming aV_{id} of 1 mV. This figure is compatible with the analytical derivations discussed in Section 3. The proposed circuit provides the fastest comparison, and its best delay is better than other works by 110 ps. Moreover, the proposed comparator works on a wider input common mode range, since the latch stage is activated stronger and faster compared to other methods. The delay of the comparator is less than 220 ps for a wide input common mode range of 0–1.2 V. For higher common mode voltage levels the speed of the proposed circuit reduces since the in V_{cm} put *PMOS* transistors work in the *sub-threshold* region, unlike [6] in which the input transistors are *NMOS* and work in a strong *active region*.

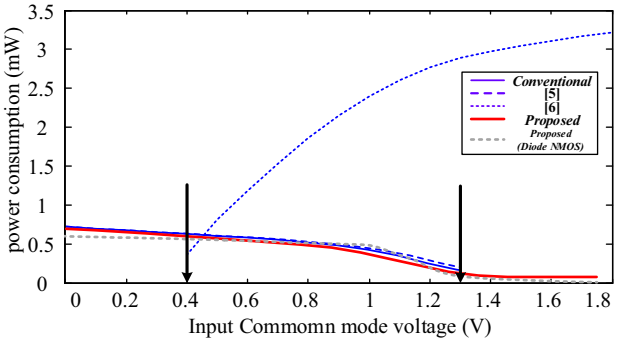

Fig. 10. Power consumption of the proposed and other comparators versus input V_{cm} considering a clock frequency of 500 MHz.

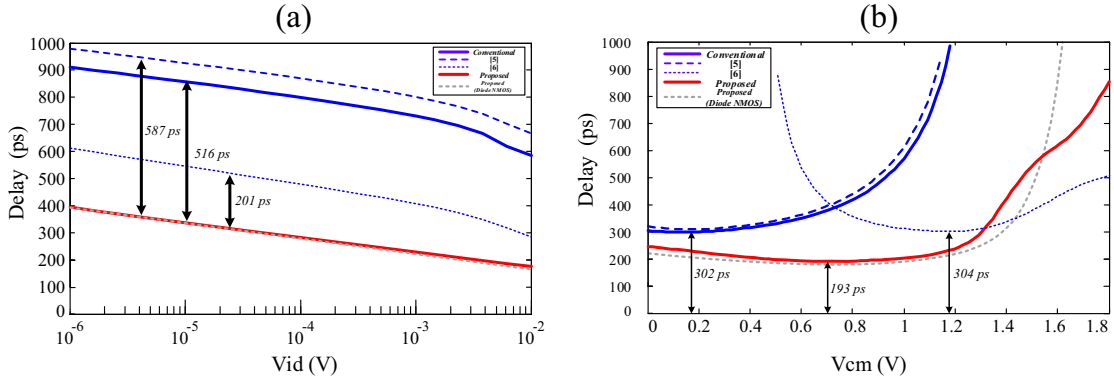

Fig. 9. (a) Comparator's delay versus input V_{id}, (b) comparators delay versus input V_{cm}.

Table 1
Comparison between comparators based on the author simulations.

	Conventional	[5]	[6]	[8]	Proposed
Average power consumption (mW) at 500 MHz	0.42	0.42	2.3	2.75	0.42
Estimated area (μm^2)	434.7	370	574.56	1096	453
Clock frequency (GHz)	2.08	1.92	2.32	2.27	4.54
Common mode range (%*VDD*) at 500 MHz	64%	66%	71%	100%	100%

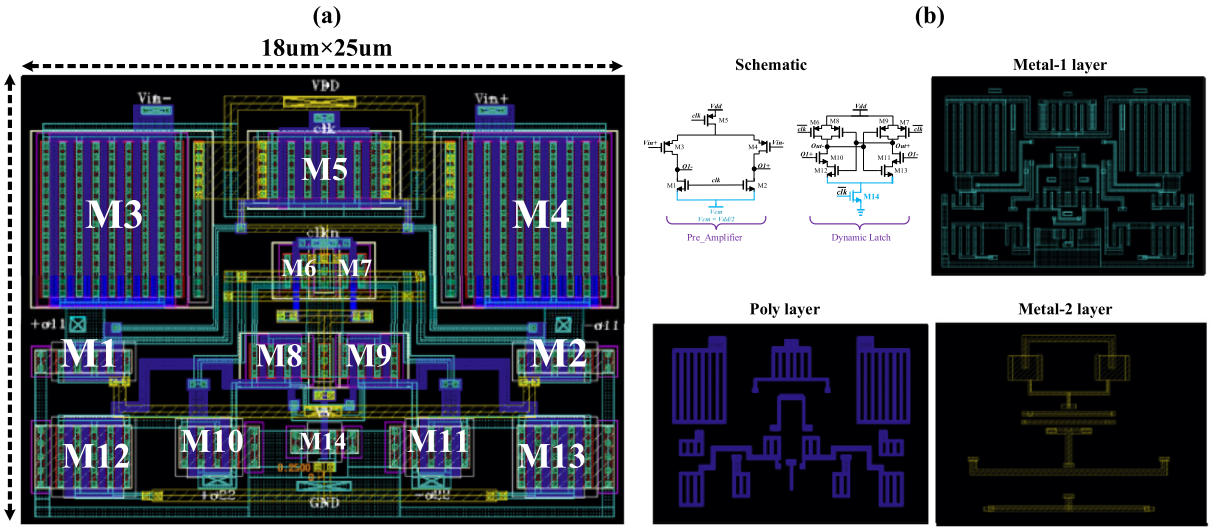

Fig. 11. (a) The layout of the proposed comparator, (b) different layers of the proposed layout.

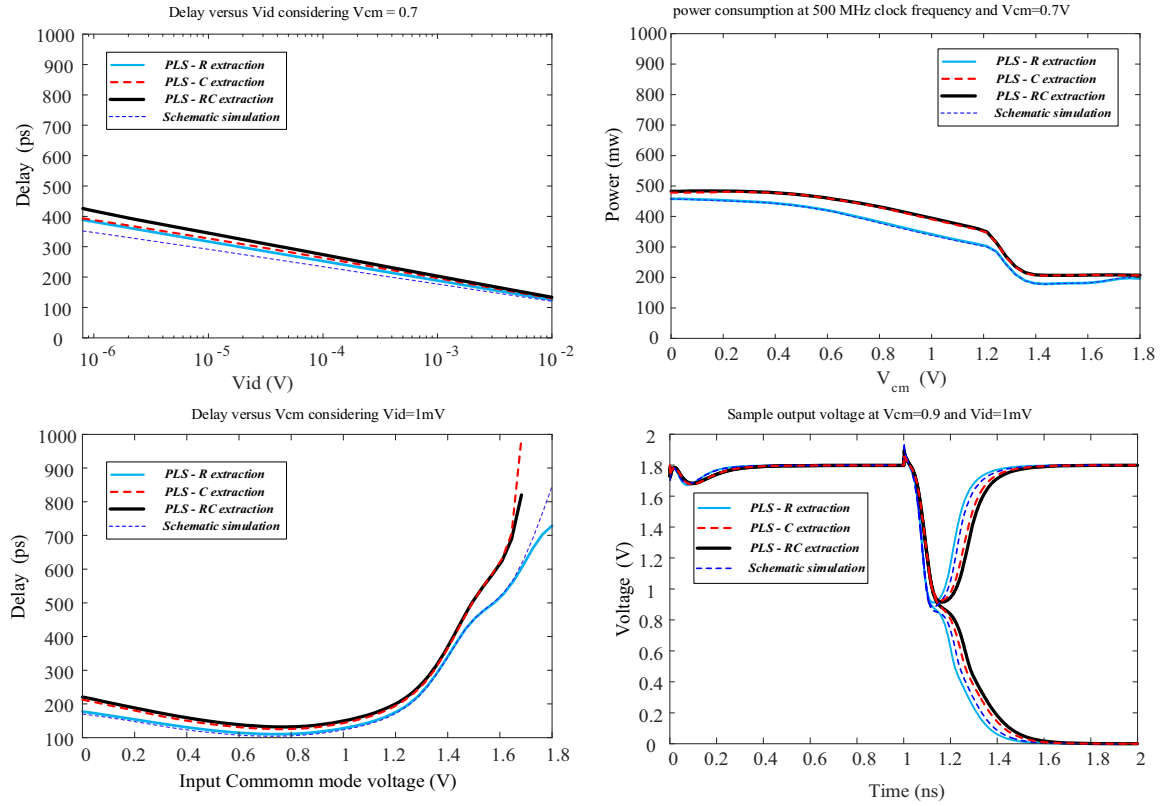

Fig. 12. Post layout simulation results of the proposed comparator versus schematic simulation results.

Table 2
Comparison between the proposed and other comparators.

	[7]	[5]	[6]	[8]	Proposed
Clock (GHz)	–	33 MHz	1 GHz	0.9 GHz	4.54 GHz
Offset voltage (mV)	7.78	0.056	5.62	16.5	2.5
Area (μm^2)	–	64,000	–	260	486
Power (uW)	600	766	–	51	420
Input common mode range ($\times VDD$)	63%	66%	71%	100%	100%
Technology	130 nm	0.5 um	90 nm	90 nm	0.18 um

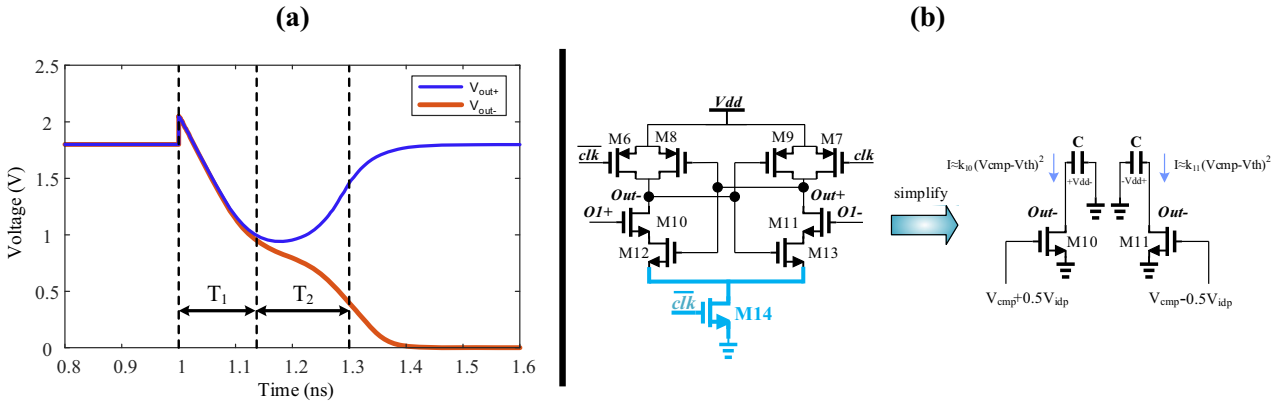

Fig. 13. (a) Typical waveform of a latch with PMOS transistors at the input (PMOS latch), (b) equivalent circuit of a PMOS latch used to calculate T_1.

The power consumption versus input common mode voltage is shown in Fig. 10 while the clock frequency was chosen 500 MHz for all the comparators. The vertical arrows present the lower bound and the upper bound of the input common mode voltage range of the comparators. Fig. 10 shows that the higher speed of the proposed comparator is achieved at almost equal budget of the power consumption. However, the comparator proposed in [6] uses much higher power consumption to provide the high speed comparison.

Table 1 compares the proposed comparator with some other comparators based on author simulations in similar offset voltage budget. In this table, maximum clock frequency is calculated over a V_{cm} range of *Vdd/2*, since in SAR ADCs differential binary weighted capacitive DACs typically offer a V_{cm} range of *Vdd/2* [14]. However, in some works which reduce the power consumption significantly, V_{cm} variation is *0-Vdd* [13,18]. Nonetheless, in recent years the main trend in the range of a DAC has been *VDD/2* to avoid non-linear effects caused by comparator offset variation [15]. As can be seen, the proposed circuit suggests the best clock frequency along with a large input common mode range and an acceptable power consumption.

To further verify the benefits of the proposed comparator, a symmetric layout was provided. Fig. 11 presents this layout. In order to achieve such a symmetric layout, the finger number of all of the transistors should be chosen carefully. Fortunately, thanks to the symmetric layout, the static offset voltage caused by the layout parasitic components was measured less than 70 uV over a complete range of V_{cm}. In fact, cross-coupled circuits cannot be laid out fully symmetric. Therefore, the layout designers try to make a layout as symmetric as possible. Here, we have tried to minimize the capacitor mismatch at the output of the first stage to avoid unexpected offset voltage. As shown in Fig. 11(b), there is only one asymmetric interconnect which happens in the metal-1 layer.

Post layout simulations (PLS) are performed to be compared with the schematic simulation results. Fig. 12 presents PLS results along with the schematic simulation results. In this figure, R-extracted, C-extracted, and RC-extracted simulation results are presented. Fortunately, by virtue of the compactness and symmetry of the layout, PLS results almost match the schematic simulation results.

Table 2 presents a comparison between the proposed and previously reported circuits. Obviously, the proposed circuit presents a high-speed comparator with acceptable amounts of power consumption and offset voltage. Through using the proposed circuit, the maximum clock frequency of 4.5 GHz is achieved. Also, the proposed method of limiting the voltage swing of the preamplifier stage can be used in all two-stage dynamic comparators to increase the comparison speed. As a result, the proposed comparator is an efficient candidate for high-speed low-power applications. Moreover, this comparator can significantly reduce the power consumption in those applications where more than one comparator is required in an ADC, such as the ADC's reported in [16–18].

6. Conclusion

A high speed low power comparator is presented. In this circuit, the voltage variation of the first stage is limited to $Vdd/2$. Therefore, the power consumption of the first stage which is the dominant part of the total power consumption is reduced. Moreover, the speed of the circuit and maximum input common mode range is increased. That is because owing to the higher common mode voltage at the output of the first stage, the delay of the latch stage is reduced. Analytical derivations of the delay verify the high speed benefit of the proposed comparator. Moreover, solid analysis is presented that models the delay of the comparator. Simulation results in equal budget of power consumption and offset voltage as well post layout simulations prove the advantages of the proposed comparator over the state of the art of published works.

Appendix 1. Delay of the dynamic latch

Fig. 13(a) presents a typical waveform of a PMOS latch. Based on this figure, the delay of a latch can be divided into two parts.

Firstly, the voltage of the output nodes discharges from *VDD* to $VDD - V_{thn}$ with almost the same rate considering a small differential voltage at the input (since the differential voltage at the output of the preamplifier stage is small). Then the PMOS transistors turn on (M8, M9) and the back to back inverter starts to amplify its input differential voltage until it locks. Eq. (1) presents an approximation of the second delay. To praise the first delay of the latch when it is in the comparator circuit, the signal at the both inputs of the latch are assumed to be V_{cml} neglecting the differential voltage. In this case, when the latch is activated M_{12-14} are deeply triode, M_{6-7} are off and $M_{10,11}$ work in the saturated region. Therefore, the equivalent circuit of Fig. 13(b) is obtained. If a capacitor is charged using a DC current source the voltage of the capacitor and the charging time are calculated as follows.

$$V_c(t) = \frac{I}{C}t \Rightarrow t = \frac{C}{I}\Delta V \tag{22}$$

Consequently, the delay which is the time required to discharge the output nodes as large as V_{thp} is derives as follows

$$T_1 = \frac{C}{I} \times \Delta V = \frac{C \times (VDD - (VDD - V_{thp}))}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{10,11}(V_{GS} - V_{thn})^2} = \frac{C \times V_{thp}}{\frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{10,11}(V_{cml} - V_{thn})^2} \tag{23}$$

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