Hybrid-Switching Full-Bridge DC–DC Converter With Minimal Voltage Stress of Bridge Rectifier, Reduced Circulating Losses, and Filter Requirement for Electric Vehicle Battery Chargers

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***Abstract*—This paper first presents a hybrid-switching step-down dc–dc converter, and then, by introducing transformer isolation, a novel hybrid-switching phase-shift full-bridge dc–dc converter is derived for electric vehicle battery chargers. The proposed converter provides wide zero-voltage-switching range in the leading-leg switches, achieves zero-current-switching for lagging-leg switches, and uses a hybrid-switching method to avoid freewheeling circulating losses in the primary side. Because the resonant capacitor voltage of the hybrid-switching circuit is applied between the bridge rectifier and the output inductor for the duration of the freewheeling intervals, a smaller sized output inductor can be utilized. With the current rectifier diode of the hybrid-switching circuit providing a clamping path, the voltage overshoots that arise during the turn-off of the rectifier diodes are eliminated and the voltage stress of bridge rectifier is clamped to the minimal achievable value, which is equal to secondary-reflected input voltage of the transformer. The inductive energy stored in the output inductor and the capacitive energy stored in the resonant capacitor of the hybrid-switching circuit are transferred to the output simultaneously during the freewheeling intervals with only one diode in series in the current path, achieving more effective and efficient energy transfer. The effectiveness of the proposed converter was experimentally verified using a 3.6-kW prototype circuit designed for electric vehicle onboard chargers. Experimental results of the hardware prototype show that the converter achieves a peak efficiency of 98.1% and high system efficiencies over wide output voltage and power ranges.**

***Index Terms*—Hybrid-switching method, phase-shift full-bridge dc–dc converter, plug-in electric vehicle battery charger, zero-current-switching, zero-voltage-switching.**

I. Introduction

PLUG-IN hybrid electric vehicles (PHEV) utilize a high-voltage battery pack with high-energy density to store energy for the electric traction system. The high-energy battery pack can be charged from the ac outlets by an ac–dc charger, which typically includes a frond-end power factor corrector (PFC) followed an isolated dc–dc converter [1]–[8]. The frond-end PFC is used to improve the quality of the input current and to regulate dc bus voltage; the dc–dc converter is used to charge the high-voltage pack and provide isolation between the utility mains and the traction battery pack.

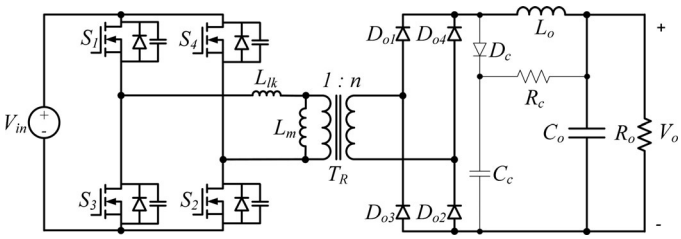

Fig. 1. Conventional PSFB dc-dc converter with an RCD snubber.

The zero-voltage-switching (ZVS) phase-shift full-bridge (PSFB) converter, as shown in Fig. 1, is the most popular topology in the power range of a few kilowatts (1–5 kW) for battery chargers [8]–[33]. The ZVS for primary switches of PSFB dc–dc converters can be achieved using the leakage inductance of the transformer and the junction capacitances of the devices without additional components. However, there are several fundamental limitations with the traditional ZVS PSFB dc–dc converter. The first limitation is the limited ZVS range for lagging-leg switches. The output power range is very wide for battery charger applications. Since the ZVS of the lagging-leg switches is achieved with the energy stored in the leakage inductor, the lagging-leg switches tend to lose ZVS at light load conditions. The ZVS range can be extended to lower load operations by increasing the leakage inductance of the transformer [9] or by adding an external series inductor [3]. However, a large leakage or series inductance extends the time required for the primary current to change direction from negative to positive, and vice versa, which results in a loss of effective duty cycle on the secondary side of transformer and decreases the conversion efficiency. Normally, a transformer with higher turns ratio is required to compensate the secondary-side duty-cycle loss. With a higher turns ratio, the reflected output current into the primary side is increased, which results in higher primary-side conduction losses. In addition, the higher turns ratio increases the voltage stress on the secondary-side bridge rectifier. A number of techniques which utilize the inductive energy stored in the additional auxiliary

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circuits instead of in the leakage or external series inductance to extend the ZVS range have been proposed [11]–[15]. However these proposed methods cannot optimally resolve the trade-off between power-loss savings obtained by the wide- or full-load-range ZVS and power losses of the auxiliary circuits for electric vehicle battery charger applications, where a very wide load and duty cycle range operations are required. The second limitation of traditional ZVS PSFB dc–dc is that during the freewheeling intervals, the primary current, which is reflected from the output inductor current, circulates through the primary side, causing excessive conduction loss. In battery charger applications, the output voltage range is very wide, which requires the PSFB dc–dc converter to operate with a wide duty cycle range. At small duty cycle and high-power conditions, the circulating losses during the freewheeling intervals become severe, significantly degrading the conversion efficiency. The third major limitation with the conventional PSFB dc–dc converter for high output voltage applications is the severe voltage overshoots and oscillations across the output diodes when they are turned OFF. Quite a few solutions have been proposed to solve this problem. Since the voltage overshoots are basically caused by the parasitic ringing between the junction capacitors of the rectifier diodes and transformer leakage inductance, some solutions tried to decrease the leakage inductance as much as possible through special arrangement of transformer windings. However, reducing the leakage inductance will result in a very narrow range of ZVS operation for the lagging-leg switches. In [10], an RCD snubber circuit was used to mitigate the voltage overshoots across the bridge rectifier. The main problem with the snubber circuit is the amount of loss in the snubber resistor, which considerably degrades the efficiency of the converter especially during high-power operation. The active clamp method in [16] solved the efficiency degradation problem and effectively clamped the voltage spike of the output diodes. However, the active clamp circuit increases the complexity of the converter and degrades the system reliability because an additional gate driver circuit is required to control the secondary active switch. Several energy recovery clamp circuits (ERCCs) with lossless passive components have been proposed in [17]–[24] to relieve the effect of the voltage overshoots. Although these ERCC techniques are able to reduce the voltage stresses of the output diodes, the magnitude of the voltage stresses depends on the duty cycle [17], [18] and the output voltage value [19]–[24]. Hence, these techniques are not preferred in battery charger applications, where the wide ranges of duty cycle and output voltage operations are required.

II. Proposed Solution/Topology

In order to overcome the aforementioned limitations of the conventional PSFB dc–dc converter for high-voltage electric vehicle battery charger applications, a novel hybrid-switching phase-shift full-bridge (HSPSFB) dc–dc converter as shown in Fig. 2(c) is presented. This converter is essentially derived by introducing transformer isolation [34] into a novel nonisolated hybrid-switching step-down (HSSD) dc–dc converter, as shown in Fig. 2(b). This HSSD dc–dc converter belongs to a new category of switching converters named hybrid-switching converters [35], [36] recently invented by Cuk. This HSSD dc–dc converter is characterized by hybrid resonant and PWM waveforms of currents and voltages. The charge balance of the resonant capacitor is satisfied by hybrid linear PWM current and sinusoidal resonant current. Such power conversion can lead to much reduced voltage stresses on switches when compared to the best PWM converters with the same dc conversion ratio.

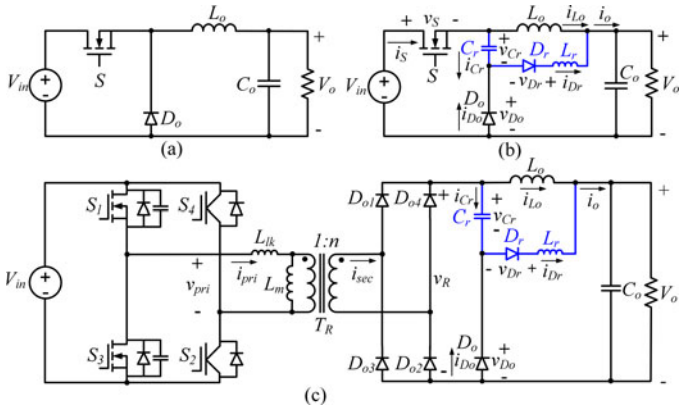

Fig. 2. (a) Conventional PWM buck dc–dc converter, (b) proposed hybrid-switching step-down dc–dc converter, (c) proposed ZVZCS hybrid-switching full-bridge dc–dc converter.

The proposed converter in Fig. 2(c) transfers energy from input to output and simultaneously stores energy in the resonant capacitor C_r and output inductor L_o during the active intervals. During the freewheeling intervals, the capacitive energy stored in the resonant capacitor C_r and inductive energy stored in the output inductor L_o are simultaneously transferred to the output with only one series diode in the current path, achieving effective and efficient energy transfer. The hybrid-switching circuit provides additional current to assist ZVS for leading-leg switches and resets the primary current to zero instantly at the start of freewheeling intervals. As a result, the leading-leg switches can achieve ZVS over a wide power range and lagging-leg switches can achieve ZCS at turn-off. The primary circulating currents during the freewheeling intervals of the conventional PSFB dc–dc converter are also mitigated, greatly reducing the conduction losses. As a result of the resonant capacitor voltage v_{Cr} being applied between the bridge rectifier and the output inductor during the whole freewheeling interval, a smaller output inductor which has compact size and light weight can be utilized. The voltage ringing and overshoots that arise during the turn-off of the output diodes associated with conventional PSFB dc–dc converter are also eliminated and the voltage stresses on the bridge rectifier diodes are well clamped to the secondary-reflected input voltage, greatly reducing the voltage stresses on the rectifier diodes and providing enhanced reliability.

With a simple structure, physically smaller output inductor, minimized voltage stress across the bridge rectifier, and high efficiency over wide output power and voltage ranges, this converter is very attractive for electric vehicle battery charger applications. The analysis, advantages, and design considerations of the proposed converter will be described in detail in this paper. A 3.6-kW prototype circuit has been implemented to verify

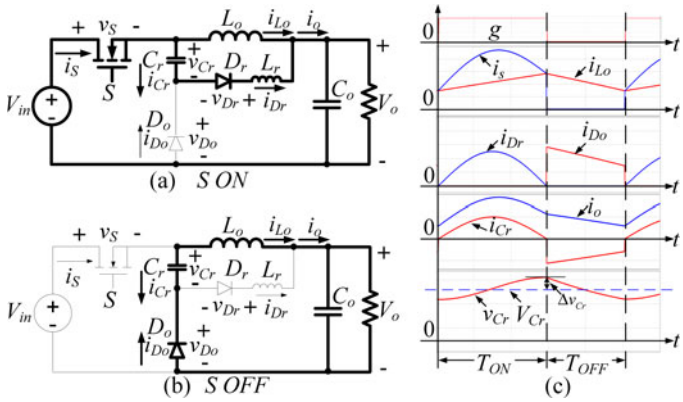

Fig. 3. (a) Topological stage during on-time interval, (b) topological stage during off-time interval, and (c) key waveforms.

the basic operation and performance of the proposed converter under different output voltage and power conditions.

III. Basic Operation of the Proposed HSSD DC–DC Converter

The operation of a traditional buck converter, as shown in Fig. 2(a), is based on the inductive energy storage and transfer only. The proposed HSSD dc–dc converter in Fig. 2(b) has an additional capacitive energy storage and transfer from input to output through use of the hybrid-switching method. This reduces the voltage stresses and switching losses of the switches. The optimal operating mode of the HSSD dc–dc converter is constant on-time and variable off-time control [35], [36] where the on-time is always equal to half of the resonant period as

$$T_{\rm ON} = D \cdot T_s = \frac{T_r}{2} = \pi\sqrt{L_r C_r}. \tag{1}$$

In this operation mode, the current rectifier diode D_r turns OFF with zero current. This eliminates the undesirable diode reverse-recovery current induced losses which are especially prevalent in high-voltage applications. This in turn also minimizes turn-off losses of the main switch *S*.

The topological stages and key waveforms of the HSSD dc–dc converter are shown in Fig. 3, where *g* represents the gating signal. The energy storage and transfer process during on-time interval $T_{\rm ON}$ and off-time interval $T_{\rm OFF}$ is

1) *Charge interval [see Fig. 3(a)]*: the source current during this on-time interval:
   a) charges the resonant capacitor C_r;
   b) stores the inductive energy in the output inductor L_o;
   c) delivers power to the load with combined resonant and PWM currents.

Discharge interval [see Fig. 3(b)]: During this off-time interval:

a) inductive energy stored in the output inductor L_o is passed to the load;
b) capacitive energy in the capacitor C_r is passed to the load.

Note that the resonant capacitor C_r is charged in a resonant way during the on-time interval $T_{\rm ON}$ and discharged linearly as in PWM converters during the off-time interval $T_{\rm OFF}$. Note also that the resonant inductor L_r is fully flux-balanced during the on-time interval only. The flux-balance condition on this resonant inductor L_r leads to

$$V_{Cr} = V_{\rm in} - V_o. \tag{2}$$

Flux balance on the output inductor during the whole switching period leads to

$$(V_{\rm in} - V_o) \cdot DT_s = (V_o - V_{Cr}) \cdot (1 - D)T_s. \tag{3}$$

Combining (2) and (3) results in

$$M = V_o/V_{\rm in} = 1/(2 - D). \tag{4}$$

The voltage stresses of switches can be derived as

$$V_s = V_{\rm in} - V_{Cr} = V_o = V_{\rm in}\frac{1}{2 - D} \tag{5}$$

$$V_{Do} = V_{Dr} = V_o = V_{\rm in}\frac{1}{2 - D}. \tag{6}$$

The voltage conversion ratios and voltage stresses of the devices of the proposed HSSD and traditional buck dc–dc converters are shown in Fig. 4(a) and (b), respectively. Fig. 4(a) and (b) illustrates that for the same duty cycle, the proposed HSSD can achieve a higher voltage conversion ratio with much reduced voltage stresses of switches.

IV. Steady-State Operation Mode Analysis of the Proposed HSPSFB DC–DC Full-Bridge Converter

By introducing transformer isolation into the above proposed HSSD dc–dc converter and applying phase-shift PWM control, a high-efficiency HSPSFB dc–dc converter is presented, as shown in Fig. 2(c). The optimal control mode, which changes the freewheeling interval time while keeping the active interval equal to half of the resonant period, can be applied to the proposed HSPSFB dc–dc converter. However, the wide range of output voltage can also simply be regulated by traditional phase-shift PWM control with fixed switching frequency. Moreover, the resonant inductor L_r can be removed in favor of using the leakage inductor $L_{\rm lk}$ of a transformer to resonate with the capacitor C_r, further reducing the number of components. IGBTs instead of MOSFETs are utilized as the lagging-leg switch es in our report due to the facts that the costs of IGBTs are much lower than MOSFETs and IGBTs are in favor of ZCS because the tailed-current-induced losses of IGBTs are minimized with zero-current turn-off.

Since traditional phase-shift PWM control with fixed switching frequency and variable duty ratio is applied to the proposed HSPSFB dc–dc converter, three distinct operation modes, designated as Mode 1, Mode 2, and Mode 3, as discussed in [36], exist, according to the following simple quantitative criteria:

Mode 1	Mode 2	Mode 3
$T_{Active}>t_r$	$T_{Active}=t_r$	$T_{Active}<t_r$

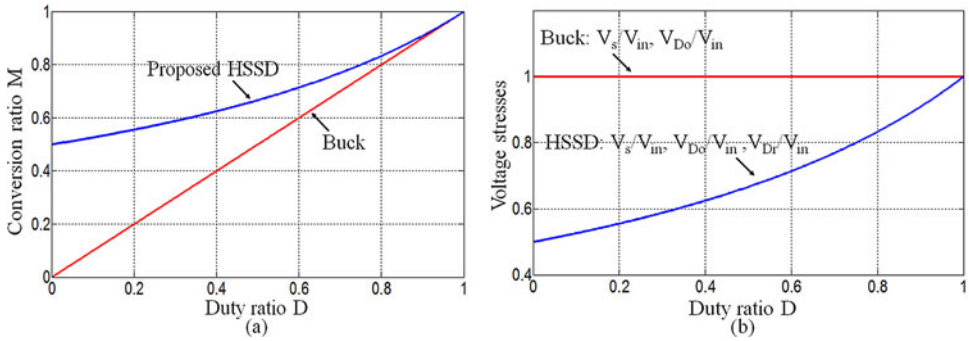

Fig. 4. (a) Voltage conversion ratios of the proposed HSSD and buck dc–dc converters. (b) Voltage stresses of devices of the proposed HSSD and buck dc–dc converters.

where t_r is the half of the resonant period T_r, expressed as follows:

$$t_r = \frac{T_r}{2} = \pi n \sqrt{L_{\rm lk} C_r} \tag{7}$$

and $T_{\rm Active}$, as expressed in (2), is the duration of the active interval of the PSFB dc–dc circuit

$$T_{\rm Active} = D \cdot \frac{T_s}{2}. \tag{8}$$

These three operation modes can be distinguished by the resonant current i_{Dr} through the diode D_r. In Mode 1 operation, the resonant current i_{Dr} reaches zero before the converter enters into the freewheeling intervals. In Mode 2 operation, the resonant current i_{Dr} reaches zero at the instant when the converter enters into the freewheeling intervals. In Mode 3 operation, the resonant current i_{Dr} is higher than zero and is interrupted at the instant the converter begins freewheeling.

A. Mode 1 Operation ($T_{\rm Active} > t_r$)

There are six topological stages within each half-switching cycle for Mode 1 operation. The equivalent operation circuits and key waveforms for different topological stages are shown in Figs. 5 and 6, respectively. In Fig. 6, g_1–g_4 represent gating signals applied to the devices S_1–S_4 and the definitions of $v_{\rm pri}$, $i_{\rm pri}, i_{\rm sec}, i_o, i_{Lo}, i_{Dr}, i_{Do}, i_{Cr}, v_{Ch}$, and v_R are shown in Fig. 2(c). The magnetizing current of the transformer is neglected due to its relatively small value.

Stage 1 ([t $_0$, t_1]) [see Fig. 5(a)]: prior to t_0 both the primary and secondary currents of the transformer are zero. All the bridge rectifier diodes are OFF because they are reverse biased by C_r; only the primary switch S_1 is ON. The energy stored in C_r is passed to the output through D_o and L_o. Switch S_2 is turned ON at time t_0, both primary and secondary currents start to increase linearly from zero. The duration of this period can be expressed as

$$\Delta t = t_1 - t_0 \cong \frac{n \cdot i_{Lo}(t_1) \cdot L_{\rm lk}}{V_{\rm bus} - v_{Cr}/n}. \tag{9}$$

Since the secondary current $i_{\rm sec}$ is lower than the output inductor current i_{Lo} during this period, diode D_o is kept ON and the energy stored in the capacitor C_r is passed to the output until the secondary current $i_{\rm sec}$ is equal to the output inductor current i_{Lo}.

Stage 2 ([t $_1$, t_2]) [see Fig. 5(b)]: at time t_1, the secondary current $i_{\rm sec}$ becomes higher than i_{Lo}, diode D_o is reverse biased and diode D_r is ON. Leakage inductor $L_{\rm lk}$ starts to resonate with C_r, transferring energy from the input to the output in resonant mode. The primary current $i_{\rm pri}$ is the sum of the resonant current i_{Dr} through the diode D_r and the PWM current i_{Lo} through the output inductor L_o reflected to the primary side, expressed as

$$i_{\rm pri} = n \cdot (i_{Lo} + i_{Dr}). \tag{10}$$

Hence, the energy transferred through the transformer T_R is a parallel combination of linear PWM and sinusoidal resonant modes, increasing the total power delivery from the input to the output.

Stage 3 ([t $_2$, t_3]) [see Fig. 5(c)]: at time t_2, i_{Dr} resonates to zero and diode D_r turns OFF with zero current. Transformer T_R continues to transfer energy from input to output with the secondary current equal to i_{Lo} as in a traditional PSFB dc–dc converter.

Stage 4 ([t $_3$, t_4]) [see Fig. 5(d)]: at time t_3, S_1 turns OFF, the primary side current $i_{\rm pri}$ starts to charge and discharge the junction capacitors of the leading-leg switches. When the drain–source voltage of S_3 reaches to zero, $i_{\rm pri}$ flows through the body diode of S_3. After the dead time, S_3 is turned ON with ZVS.

Stage 5 ([t_4, t_5]) [see Fig. 5(e)]: at time t_4, the secondary current $i_{\rm sec}$ is lower than the output inductor current i_{Lo}, so diode D_o becomes forward biased. The capacitor voltage v_{Cr} is applied across the bridge rectifier. As a result, the primary current $i_{\rm pri}$ is quickly reset to zero, providing ZCS turn-off of lagging leg switches and reducing the primary circulating losses. The duration of this period can be expressed as

$$\Delta t = t_5 - t_4 \cong \frac{n \cdot i_{Lo}(t_4) \cdot L_{\rm lk}}{v_{Ch}/n}. \tag{11}$$

Stage 6 ([t $_5$, t_6]) [see Fig. 5(f)]: at time t_5, both the primary and secondary currents of the transformer are reduced to zero, the stored capacitive energy in C_r and inductive energy in L_o are passed to the output simultaneously through diode D_o until the switch S_4 turns ON at t_6. Since the resonant capacitor voltage v_{Cr} is always higher than zero, the bridge rectifier is reversed biased by the resonant capacitor C_r and never conducts during this freewheeling stage. Traditional PSFB converters have two diode voltage drops in the current path during this freewheeling stage due to the bride rectifier conducting the output inductor

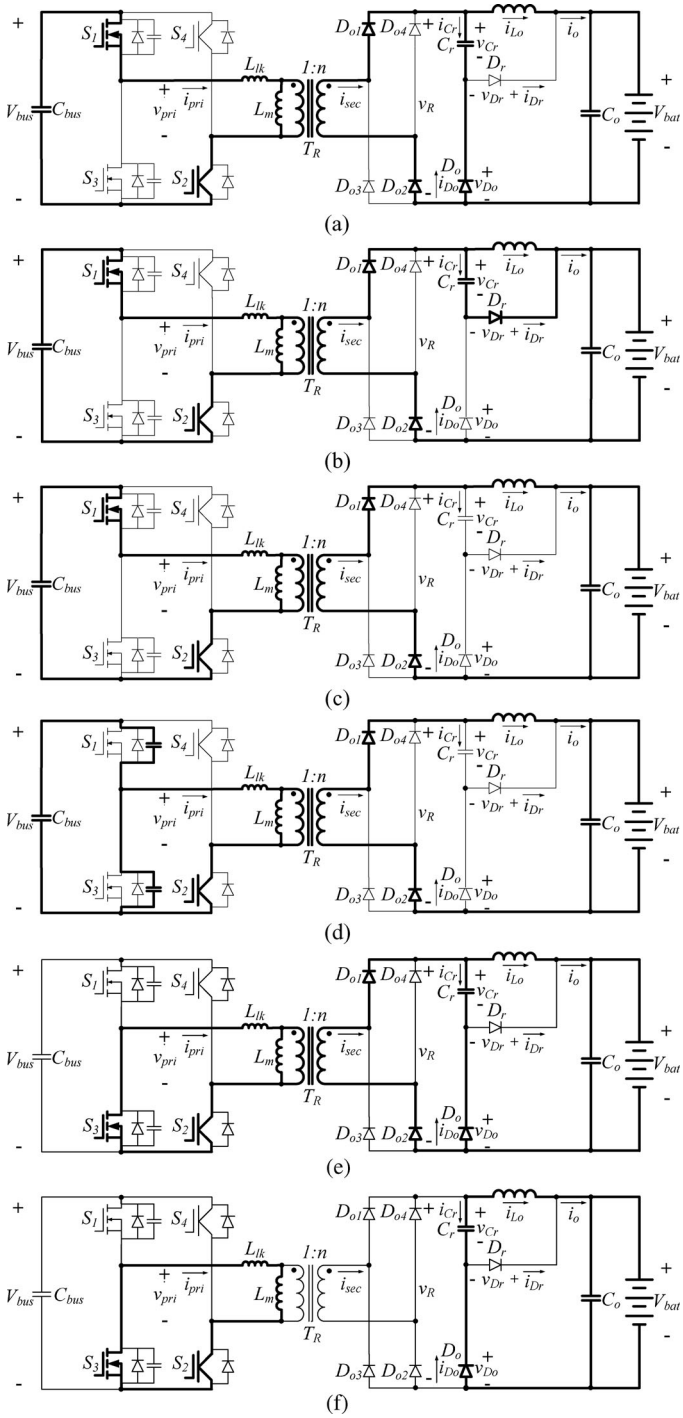

Fig. 5. Topological stages of the proposed HSPSFB dc–dc converter in Mode 1 operation. (a) $[t_o, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, (d) $[t_3, t_4]$, (e) $[t_4, t_5]$, and (f) $[t_5, t_6]$.

current. For the proposed converter, only one diode D_o is in the current path during this freewheeling stage, reducing the fixed voltage drop by half and transferring energy more efficiently.

B. Mode 2 Operation ($T_{\text{Active}} = t_r$)

The key waveforms for Mode 2 operation are shown in Fig. 7. It is similar to Mode 1 operation; the only difference is that Stage 3 of Mode 1, as shown in Fig. 5(c), does not exist in Mode 2 because the switch S_1 is turned OFF at the instant resonant current i_{Dr} reaches zero. The other five stages are same as in Mode 1.

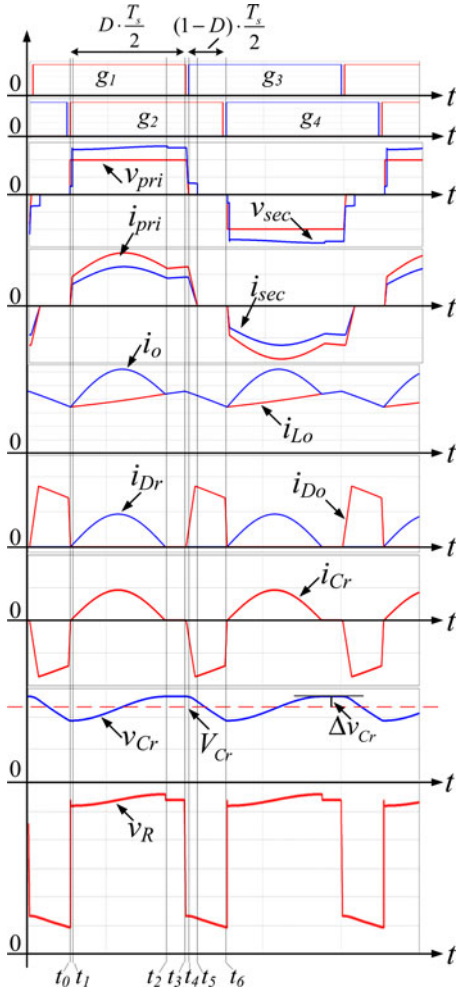

Fig. 6. Key waveforms of the proposed HSPSFB dc–dc converter in Mode 1 operation.

C. Mode 3 Operation ($T_{\text{Active}} < t_r$)

Fig. 8 shows the key waveforms of Mode 3 operation for the proposed converter. Because the half resonant period of the hybrid-switching circuit is longer than the active interval of the HSPSFB dc–dc converter, the resonant current i_{Dr} is higher than zero and the resonance is stopped at the time instant t_3 when the proposed converter starts to enter into the freewheeling period. The topological Stages 1 and 2 for Mode 3 operation are same as in Mode 1 operation, and are shown in Fig. 5(a) and (b). The topological Stage 3 for Mode 3 operation is shown in Fig. 9.

Stage 3 ([t 2, t3]) [see Fig. 9]: at time t_2, S_1 is turned OFF and the current i_{pri}, which is composed of the reflected output inductor current $n{\cdot}i_{Lo}$ and the reflected resonant current $n{\cdot}i_{Dr}$, starts to charge and discharge the junction capacitors of switches S_1 and S_3, respectively. When the drain–source voltage of S_3 reaches zero, the current i_{pri} flows through the body diode of S_3.

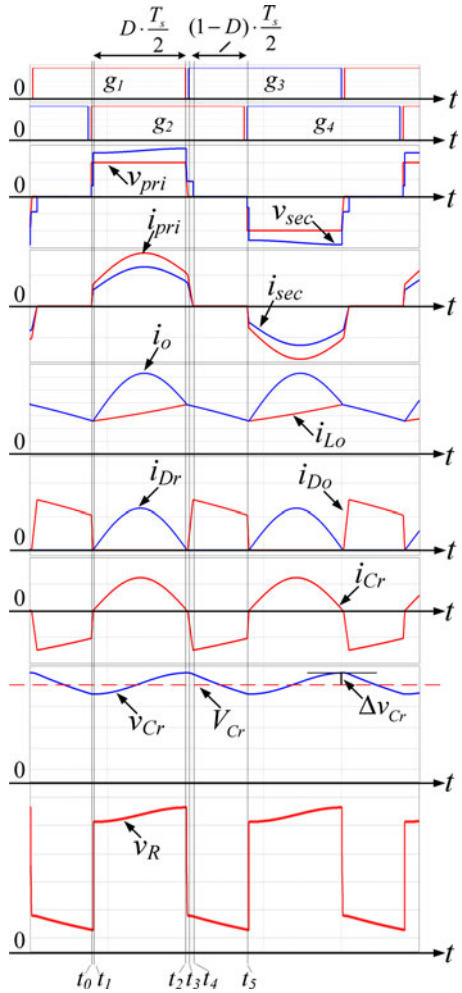

Fig. 7. Key waveforms of the proposed HSPSFB dc–dc converter in Mode 2 operation.

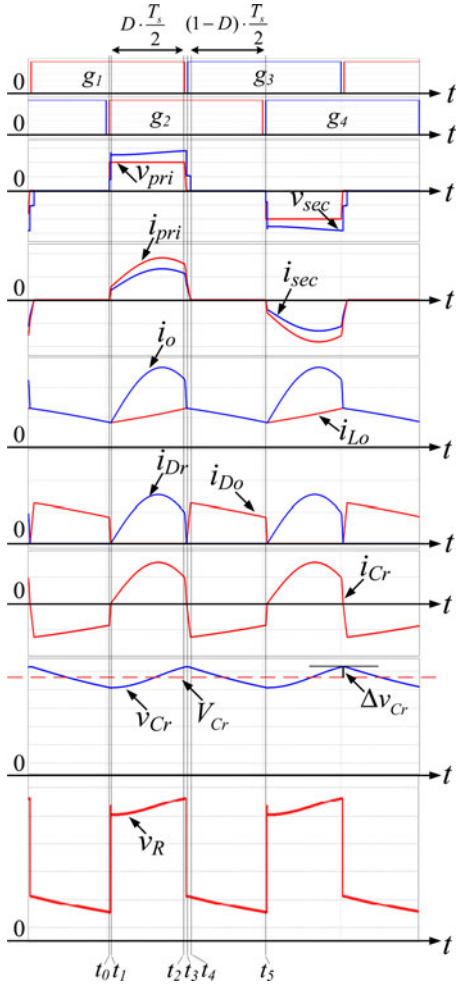

Fig. 8. Key waveforms of the proposed HSPSFB dc–dc converter in Mode 3 operation.

After the dead time, S_3 is turned ON with ZVS. The current that charges and discharges the junction capacitors of the devices in Mode 1 and Mode 2 consists only of the reflected output inductor current. In Mode 3, the addition of the reflected resonant current extends the ZVS operation range of the leading-leg switches. The topological Stages 4 and 5 of Mode 3 operation are the same as the topological Stages 5 and 6 of Mode 1 operation, which are shown in Fig. 5(e) and (f).

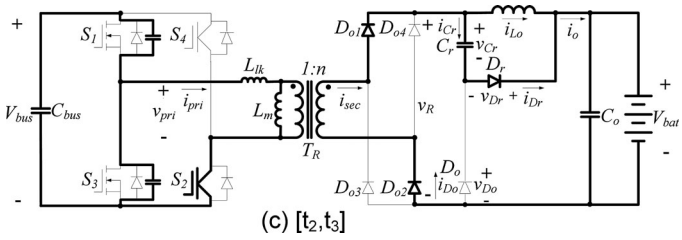

Fig. 9. Topological Stage 3 in Mode 3 operation.

V. Features of the Proposed HSPSFB DC–DC Converter

A. Hybrid Resonant and PWM Power Transfer During Active Intervals and Simultaneous inductive and Capacitive Energy Transfer During Freewheeling Intervals

The steady-state secondary-side equivalent circuits of traditional PSFB dc–dc converters and the proposed HSPSFB dc–dc converter are comparatively shown in Fig. 10. During the active intervals, the proposed converter has an additional resonant current path, as shown in Fig. 10(b), to transfer energy from the input to the output in parallel with the linear PWM current path, increasing the total power delivery from the source to the load. During the freewheeling intervals, traditional PSFB dc–dc converters pass the stored inductive energy only to the output with two diode voltage drops in the current path, as shown in Fig. 10(c). For the proposed converter, due to the fact that the resonant capacitor voltage v_{Cr} is always higher than zero, the bridge rectifier diodes are all reverse biased during the freewheeling intervals. The inductive energy stored in the output inductor L_o and the capacitive energy stored in the resonant capacitor C_r are passed to the output simultaneously with only one diode voltage drop in the current path, achieving more effective and efficient energy transfer.

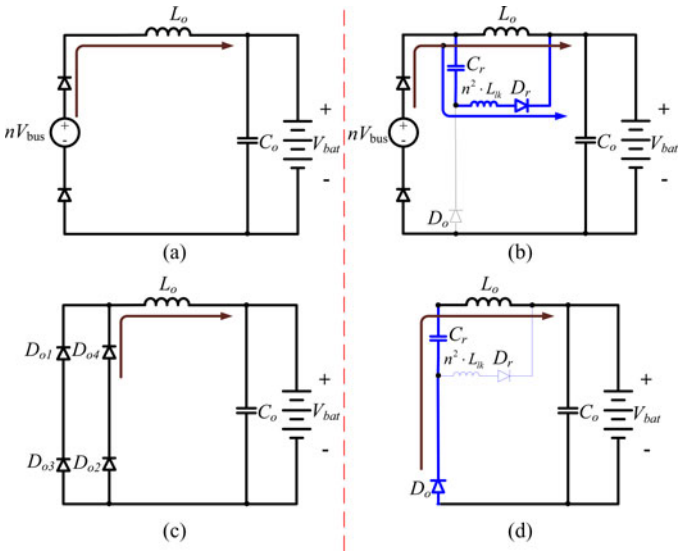

Fig. 10. Steady-state secondary-side equivalent circuits of traditional PSFB dc–dc converter and the proposed HSPSFB dc–dc converter. (a) Active stage of traditional PSFB dc-dc converter. (b) Active stage of proposed HSPSFB dc-dc converter. (c) Freewheeling stage of traditional PSFB dc-dc converter. (d) Freewheeling stage of proposed HSPSFB dc-dc converter.

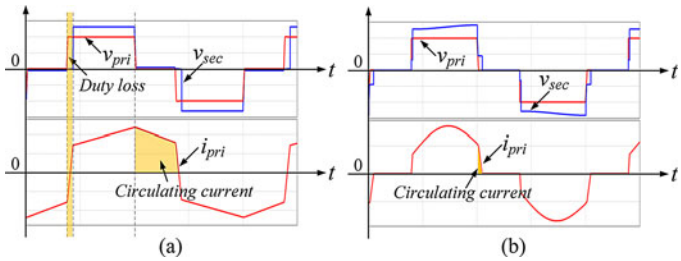

Fig. 11. Comparative analysis of duty loss and circulating currents: (a) conventional PSFB converter and (b) proposed HSPSFB dc–dc converter.

B. Minimized Circulating Losses and Nearly Zero Duty-Cycle Loss

Fig. 11 illustrates the primary circulating current and the duty-cycle losses of the traditional PSFB dc–dc converter and the proposed HSPSFB dc–dc converter. For traditional ZVS PSFB converter, the circulating current, as shown in Fig. 11(a), which flows through the trasnformer and primary switches during freewheeling intervals, is reflected from the output inductor current. This circulating current results in excessive primary conduction losses, which become much more severe at high-power and low duty-cycle conditions. For the proposed converter, the primary circulating losses occur only during the primary side current resetting interval, as illustrated in Fig. 11(b), which is negligibly small compared to the half-switching period, so the primary circulating losses are minimized.

In traditional PSFB dc–dc converters, the ZVS of lagging-leg switches is achieved over a wider load range with larger values of leakage inductance or by adding an external series inductor. However, this extends the time required for the primary current to change direction from negative to positive, and vice versa, as shown in Fig. 11(a), which results in a loss of duty cycle on the secondary side of transformer and decreases the conversion efficiency. Normally, a higher turns ratio in the transformer is required to compensate the secondary-side duty-cycle loss. With a higher turns ratio, the reflected output current into the primary side is increased, which results in higher primary-side conduction losses. In addition, the higher turns ratio increases the voltage stress on the secondary-side bridge rectifier. This may necessitate the use of diodes with higher voltage ratings, which typically have higher conduction losses and poorer reverse recovery characteristics. In the proposed converter, the commutation interval, during which the primary current is increased from zero to the reflected output inductor current, can be greatly reduced with minimized leakage inductance. As a result, the duty cycle available to the secondary side is increased and a low turns ratio transformer can be utilized to reduced the voltage stress of the bridge rectifier.

C. Elimination of Voltage Overshoots Across the Rectifier Diodes and Minimal Achievable Voltage Stresses on the Rectifier Diodes

Since the resonant capacitor C_r and the diode D_r provide a clamping path to the output capacitor C_o for the bridge rectifier in the proposed converter, the voltage overshoots associated with the traditional PSFB dc–dc converter arising from the parasitic ringing of leakage inductance and junction capacitors of rectifier diodes are eliminated. Furthermore, the voltage stresses of the bridge rectifier diodes are clamped to

$$V_{\text{Rectifer\_diode}} = v_{Cr} + V_o. \tag{12}$$

The resonant capacitor voltage v_{Cr} of the proposed converter is composed of an average dc voltage V_{Cr} and a small amount of superimposed rippled voltageΔv_{Cr}. The average dc voltage V_{Cr} can be derived from the flux-balance condition on the leakage inductance L_{lk} during the active interval as

$$V_{Cr} \cong nV_{\text{in}} - V_o. \tag{13}$$

Substituting (13) into (12) yields

$$V_{\text{Rectifer\_diode}} \cong nV_{\text{in}}. \tag{14}$$

Equation (14) illustrates that the voltage stresses on the bridge rectifier diodes are nearly equal to the secondary-reflected input voltage independent of the duty cycle and the variations of the output voltage. This value is the minimal achievable voltage stress on the bridge rectifier for a full bridge dc–dc converter. This feature is very desirable in high-voltage electric vehicle battery charger applications, where wide duty cycle and output voltage range operations are normally required. Table I lists the voltage stresses across the rectifier diodes using different secondary clamping or passive energy recovery circuits. From Table I, we can see that the voltage stress on the bridge rectifier of the proposed converter is minimal for the prototype battery charger circuit and only the proposed converter can employ 600-V breakdown voltage diodes as bridge rectifier diodes.

In addition, the voltage stresses on the diodes D_o and D_r are also clamped to the output voltage and have a maximum voltage stress equal to 420 V.

TABLE I
V_R WITHOUT CONSIDERING AUXILIARY SNUBBERS

Topology	V_{Rmax} equation	V_{Rmax} for the prototype V_{bus}:400V, V_{bat}=250V-420V; n=34/29
[17]	$2nV_{in}-V_o$	$2nV_{in}-V_{bat\_min}=688V$
[18]	$nV_{in}+V_o$	$2nV_{in}-V_{bat\_max}=889V$
[19]	$3V_o/2$	$3V_{bat\_max}/2=630V$
[20]	$2V_o$	$2V_{bat\_max}=840V$
Proposed	nV_{in}	$nV_{in}=34\cdot 400/29=469V$

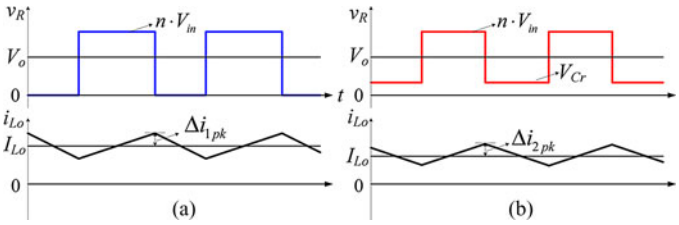

Fig. 12. Simplified rectified voltage waveforms of conventional PSFB converter and proposed HSPSFB dc–dc converter.

D. Reduced Filter Requirement

The output filter inductance can be reduced for the proposed converter with respect to the traditional PSFB converter because the resonant voltage v_{Cr} is applied to the output inductor L_o during the freewheeling intervals. The simplified rectified voltage waveforms of conventional PSFB converters and the proposed hybrid-switching ZVZCS converter are shown in Fig. 12. For conventional ZVS PSFB converters, the peak current ripple of output inductor can be expressed as

$$\Delta i_{1\mathrm{pk}}(M,V_o)=\frac{(1-M\cdot n)\cdot V_o\cdot\dfrac{T_s}{2}}{L_o} \tag{15}$$

where *M* is the dc conversion ratio and defined as $M=V_o/V_{\mathrm{in}}$.

For the proposed HSPSFB dc–dc converter, the peak current ripple of output inductor is given by

$$\Delta i_{2\mathrm{pk}}(M,V_o)=\frac{\left(\dfrac{1}{nM}-1\right)\cdot\left(2-\dfrac{1}{nM}\right)\cdot V_o\cdot\dfrac{T_s}{2}}{L_o}. \tag{16}$$

The current ripple ratio of the proposed converter to the traditional PSFB converter with the same filter inductance is obtained from (15) and (16)

$$R_{\mathrm{ripple}}=\frac{\Delta i_{2\mathrm{pk}}(M,V_o)}{\Delta i_{1\mathrm{pk}}(M,V_o)}=\frac{\left(\dfrac{1}{nM}-1\right)\cdot\left(2-\dfrac{1}{nM}\right)}{(1-M\cdot n)}. \tag{17}$$

The normalized peak current ripple of the traditional PSFB dc–dc converter, the proposed HSPSFB dc–dc converter, and the relationship of the current ripple ratio R_{ripple} versus the conversion ratio *M* is shown in Fig. 12. It can be seen from (17) and

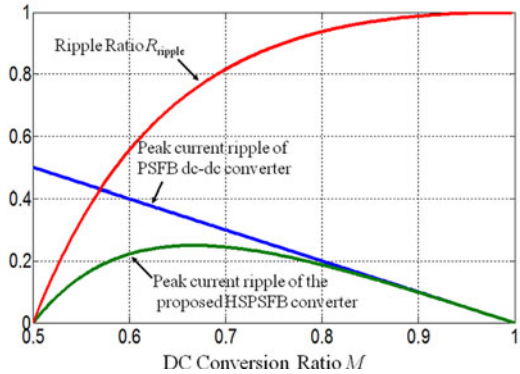

Fig. 13. Normalized peak current ripple of the traditional PSFB dc–dc converter, the proposed HSPSFB dc–dc converter, and current ripple ratio of proposed converter to traditional PSFB converters.

Fig. 13 that the output inductor current ripple can be reduced for the proposed converter compared to traditional ZVS-FSFB within a wide range of voltage conversion ratio. This means that the inductance can be reduced at the given output inductor current ripple condition, allowing compact output inductor size.

VI. DESIGN CONSIDERATIONS

A. Transformer Turns Ratio

According to the flux balance of the output inductor L_o and secondary rectifier waveform shown in Fig. 12(b), one can obtain

$$(nV_{\mathrm{in}}-V_o)D=(V_o-V_{Cr})(1-D). \tag{18}$$

Substituting (13) into (18) yields the conversion ratio of the proposed HSPSFB dc–dc converter

$$M_{\mathrm{HSPSFB}}=\frac{V_o}{V_{\mathrm{in}}}=\frac{n}{2-D}. \tag{19}$$

Equation (19) illustrates that the conversion ratio of the proposed converter varies between *n* (when $D=1$) *to n/2* (when $D=0$). Therefore, in order to satisfy the full ranges of battery voltage operation, *n* should chosen as

$$V_{\mathrm{bat\_max}}/V_{\mathrm{bus}}<n<2\cdot V_{\mathrm{bat\_min}}/V_{\mathrm{bus}}. \tag{20}$$

B. ZVS and ZCS Conditions

In order to achieve ZVS of the leading-leg switches, there is a dead time δt_1 requirement between S_1 and S_3 to allow time for the drain–source voltage to decrease to zero before the switch is turned ON [9]. The value of δt_1 can be determined from the following equation:

$$(C_{s1}+C_{s2})\cdot V_{\mathrm{in}}+C_{\mathrm{TR}}\cdot V_{\mathrm{in}}\le I_p\cdot\delta t_1 \tag{21}$$

where C_{TR} is the equivalent parasitic capacitance of the transformer, C_{s1} and C_{s2} are equivalent junction capacitors of the MOSFETs, and I_p is the primary side reflected current from the secondary side. In Mode 1 and Mode 2 operations, I_p is the primary-reflected peak current in the output inductor L_o, which is similar to that of traditional ZVS PSFB converters. In Mode 3

operation, I_p is the primary-reflected sum of the peak current in the output inductor L_o and the resonant current i_{Dr} through the diode D_r, which results in a wider ZVS range for the leading-leg switches than in traditional ZVS PSFB converters.

The basic requirement for achieving ZCS turn-off in the lagging-leg switches is to decrease primary current to zero within the freewheeling interval. For a well-designed circuit with all three operation modes, we only need to consider the ZCS requirement in Mode 1 operation since the freewheeling interval time is large enough to reset the primary current to zero before the turn OFF of the lagging-leg switches in Mode 2 and Mode 3.

According to the flux-balance of the output inductor, one obtains

$$V_{Cr} \cdot D_r + (nV_{\text{in}} - V_o) \cdot (D - D_r) = (1 - D) \cdot (V_o - V_{Cr}). \tag{22}$$

Substituting (19) into (22) and solving (22) yields

$$V_{Cr} = nV_{\text{in}} \cdot \left(\frac{1 - D_r}{2 - D} - (D - D_r) \right) \tag{23}$$

where D_r is the resonant duty cycle for Mode 1 operation and defined as

$$D_r = \frac{T_r}{2} / \frac{T_S}{2}. \tag{24}$$

The charge balance of the resonant capacitor C_r in the steady state requires that

$$I_{r\_\text{avg}} = (1 - D) \cdot I_{Lo} \tag{25}$$

where I_{r_avg} is the average resonant charge current through C_r in Stage 2 and I_{Lo} is the average current through the output inductor L_o.

The ripple voltage Δv_{Cr} on the resonant capacitor can be obtained as

$$\Delta v_{Cr} = \frac{I_{r\_\text{avg}} T_s / 2}{2C_r} = \frac{1}{4} \frac{1 - D}{2 - D} \frac{P_o T_s}{C_r V_o}. \tag{26}$$

From (11), the requirement for ZCS in the lagging leg switches is obtained as

$$\frac{n^2 I_{Lo} \cdot L_{\text{lk}}}{(V_{Cr} + \Delta v_{Cr})} \le (1 - D) \frac{T_s}{2}. \tag{27}$$

Substituting (23) and (26) into (27) yields

$$\frac{n^2 L_{\text{lk}} / R_o}{[(1 - D_r)(2 - D) - (2 - D)^2 (D - D_r)] + \dfrac{1 - D}{4} \dfrac{T_s}{R_o C_r}} \le (1 - D) \frac{T_s}{2} \tag{28}$$

where R_o is the equivalent load resistor. Equation (28) shows that reducing the leakage inductance can extend the ZCS operation range of the lagging leg switches and that the ZCS can be achieved relatively easily at light load.

C. Resonant Capacitor

As analyzed earlier, ZVS of the leading-leg switches of the proposed converter is easier to achieve than in traditional PSFB converters in Mode 3 operation. While in Mode 1 and Mode 2 operations, D_{r1} achieves ZCS turn-off, eliminating the diode reverse recovery induced losses. Therefore, the resonant period should be optimally selected as

$$\frac{T_r}{2} = \pi n \sqrt{L_{\text{lk}} C_r} = D_{\text{middle}} \cdot \frac{T_s}{2} \tag{29}$$

where D_{middle} is the duty cycle of PSFB dc–dc circuit when the output voltage is at the middle of the whole output voltage range.

Another consideration which should also be taken into account is that the resonant capacitor voltage v_{Cr} should not be discharged below zero anywhere within the operating range. If v_{Cr} was discharged below zero during the freewheeling intervals by the output inductor current, the ripple voltage Δv_{Cr} on the resonant capacitor C_r would be increased. This would cause higher voltage stresses on the rectifier diodes. In addition, if v_{Cr} was discharged below zero during the freewheeling intervals, the output inductor current would flow through the bridge rectifier with double fixed voltage drop of diodes, resulting in higher conduction losses. To ensure the resonant capacitor voltage v_{Cr} higher than zero anywhere within the operating range, the following equation must be satisfied:

$$\Delta v_{Cr} < V_{Cr}. \tag{30}$$

Substituting (13) and (26) into (30) yields

$$C_r > \frac{(2 - D) P_o}{8 n^2 V_{\text{in}}^2 f_s}. \tag{31}$$

TABLE II
OPERATION CONDITION AND CIRCUIT PARAMETERS OF THE PROTOTYPE CIRCUIT

Input voltage	400 V
Output voltage	250 V- 420 V
Output power	3.6 kW
Operating frequency	41.67 KHz
S_1, S_3	FCA76N60N
S_2, S_4	IRGP4063D
D_{o1}, D_{o2},D_{o3},D_{o4}, D_{r1},D_{r2}	HFA50PA60C
C_r	Polypropylene film capacitor, 0.47uF
L_o	370uH
C_o	2×22uF
Transformer Core	2×Ferrite EE80
Transformer Turns Ratio	29:34
L_m	10.5mH
L_{lk}	8.9uH

VII. EXPERIMENTAL RESULTS

A 41.67-kHz, 3.6-kW prototype circuit has been built and tested to verify the operation principles and the performance of the proposed HSPSFB dc–dc converter. A digital control board with Texas Instrument's 28335 DSP is employed as the controller. Table II lists the operating conditions and circuit parameters of the prototype circuit. According to (29), the resonant frequency of the hybrid-switching circuit f_r is equal to 66 kHz and $D_{\text{middle}} = 0.63$. In addition, the (31) requires that the

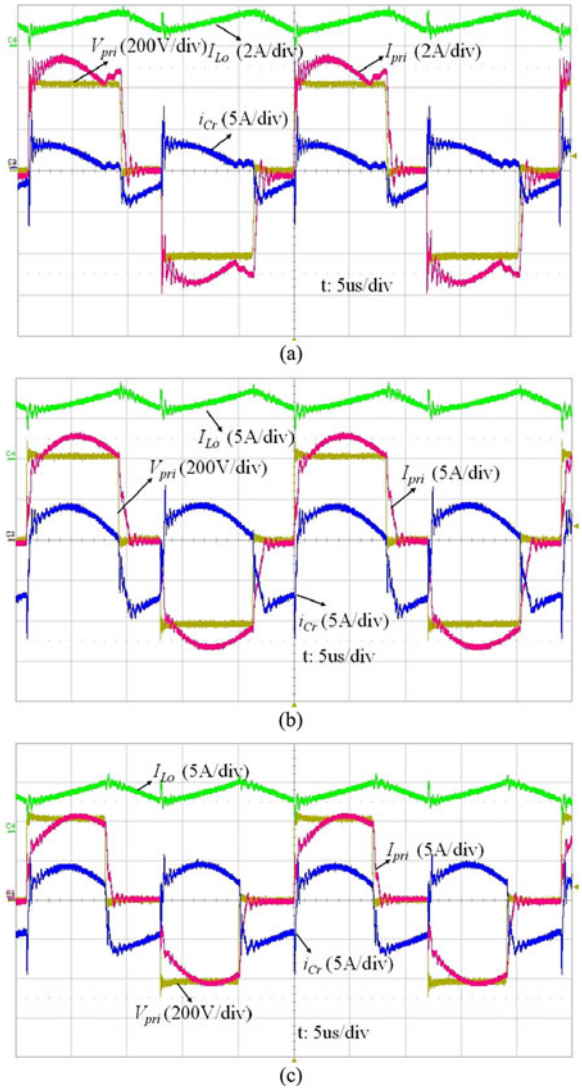

Fig. 14. Experimental waveforms for three different operation modes: (a) Mode 1: $V_{\rm in} = 400$ V, $V_o = 360$ V, $P_o = 1.3$ kW; (b) Mode 2: $V_{\rm in} = 400$ V, $V_o = 330$ V, $P_o = 3.1$ kW; and (c) Mode 3: $V_{\rm in} = 400$ V, $V_o = 300$ V, $P_o = 2.2$ kW.

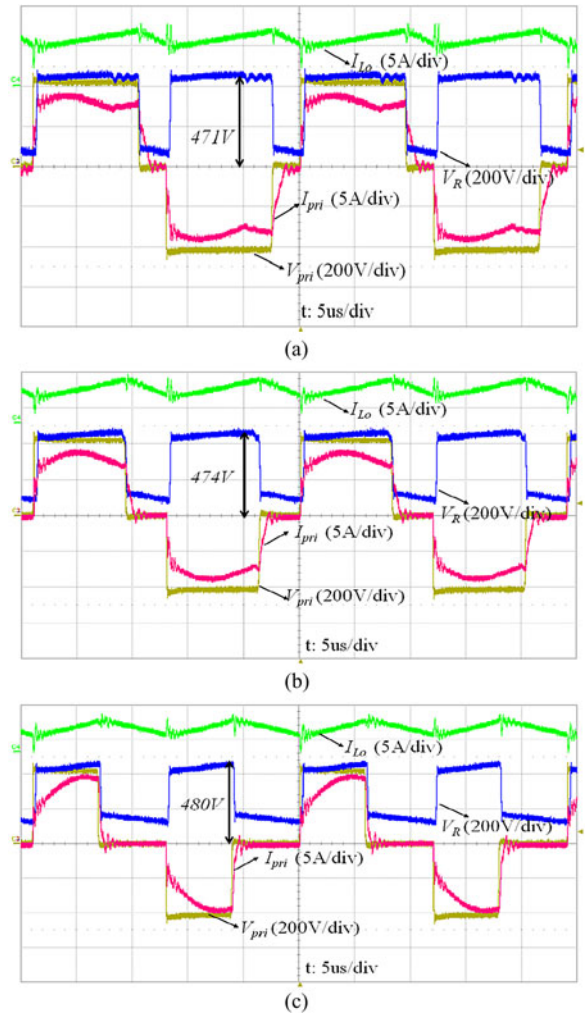

Fig. 15. Experimental waveforms demonstrating the secondary-side rectifier output voltage V_R: (a) Mode1, (b) Mode 2, and (c) Mode 3 operations.

resonant capacitor C_r is larger than 0.1 μF. The selected capacitor for the prototype circuit is 0.47 μF, which is larger than 0.1 μF and satisfies (31).

Fig. 14 illustrates the key waveforms of the output inductor current i_{Lo}, transformer primary side voltage $v_{\rm pri}$, transformer primary current $i_{\rm pri}$, and resonant capacitor current i_{Cr} for three different operating modes. As expected, the primary current $i_{\rm pri}$ is combined with hybrid linear PWM current and sinusoidal resonant current and in phase with the primary voltage achieving minimized circulating conduction loss. The resonant capacitor C_r is charged by resonant sinusoidal current during the powering intervals and discharged by linear PWM current during the freewheeling intervals. The primary side circulating current is reduced to zero within 1 μS for all three cases and the lagging-leg switches are turned OFF near ZCS; only the magnetizing current flows when the switches turn OFF. The current ripple of the output inductor is minimized.

Fig. 15 shows the secondary rectified output voltage V_R for three operating modes. The ideal rectified voltage is $\mathrm{n}V_{\rm in} = (34/29) \cdot 400 = 469$ V. For the test cases of the three operation modes, the maximum rectifier voltages are 471, 474, and 480 V, respectively, which shows that the voltage stresses on the rectifier diodes close to the ideal calculated value and without any overvoltage stresses for all operation conditions.

Fig. 16 highlights the ZVS operation of leading-leg switches and ZCS operation of lagging-leg switches.

The measured efficiency curves of the power stage for three output voltages 250, 360, and 420 V over the wide load range from 160 W to 3.6 kW are shown in the Fig. 17. The maximum efficiency 98.1% is achieved at an output voltage of 420 V and 3.6 kW load condition. System efficiency is high over wide output power ranges. The proposed converter is essentially a buck-type converter. When the output voltage is higher, the duty is higher, which means the period of energy transfer from the input to the output is longer. Accordingly, the efficiency is higher, which can be illustrated by the measured efficiency curves in Fig. 17.

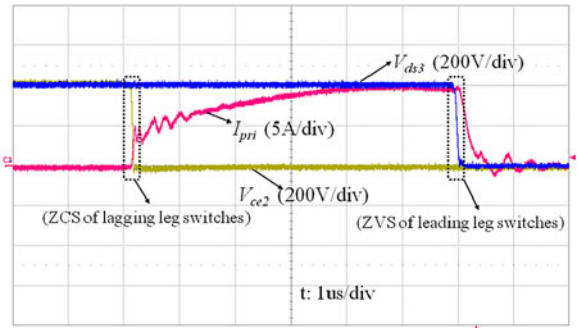

Fig. 16. ZVS for leading-leg switches and ZCS for legging-leg switches.

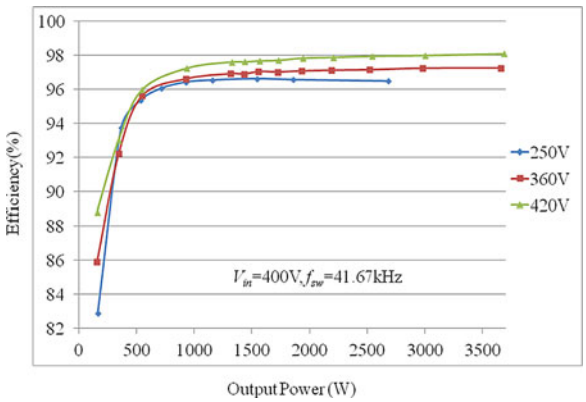

Fig. 17. Measured efficiencies.

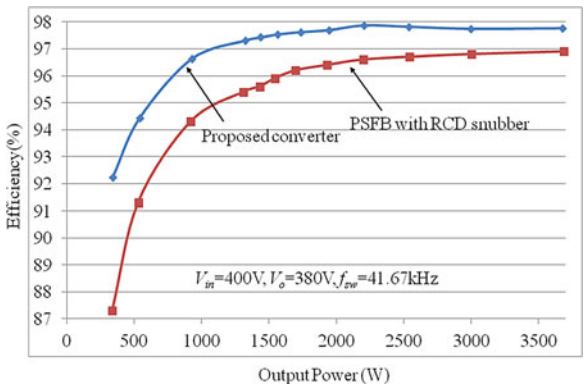

Fig. 18. Efficiency curves for proposed converter and traditional PSFB dc–dc converter with RCD snubber.

The comparative efficiency curves for the proposed converter and a traditional ZVS PSFB dc–dc converter with an RCD snubber are given in Fig. 18 for a 380-V output voltage. The efficiency of the proposed converter is higher than that of the traditional ZVS PSFB dc–dc converter with RCD snubber over wide ranges of output power.

VIII. Conclusion

This paper first presents a hybrid-switching step-down dc–dc converter, and then, by introducing transformer isolation, a novel high-efficiency hybrid-switching full-bridge dc–dc converter is presented for electric vehicle chargers. The distinctive characteristics of the proposed HSPSFB dc–dc converter are summarized as follows:

1) ZVS turn-on of the leading-leg switches can be achieved over a wide load range.
2) As a result of resonant capacitor voltage resetting the primary side current to zero at the beginning of the freewheeling intervals, the lagging-leg switches achieve ZCS turn-off and primary circulating current losses are avoided.
3) Energy is transferred to the output with a combined resonant power conversion mode and PWM power conversion mode during the powering stages; in the freewheeling stages, the capacitive energy and inductive energy are transferred to the output simultaneously with only one diode voltage drop in the current path. Hence, more effective and efficient energy transfer can be achieved.
4) The resonant capacitor voltage is applied to the output inductor during the freewheeling states. As a result, the output filter inductance can be reduced and a more compact inductor can be used compared to traditional PSFB converters.
5) The voltage stresses of the secondary bridge rectifier diodes are close to the ideal transformer secondary reflected voltage $nV_{\rm in}$ without a danger of overvoltage. This is due to the clamping feature of the secondary resonant circuit.
6) Experimental results based on the designed 3.6-kW prototype circuit show 98.1% peak efficiency and high efficiency over a wide output voltage and power range. Due to its simple structure, high efficiency, and high reliability, the proposed converter is a very attractive design for electric vehicle battery chargers.

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Dr. Lai has chaired the 2000 IEEE Workshop on Computers in Power Electronics, 2001 IEEE/DOE Future Energy Challenge, and 2005 IEEE Applied Power Electronics Conference and Exposition. His work has resulted in several distinctive awards including a Technical Achievement Award at Lockheed Martin Award Night, two IEEE IAS Conference Paper Awards, and Best Paper Awards from IEEE International Conference on Industrial Electronics, Control and Instrumentation, 1997, International Power Engineering Conference 2005, and Power Conversion Conference 2007.

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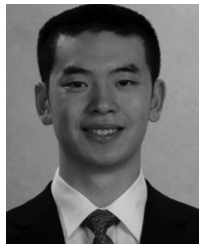

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