Nanodiamond Vacuum Field Emission Integrated Differential Amplifier

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***Abstract*—The development of a novel vacuum differential amplifier (diff-amp) array employing vertically configured nanodiamond (ND) vacuum field emission transistors (ND-VFETs) on a single chip is presented. The diff-amp array is composed of a common ND emitter array integrated with partition gates and split anodes. An identical pair of ND-VFETs with well-matched field emission transistor characteristics was fabricated by using a dual-mask well-controlled microfabrication process, involving a mold-transfer self-aligned gate–emitter technique in conjunction with ND deposition into the micropatterned molds in the active layer of a silicon-on-insulator substrate followed by gate partitioning to form diff-amp array. The ND-VFETs show gate-controlled modulation of emission with distinct cutoff, linear, and saturation regions. Signal amplification characteristics of the ND-VFET diff-amp are presented. A large common-mode-rejection ratio (CMRR) of 54.6 dB was measured for the diff-amp. The variation of CMRR performance with transconductance was examined, and the results were found to agree with the equivalent circuit model analysis. The accomplishment of this basic circuit building block, consisting of an integrated diff-amp, demonstrates the feasibility of using vacuum integrated circuits for practical applications, including high-radiation and temperature-tolerant space electronics.**

***Index Terms*—Differential amplifier (diff-amp), integrated circuits (ICs), nanodiamond (ND), transistor, vacuum field emission (VFE).**

I. Introduction

VACUUM FIELD EMISSION (VFE) microelectronics, relying on ballistic electron transport in vacuum, promises for high operation speed, low energy loss, and temperature and radiation immunity performance [1], [2]. Vacuum microelectronic devices are favorable for a variety of applications ranging from sensors and field emission displays to high-performance integrated circuits (ICs). VFE devices possess better noise immunity than solid-state devices and thereby can operate at a much lower current with good noise rejection performance. VFE integrated devices and circuits are good for high-speed and high-power applications and in harsh environments including high temperature and high radiation. In the past, only few practical implementations of VFE devices at circuit level have been reported even though the concepts and modeling of vacuum ICs were described [3], [4]. Improvement in VFE device stability, particularly cathode reliability, is required for the practical implementation of vacuum microelectronic devices in ICs.

Recent development of carbon-derived materials such as nanodiamond (ND) film and carbon nanotubes has revealed their superior electron field emission characteristics [5]–[16]. ND possesses the unique properties of low electron affinity, thermal stability, and mechanical hardness, making it a robust cathode material for VFE devices [6], [7]. In addition, n-type conductivity can be achieved by *in situ* nitrogen doping in chemical-vapor-deposited (CVD) ND film, concomitantly providing a deliberate amount of sp^2 graphitic inclusion in the sp^3 diamond matrix with enhanced electron emission characteristics [8], [9]. Moreover, the small grain size and smooth surface morphology of ND allow compatible integration with silicon microfabrication and thus further facilitate the development of vacuum microelectronics via the mold-transfer self-aligned gate–emitter technique [17].

VFE transistors (VFETs) utilizing CVD ND as the emitters with low threshold voltage, stable emission current, and high voltage gain have been reported [10]–[12], allowing their further implementations into vacuum ICs and logic gates. A realistic approach to demonstrate IC capability is the implementation of a differential amplifier (diff-amp), which is known to be the most important circuit building block used in analog and mixed-signal circuits of solid-state microelectronics. For instance, the input stage of an operational amplifier and the basic element of emitter-coupled high-speed logic [18], [19] incorporate the diff-amp. Our group created a VFE diff-amp based on carbon-nanotube emitters in 2009 [16]. Recently, we have developed highly reliable nitrogen-incorporated ND cathodes for VFE devices [9]–[15] and have considered their deployment in vacuum ICs [20]. In this paper, the fabrication processes, dc field emission, and ac amplification characteristics of an ND-VFET diff-amp are presented. The advantage of better noise rejection was demonstrated by choosing to operate the device at low current. The device performance including the common-mode-rejection ratio (CMRR), an important figure of merit for diff-amp, has been evaluated by experimental measurement. The

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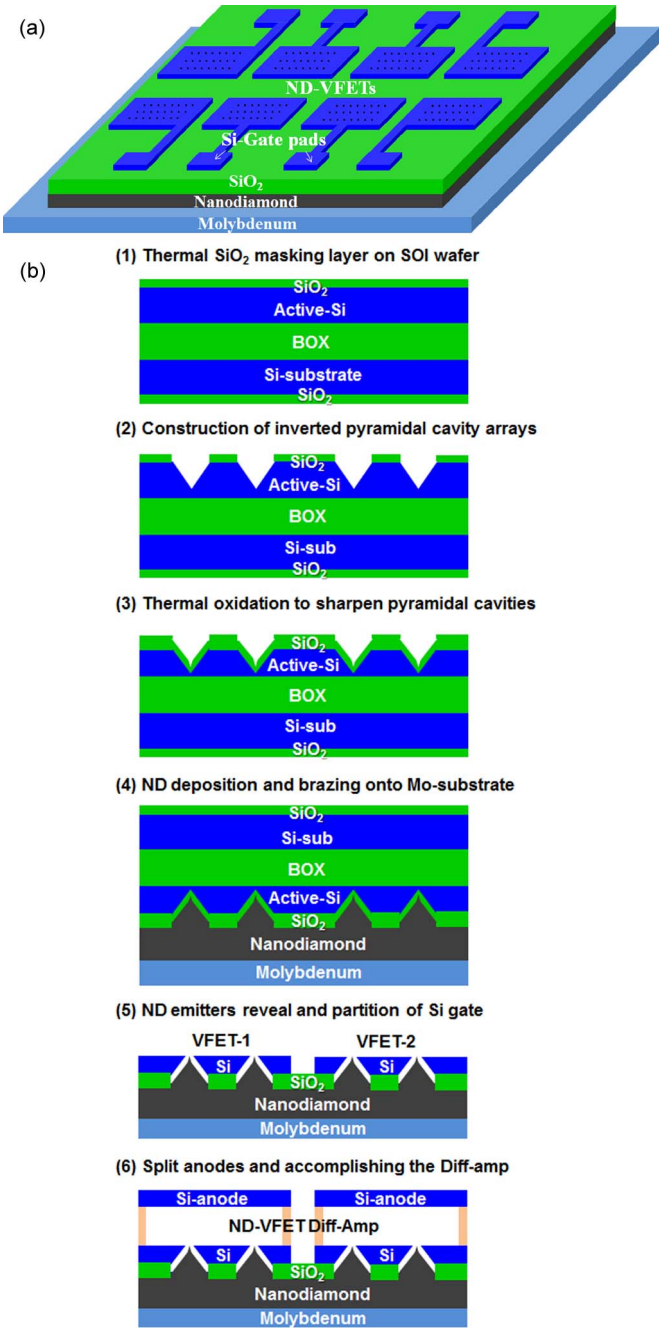

Fig. 1. (a) Schematic diagram of the ND-VFET diff-amp array chip with separate contact pads. The chip is brazed onto a Mo substrate. (b) Fabrication flowchart of the ND-VFET diff-amp.

equivalent circuit analysis based on dc characteristics has also been performed to analyze the CMRR value. The successful implementation of the ND-VFET diff-amp demonstrates the feasibility of using vacuum ICs as an alternative electronic circuit for harsh environment operation.

II. Fabrication of ND Vacuum Diff-Amp

Fig. 1 shows the schematic layout and fabrication scheme of the ND-VFET diff-amps on a chip. The IC chip consisting of an array of ND-VFETs, each has 80 × 80 ND emitter tips, was fabricated by a simple dual-mask photolithography process on a silicon-on-insulator (SOI) substrate using a mold-transfer self-aligned gate–emitter technique. The high-conductivity active silicon layer of the SOI was used as the mold as well as the gate layer. Inverted pyramidal molds were first constructed on the active silicon layer by photolithography patterning followed by silicon anisotropic wet etching [17]. The resulting mold layer was later used in the self-aligned gate structure. Next, a 1-μm-thick SiO_2 was thermally grown on the inverted silicon pyramidal mold cavities to form the dielectric isolation between the gate and emitter electrodes and simultaneously produce an ultrasharp apex at the inverted pyramidal mold tips as the deposited ND conforms to achieve the tips or the emitters. Subsequently, nitrogen-incorporated ND was deposited into and on the molds by plasma-enhanced chemical vapor deposition using a gas mixture of $CH_4/H_2/N_2$, automatically self-aligning the ND emitters to the silicon gate. The ND-filled mold was then coated with a composite layer of sputtered titanium and nickel to form the back contact and brazed onto a molybdenum substrate using a titanium–copper–silver (ticusil) brazing alloy. The Ti/Ni bilayer provided strong metallurgical adhesion with ND and facilitated the brazing of diamond onto the Mo substrate, while the ticusil layer provided good metal contact between ND and Mo substrate after being melted at 900 °C in vacuum of 10^{-7} torr and solidified upon cooling. After etch removal of the silicon substrate and the buried oxide layer of the SOI, ultrasharp ND pyramidal cathodes with self-aligned Si gates were revealed by a thin down process of the active silicon layer in a HF/HNO_3 (1 : 30 volume ratio) mixture followed by partial etch of the thermal SiO_2 around the ND tips. This silicon thin down process was well controlled, providing uniform gate openings and the optimized proximity of gate to emitters. Then, a second lithographic patterning and silicon reactive ion etching was executed to partition the Si gate and form individual ND-VFETs with separate contact pads for diff-amp implementation. Finally, the diff-amp was realized by mounting two highly conductive silicon anodes adjacently and above a selected pair of identical ND-VFETs forming a split anode with 600-μm spacing above the gate electrodes.

The fabricated adjacent ND-VFETs examined under scanning electron microscope (SEM) are shown in Fig. 2(a). Fig. 2(b) shows part of the ND-VFET and higher magnifications. A single ND cathode with an ultrasharp apex and a self-aligned Si gate surrounding it is displayed in the inset. When examined under high magnification, the ND-VFET exhibited similar gate-to-cathode spacing of ∼1 μm and uniform ND tip sharpness, with more than 90% yield. Uniform gate-to-cathode spacing with well-formed ND cathodes is crucial to acquiring an identical transistor pair with well-matched electrical characteristics for practical diff-amp implementation.

III. Characterization and Modeling of Diff-Amp

Fig. 3 shows the schematic test setup for characterizing the ND-VFET diff-amps. The fabricated ND-VFE devices on the chip were placed in a vacuum chamber maintained at 10^{-7} torr and tested separately for dc field emission in order to evaluate the matching transistor pair's characteristics. For each ND-VFET, positive gate voltage (V_g) was applied on the gate

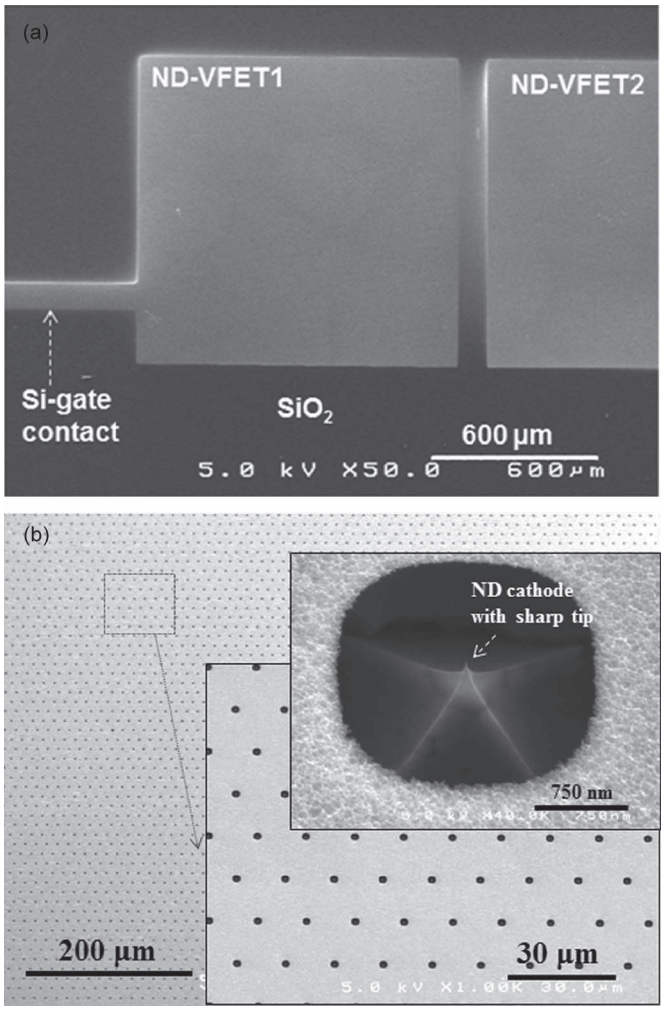

Fig. 2. (a) Top-viewed SEM image of a pair of ND-VFETs. (b) SEM micrographs showing part of the ND-VFET. Insets show higher magnification and a single ND cathode with self-aligned Si gate.

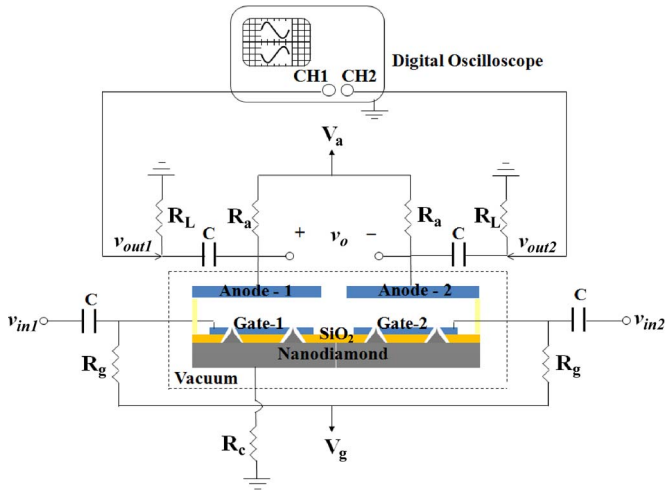

Fig. 3. Schematic diagram of the testing circuitry for the ND-VFET diff-amp in common–emitter configuration. DC bias voltages were applied to operate the pair of transistors in saturation mode. AC input small signals were applied through coupling capacitors to gate electrodes, while output voltages are collected at anode electrodes.

electrode with a given anode voltage (V_a) such that electrons induced from cathodes by V_g were gathered by anode electrodes. The anode and gate currents (I_a and I_g) were measured as a function of V_g by a downward voltage sweep method to characterize each transistor pair in the saturation mode. Two ND-VFETs with nearly identical field emission features were then utilized for diff-amp ac testing.

The ac signal amplification of the ND-VFET diff-amp was examined by feeding input signals to the gate electrodes and recording the output signals at the anode electrodes of the transistors, biased at a predetermined operating point in the saturation region [12], as shown by the schematic diagram in Fig. 3. We defined the input and output voltages of ND-VFETs to be $v_{\rm in1}$ and $v_{\rm out1}$ for transistor 1 and $v_{\rm in2}$ and $v_{\rm out2}$ for transistor 2.

For common-mode operation, both ND-VFETs amplified the same input sinusoidal signals and created a differential output voltage between anode electrodes. The input and output voltages of the diff-amp in common mode are denoted by $v_{\rm ic}$ and $v_{\rm oc}$, respectively, where $v_{\rm ic}$ is equal to $v_{\rm in1}$ and $v_{\rm in2}$ whereas $v_{\rm oc}$ is equal to $v_{\rm out1} - v_{\rm out2}$. Thus, the common-mode voltage gain $A_{\rm cm}$ is equal to $v_{\rm oc}/v_{\rm ic}$. Using the equivalent circuit analysis [18], [21], it can be expressed as

$$A_{\rm cm} = \frac{(I_{a1} - I_{a2}) \times (R_a // R_L)}{v_{\rm ic}} = \frac{\Delta I_a}{V_{\rm ic}} \times (R_a // R_L) \quad (1)$$

where R_a is the anode resistance, R_L is the load resistance, and ΔI_a is the mismatch value of anode emission currents.

For differential-mode measurement, the sinusoidal small signal was first applied only to the gate electrode of transistor 1 of the diff-amp, while no signal was fed to the gate terminal of transistor 2 to achieve a half-circuit differential input, i.e., $v_{\rm in1} = V_p \sin(2\pi f t)$ V, where V_p and f are the amplitude and frequency of the input signal, and $v_{\rm in2} = 0$ V. The differential input and output voltages ($v_{\rm id} = v_{\rm in1} - v_{\rm in2}$ and $v_{\rm od} = v_{\rm out1} - v_{\rm out2}$) were then equal to the input and output voltages of transistor 1 since there was no signal amplified by transistor 2, i.e., $v_{\rm id} = v_{\rm in1}$ and $v_{\rm od} = v_{\rm out1}$. Therefore, the half-circuit differential-mode voltage gain $A_{\rm dm1}$ of the diff-amp is equal to the voltage gain of the transistor 1 [18], [21] which can be described as

$$A_{\rm dm1} = \frac{v_{\rm out1}}{v_{\rm in1}} = \frac{I_{a1} \times (R_a // R_L)}{V_{\rm in1}} = g_{m1} \times (R_a // R_L). \quad (2)$$

In this analysis, the internal parasitic capacitances were ignored since we examine low-frequency response to demonstrate the operation of ND-VFE diff-amp, and the coupling capacitors were chosen to be at the microfarad level such that their reactance was negligible.

Next, the same procedures were employed on transistor 2 with no signal applied on transistor 1. Similar differential-mode voltage gain $A_{\rm dm2}$ can be obtained from (2), but it will be 180° out of phase.

Finally, the value of CMRR was determined by $\text{CMRR} = |A_{\rm dm}/A_{\rm cm}|$. This value was utilized to evaluate the ability of a diff-amp to reject input noise common to both input terminals,

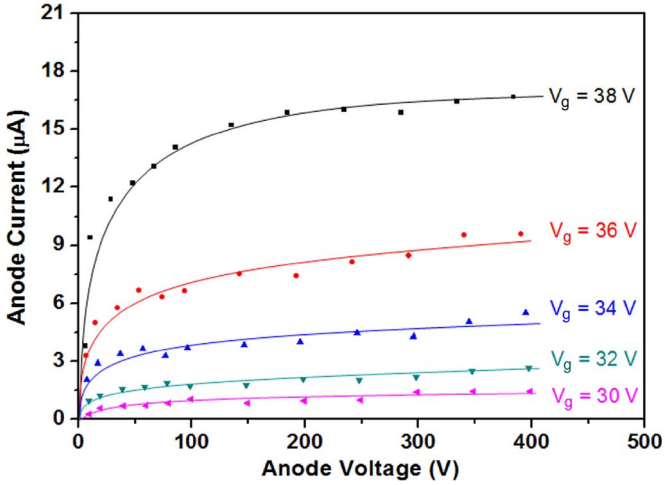

Fig. 4. Plots of the anode current versus anode voltage of the fabricated ND-VFET at various gate voltages, showing clear transistor characteristics with distinct cutoff, linear, and saturation regions.

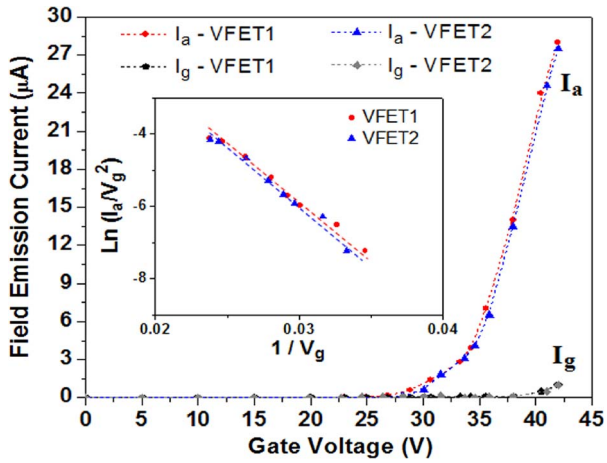

Fig. 5. DC field emission characteristics of an ND-VFET pair used for diff-amp at fixed $V_a = 350$ V exhibit well-matched anode currents as a function of gate voltage with negligible gate currents. (Inset) F–N plots of the corresponding I_a–V_g data.

particularly important when the signal of interest is contained in the voltage difference of inputs. Larger g_m and smaller ΔI_a obviously would enhance the CMRR of a diff-amp.

The transconductance (g_m) of the ND-VFET, defining the variation of I_a with the change of V_g at fixed V_a bias, was determined from the dc characteristics as described by

$$g_m = \left.\frac{\partial I_a}{\partial V_g}\right|_{va=\text{const}}. \tag{3}$$

The g_m determines the current driving capability and voltage gain of the transistor. It also plays an important role in diff-amp performance since the differential-mode voltage gain is determined by the voltage gain of a single transistor which is governed by g_m.

IV. Electrical Performance of Diff-Amp

Fig. 4 shows a family of I_a–V_a–V_g transistor characteristics of an ND-VFET, where distinct cutoff, linear, and saturation regions are observed. The anode current increased with anode voltage as V_a was less than 100 V and saturated at V_a above ~100 V for a fixed gate bias. This feature is consistent with the electron transport mechanism discussed previously [12]. The device exhibited a high amplification factor of ~215 at a constant anode current of ~9.5 μA, demonstrating a high dc voltage gain appropriate for amplifier applications. The relatively low current, compared to that in diode configuration [9], is due to the gate screening effect and the significant decrease in geometrical field enhancement factor attributed to the triode's construction. Nevertheless, higher I_a can be achieved at higher gate voltages.

The electron field emission characteristics of ND-VFETs were measured and compared in order to find a close-matched transistor pair for diff-amp testing. Fig. 5 shows the I_a–V_g curves of the VFET pair, operated in the saturation region at $V_a = 350$ V, along with corresponding gate currents. The exponential increase features of anode currents with the gate voltage are indicative of the gate-induced field emission nature, obeying the Fowler–Nordheim (F–N) equation [22]

$$I = \frac{k_1 A \beta^2 V_g^2}{\phi d^2} \exp\left[\frac{-k_2 \phi^{1.5} d}{\beta V_g}\right] \tag{4}$$

where k_1 and k_2 are constants, A is the emitting area, β is the field enhancement factor, Φ is the work function of the emitting surface, and d is the gate-to-emitter spacing.

In addition, the linearly negative slope of $\ln(I_a/V_g^2)$-versus-$1/V_g$ plots extracted from the corresponding I_a–V_g data, as shown in the inset, is consistent with the F–N relationship in (4), further confirming that the anode currents are due to the field-enhanced emission behavior. These two VFETs possessed well-matched emission anode currents up to ~28 μA at V_g of 42 V with a mismatch of 1.2% and fairly low gate turn-on voltages, defined as the voltage required to draw 1-μA emission current, of ~29 and ~30 V, respectively. Such nearly identical characteristics of the transistor pair would provide useful common-mode-rejection performance in the diff-amp. The VFETs also exhibited negligible gate intercepted currents, ~3.5% of I_a, suggesting the long-term operation capability and stability of the diff-amp.

Based on the recorded I_a–V_g values, the g_m was computed and plotted as a function of V_g at fixed $V_a = 350$ V, as shown in Fig. 6. The exponentially increasing trend was observed in the g_m-versus-V_g plot, demonstrating that the anode emission current was strongly affected by the gate voltage, governed by [23], [24]

$$g_m = \frac{k_1 A \beta}{\phi d}\left(\frac{2\beta}{d} V_g + k_2 \phi^{1.5}\right) \exp\left[-\frac{k2\phi^{1.5} d}{\beta V_g}\right]. \tag{5}$$

The g_m was determined to be ~4 μS at $V_g = 42$ V, a reasonable choice for our diff-amp operation, and the value agrees with our previous results obtained from another ND-VFET at the same anode current [12]. Higher g_m is expected at higher operation voltages and currents due to the exponential relationship between g_m and V_g. Furthermore, the emission current driving ability by gate voltage of VFETs will

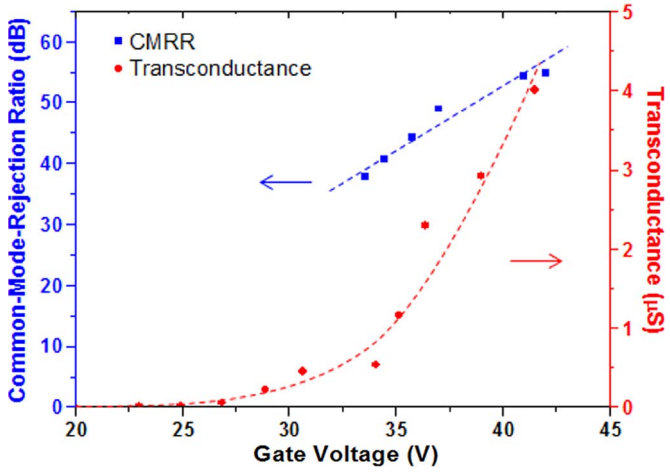

Fig. 6. Plots of the transconductance and measured CMRR versus the gate voltage of the fabricated ND-VFET pair at a given anode voltage (V_a = 350 V).

be further improved by employing a smaller gate-to-cathode distance. The effect of g_m on common-mode-rejection performance of the diff-amp will be discussed later in this section.

After acquiring dc characteristics, the ac signal amplification performance of the ND-VFET diff-amp was measured at a predetermined operation point in the saturation region. An ac sinusoidal input signal with an amplitude of 0.5 V at 100 Hz was superimposed on $V_g = 42$ V at the gate terminals, and the amplified output signals were recorded across the load resistors $R_a//R_L$ (10 MΩ each) at the anode electrodes by a digital oscilloscope. The differential output voltage $(v_{\text{out1}} - v_{\text{out2}})$ was obtained by using the built-in math function of the digital oscilloscope. In the common-mode test, the same small signals, as shown in Fig. 7(a), were applied to both of the inputs, and the signals were amplified to 15.0 and 15.2 V at outputs 1 and 2, respectively, as shown in Fig. 7(b), resulting in a small peak-to-peak common-mode output voltage v_{oc} of ∼1.1 V and a calculated A_{cm} of ∼0.0256, based on (1).

On the other hand, in the differential-mode tests, the small signal was first imposed on the first input of the diff-amp, while no signal was applied to the other input, i.e., $v_{\text{in1}} = 0.5\ \sin(2\pi ft)$ V and $v_{\text{in2}} = 0\ \sin(2\pi ft)$ V. Fig. 7(c) shows the corresponding output waveforms with a differential output voltage v_{od1} of ∼13.8 V, giving a proper voltage gain at the operating current of 28 μA. Similarly, by alternating the input sequence, the output waveform of transistor 2 v_{out2} and the corresponding differential output signal v_{od2} with an ∼13.8-V peak-to-peak value and a 180° phase shift are shown in Fig. 7(d) as the input signal amplified only by the second transistor. The A_{dm} was computed to be ∼13.8 which is equivalent to the voltage gain of a single-ended transistor amplifier. Then, the CMRR of the ND-VFET diff-amp was determined to be ∼540 (54.6 dB), demonstrating the feasibility for vacuum IC implementation. Relatively less noise was observed on v_{od1} and v_{od2} waveforms compared to v_{oc}, implying that the noise common to both input terminals was offset in the differential-mode outputs, a basic and required feature of a diff-amp. Note that a doubled CMRR of ∼1080 (60.7 dB) can be obtained under the condition of fully differential signals applied to the input terminals. This

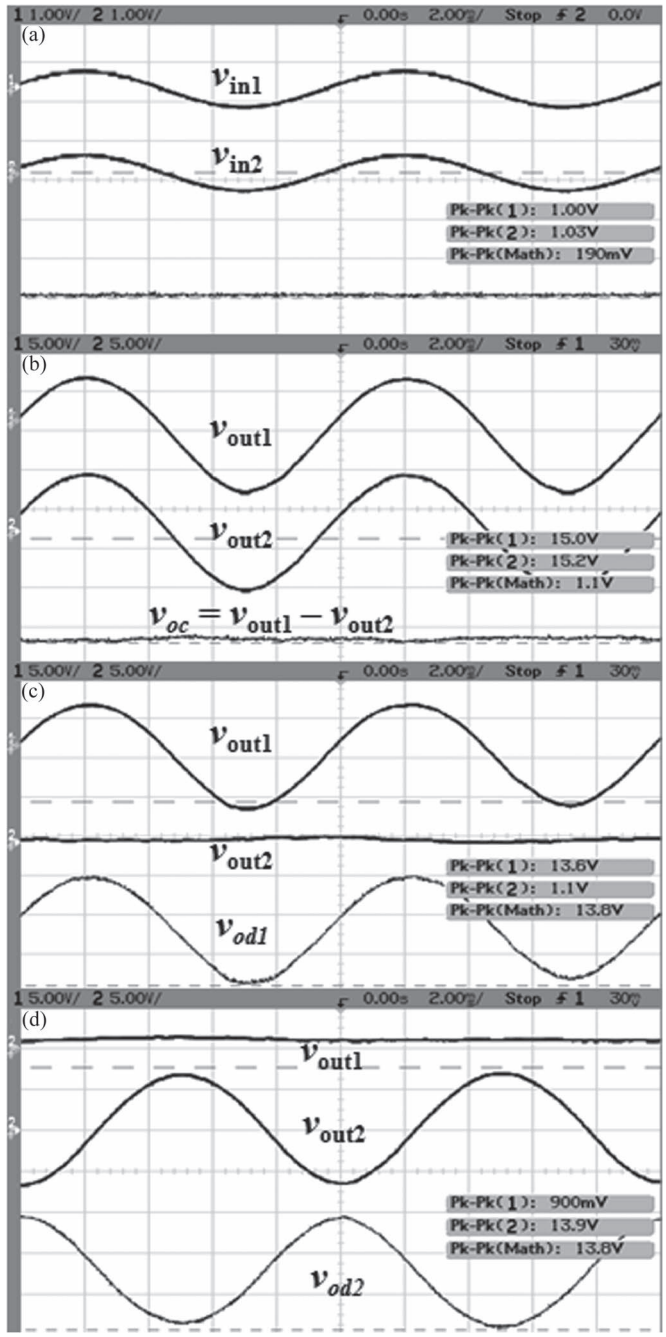

Fig. 7. AC characteristics of the single-chip ND-VFET diff-amp: (a) Input signals to both gate terminals in common mode, (b) common-mode output signals recorded at both anode electrodes, (c) first differential-mode output waveforms, and (d) second differential-mode output waveforms with 180° phase shift.

value is comparable to that of the commercially available solid-state diff-amps which are well known to have limited operating temperature range [25]. Therefore, the fabricated ND-VFET diff-amp can be an alternative IC building block providing good common-mode-rejection performance with capability for harsh environment operation [13]–[15].

The ac measurement procedures were then repeated on the ND-VFET diff-amp for variant operation points, and the corresponding CMRR is plotted as a function of V_g, as shown in Fig. 6. The enhancement of CMRR with V_g from ∼37.9 dB at

33.5 V to ∼54.6 dB at 42 V was observed, which is attributed to the increase of the g_m and transistor voltage gain, agreeing with the prediction of equivalent circuit analysis where

$$\mathrm{CMRR} = \frac{v_{\mathrm{ic}} g_m}{\Delta I_a}. \tag{6}$$

The CMRR in decibels increased linearly with the gate voltage because g_m is an exponential function of V_g as indicated in (5). The further improvement of common-mode rejection is potentially achievable by the improvement of the transconductance described earlier in this section and by minimizing the anode current mismatch. The high-frequency response of the ND-VFET diff-amp will be explored in the future with optimum device structure and better test setup.

Equations (1) and (2) were utilized to estimate the common-mode and differential-mode voltage gains of the ND-VFET diff-amp. In this experiment, the diff-amp was operated at $V_g =$ 42 V with an ac input voltage amplitude of 0.5 V for R_a and R_L of 10 MΩ each. The A_{cm} and A_{dm} were calculated to be 0.039 and 20, respectively, giving an estimated CMRR of 513 (54.2 dB) which is consistent with the experimentally measured result. The slight overestimations of both A_{cm} and A_{dm} in the analysis model were observed, which are probably due to the neglect of the noninfinite output resistance looking into the anode. Nevertheless, the estimation of CMRR is reliable since the CMRR is independent of load and output resistances, providing a simple method to evaluate the common-mode-rejection performance of the VFE diff-amp.

V. Conclusion

A basic circuit building block of ND-VFET diff-amp for vacuum IC has been developed and implemented. A dual-mask microfabrication process involving the mold-transfer self-aligned gate–emitter technique coupled with ND deposition and gate partitioning has been employed for the fabrication of the ND-VFET pairs on a chip. The ND-VFET pair showed well-matched field emission transistor characteristics with low gate turn-on voltage and negligible gate intercepted current. A large CMRR of ∼540 (54.6 dB), which is consistent with the estimated value in the analysis model, was realized at an operating gate voltage of 42 V with a transconductance of 4 μS. The enhancement of CMRR with increasing gate voltage as well as transconductance was observed, agreeing with the equivalent circuit analysis and suggesting that higher CMRR is achievable at higher operation voltage. The successful implementation of this basic circuit building block, consisting of an integrated VFET diff-amp, demonstrates the feasibility of using vacuum-based ICs for practical applications, including high-speed and temperature- and radiation-hardened electronics.

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