

RF Characteristics of 0.18- μm CMOS Transistors

Kwangseok HAN,* Jeong-hu HAN, Minkyu JE and Hyungcheol SHIN

*Department of Electrical Engineering and Computer Science,
Korea Advanced Institute of Science and Technology, Taejeon 305-701*

(Received 11 February 2001)

In this work, the high-frequency performance of a 0.18- μm CMOS device has been analyzed with various multi-finger layouts and biases to find the optimal condition. The optimal bias condition to maximize the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) have been found to be equal to that required to maximize the transconductance (g_m). At this bias condition, f_T tends to be maximized with a small number of fingers. **It has been found that f_{max} strongly depends on the gate resistance.** Finally, the de-embedding effects on cutoff frequency are presented.

PACS numbers: 85.30.De

I. INTRODUCTION

The strongly emerging wireless communication market needs device technologies that are capable of producing high product volumes at extremely low cost [1]. III-V compound semiconductor devices, which include MESFET's, HEMT's, and HBT's, have been used in microwave electronic circuits because of good high-frequency performance [2]. However, these devices are limited to a specific area due to high fabrication cost. On the other hand, due to the continuous reduction of minimum channel length in CMOS technologies, CMOSs have become candidates for RF applications. By using CMOS devices in IF and RF modules in wireless communication systems, we can integrate the system in a single chip. Consequently, substantial research is in progress today to investigate and increase the performance of CMOS devices for RF applications. By using a layout optimization technique, which reduces the parasitic components, we can obtain good RF characteristics for MOSFETs [3]. In this paper, we present the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) characteristics of 0.18- μm MOSFETs with various layouts.

II. MEASUREMENT

Multi-finger type MOSFETs were laid out with a common-source configuration. Scattering parameters were measured in devices with various unit finger lengths (L_f). Measurements of the scattering parameters were carried out in the frequency range of 0.5~50 GHz by

using on-wafer RF probes and a HP8510C vector network analyzer (VNA). The power level of the incident wave was -10 dBm. A ground-signal-ground (GSG) pad was used. System calibration with an ISS (impedance-standard substrate) was done to extend the reference plane to the probe tips. Two-step de-embedding, which includes open and short de-embedding, was performed.

III. RESULTS AND DISCUSSION

Figure 1 shows the measured scattering parameters of an nMOSFET with $W = 5 \times 20 \mu\text{m}$ and $L = 0.18 \mu\text{m}$ in the Smith chart. The magnitude of S_{21} was larger

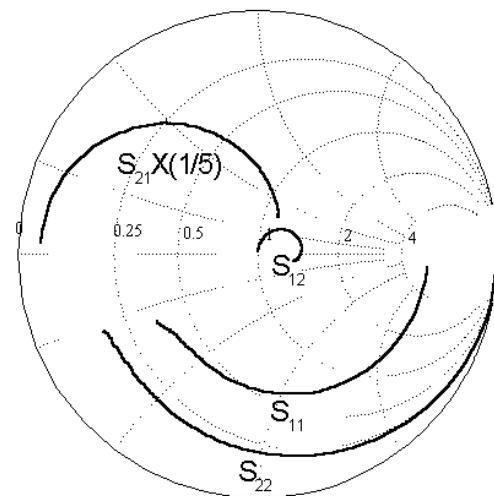


Fig. 1. Measured scattering parameters of an nMOSFET in the frequency range of 0.5~50 GHz. The power level of incident wave was -10 dBm.

*E-mail: kwhan@inca.kaist.ac.kr; Fax: +82-42-869-8590

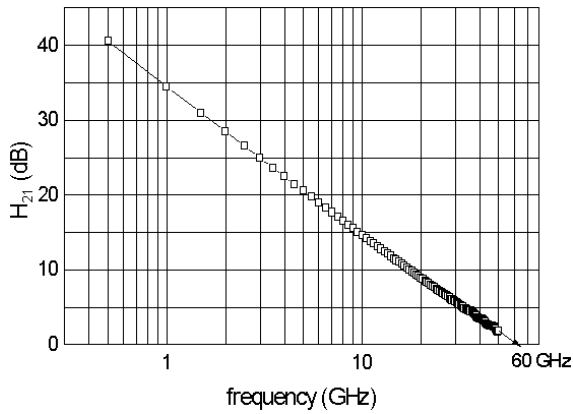


Fig. 2. f_T was extracted by using a linear regression. In this nMOSFET device, f_T was 60 GHz at $V_g=1.2$ V and $V_d=2.0$ V

than unity, which showed that the transistor amplifies the input power. H_{21} , the forward current gain, on a dB scale degraded linearly with logarithm of the frequency, as shown in Fig. 2. The cutoff frequency (f_T) is extracted at the point where H_{21} becomes unity. For this nMOSFET ($W = 5 \times 10 \mu\text{m}$ and $L = 0.18 \mu\text{m}$), f_T was 60 GHz.

Figure 3 shows the dependencies of the transconductance (g_m) and the f_T as functions of the drain current in nMOSFETs and pMOSFETs. The drain voltage was fixed to 2 V. The gate voltage was changed from 0.6 V and 2 V. The transconductance develops a distinct maximum at a certain bias. The reduced g_m at low bias is a result of the large thickness of the channel near the weak inversion condition while mobility degradation lowers g_m at high fields [4]. The mobility degradation in nMOSFETs was obviously more pronounced than in pMOSFETs within the bias boundaries. The f_T shows a similar strong bias dependency since it relates to g_m as

$$f_T = g_m / 2\pi C_{gg} \quad (1)$$

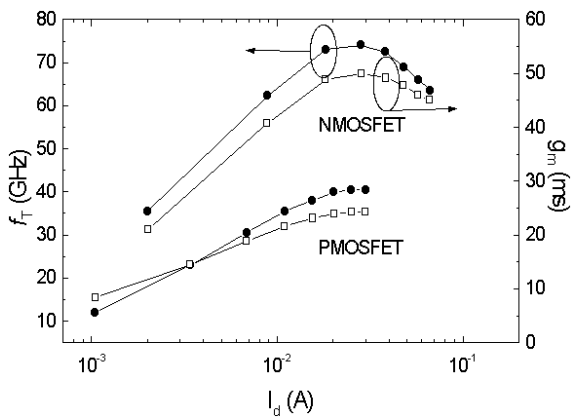


Fig. 3. Dependency of f_T on the drain current in an nMOSFET and a pMOSFET. The f_T curve has the same shape as the g_m curve.

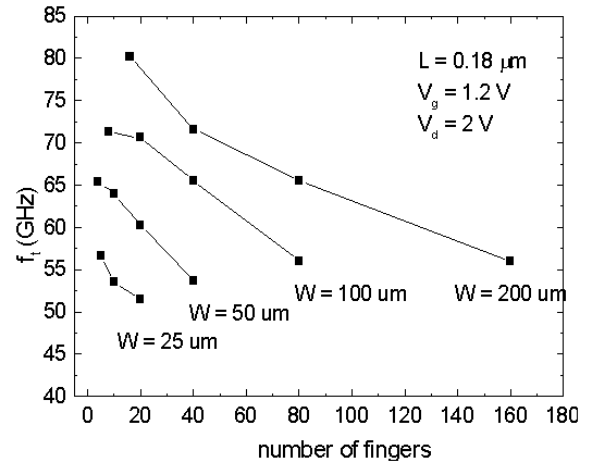


Fig. 4. Dependency of f_T on the number of fingers. f_T decreases as the number of fingers increases with the same total width.

where C_{gg} is the total capacitance at the gate node. f_T and g_m have a maximum value at $V_g=1.2$ V for $V_d=2$ V in nMOSFETs. In the saturation region, f_T changes slightly with drain bias.

Figure 4 shows the extracted f_T of nMOSFETs as a function of the number of finger at the same total device width and optimum bias condition of $V_g=1.2$ V and $V_d=2$ V. As the number of fingers increases, f_T degrades because of an increase in the number of gate contact pads and, hence, in the total value of C_{gb} indicated in the inset of Fig. 5 [5]. Since intrinsic parts of devices with large widths become large compared to the parasitic C_{gb} , devices with large total widths have higher cutoff frequencies at same number of fingers.

Figure 6 shows the de-embedding effect on f_T . Open de-embedding, which subtracts the pad capacitance and forward coupling, has a considerable effect on f_T . The cutoff frequency of intrinsic devices was two times larger than that of devices with pad parasitics, which indicated that the pad capacitance was comparable to that of an intrinsic device. However, since f_T itself is nearly inde-

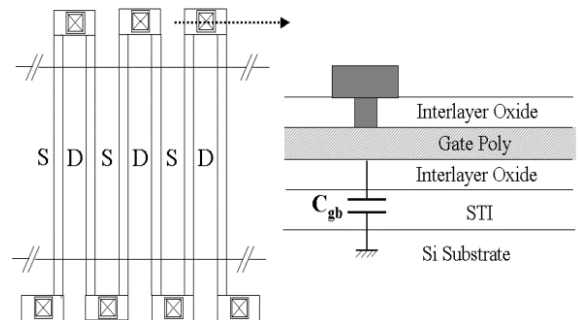


Fig. 5. Schematic of the multi-finger layout. The capacitance C_{gb} increases as the number of fingers increases, which degrades the cutoff frequency (f_T).

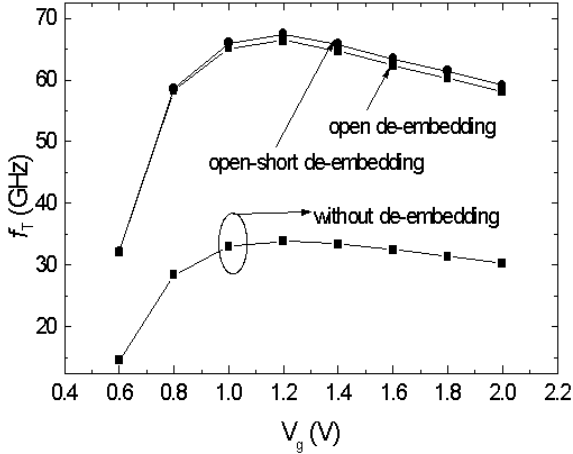


Fig. 6. This figure shows the de-embedding effect on f_T . Since f_T is nearly independent of the series resistance, short de-embedding has little effect on f_T .

pendent of the series resistance, short de-embedding has no significant effect on f_T .

Figure 7(a) shows the maximum stable gain (MSG) and maximum available gain (MAG) as a function of the frequency in devices with channel lengths from 1 μm to

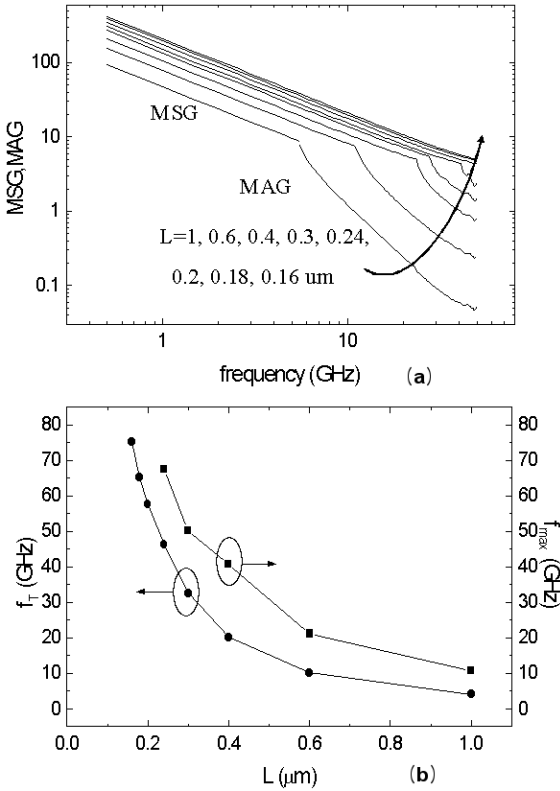


Fig. 7. (a) Maximum stable gain (MSG) and maximum available gain (MAG) for different channel lengths and (b) the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) as functions of the channel length.

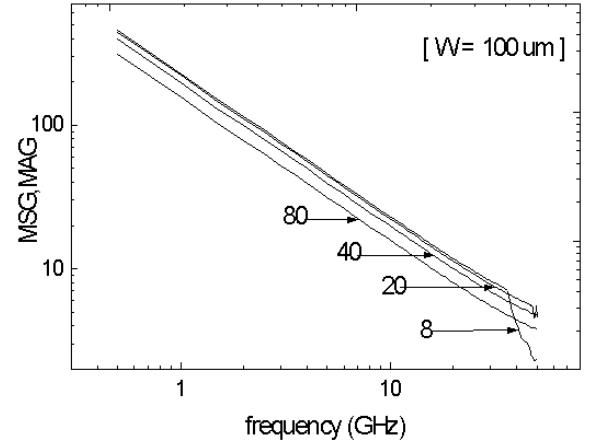


Fig. 8. MSG and MAG in 0.18- μm nMOSFETs with different finger lengths.

0.16 μm . The maximum oscillation frequency (f_{max}) is extracted at the point where MAG becomes unity [6]. For the nMOSFET with a channel length of 0.6 μm , f_{max} was 21 GHz. Figure 7(b) shows the f_T and the f_{max} versus channel length in nMOSFETs. As the channel length scales down, f_T increases because g_m increases and C_{gg} decreases.

Figure 8 shows MSG and MAG in 0.18- μm nMOSFETs with different numbers of fingers with the same total device width of 100 μm . The MAG was only observed in the device with eight fingers in the measurement range up to 50 GHz, which indicated that the device had the smallest f_{max} . The value of f_{max} can be approximately expressed as follows:

$$f_{max} = \sqrt{f_T / (8\pi R_g C_{gd})}, \quad (2)$$

where C_{gd} is the drain-to-gate capacitance and R_g is the gate resistance. The gate resistance (R_g) is a dominant parameter governing f_{max} with the layout variation of the gate fingers in MOSFETs. R_g can be expressed simply as $R_g = R_S W / (n^2 L)$, where R_S is the polysilicon sheet resistance, L is the gate length, W is the total gate width, and n is the number of gate fingers. Although the device with small number of fingers has a higher f_T , the gate resistance (R_g) dominantly degrades the maximum oscillation frequency.

IV. CONCLUSIONS

We have shown that 0.18- μm nMOSFETs have cutoff frequencies from 50 GHz to 80 GHz for different layout conditions and 0.18- μm pMOSFETs have a 40 GHz cutoff frequency with a total width of 100 μm and unit finger length of 5 μm , which indicates that submicron MOSFETs are possible candidate for RF applications. f_T and f_{max} decreased and increased, respectively, with number increase of the fingers.

ACKNOWLEDGMENTS

This work was supported by the National Program for Tera-level Nano Devices through the Ministry of science and Technology. The authors also thank the Anam Semiconductor for device fabrication.

REFERENCES

- [1] K.-H. Baek, G.M. Lim, S.D. Cho, Y.C. Kim, H.C. Kim, S.K. Kim, D.J. Kim and D.M. Kim, J. Korean Phys. Soc. **37**, S915 (2000).
- [2] S.-J. Maeng, J.-K. Mum, M.-G. Kim, J.-J. Lee and J.-L. Lee, J. Korean Phys. Soc. **30**, S117 (1997).
- [3] S.P. Voinigescu, S.W. Tarasewicz, T. MacElwee and J. Ilowski, in IEDM Tech. Dig., pp. 721-724, 1995.
- [4] J.N. Burghartz, M. Hargrove, C.S. Webster, R.A. Groves, M. Keene, K.A. Jenkins, R. Logan and E. Nowak, IEEE Trans. on Electron Devices **47**, 864 (2000).
- [5] E.Morifuji, H.S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsutka, M. Kinugawa, Y. Katsumata and H. Iwai, in Symp. VLSI Technology Dig. Tech. Papers, pp. 163-164, 1999.
- [6] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design* (Prentice-Hall, 1984)