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A novel bulk-input low voltage and low power four quadrant analog multiplier in weak inversion

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Abstract A new four quadrant voltage mode bulk input analog multiplier is presented .The proposed multiplier is designed to operate in weak inversion. Multiplication is done by driving the bulk terminals of the MOS devices which offers linear dynamic range of ±80 mV. The simulation shows, it has a linearity error of 5.6 %, THD of nearly 5 % and −3 dB band width of 221 kHz. Total power consumption is very low i.e. 714 nW. The circuit operates at a supply voltage of 0.5 V and is designed using 180 nm CMOS technology. It is suitable for low power bioelectronics and neural applications.

Keywords Analog multiplier · Bulk-input MOS circuits · Four quadrant multiplication · Low voltage and low power analog IC design · MOS transistor · Weak inversion

1 Introduction

Analog IC design has been revolutionized by the low voltage and low power design methodology especially when it comes to portable, battery operated systems. In analog signal processing, four-quadrant-multiplication is one of the important operations performed on signals. It is used in a number of applications including modulator, doublers, adaptive filters in communication circuit, in phase detection in Phase Locked Loop, as a mixer in a front-end receiver and synaptic multiplier in hardware implementation of neural networks [1, 2], convolver in sensor applications [3]. Considering the importance of multiplier and its applications, it is challenging to design a multiplier suitable for low voltage and low power operations.

Analog multiplier design was first reported in the work of Gilbert [4] which was implemented using BJT. Since then number of works has been reported specially in CMOS technology based on (i) mode of input i.e. current mode and voltage mode and (ii) the region of the operation of MOS device. If we consider the designs based on strong inversion regime, the voltage mode multipliers in saturation can be found in [5, 6], in linear region can be found in [7, 8], and current mode multipliers can be found [9, 10]. For saturated weak inversion regime, voltage mode multipliers are reported in [11–13] and current mode multipliers in [14]. The designs based on weak inversion region mostly followed the Gilbert cell topology and modified Gilbert cell [15] for voltage mode operation. The designs in weak inversion suffered from poor dynamic range, limited voltage swing (few hundred mV) and limited band width. For low voltage and low power applications operating devices in weak inversion is quite advantageous [16, 17]. One of the best features being very low $V_{DS.sat}$ which nearly four times the thermal voltage [18, 19].

Usually the gate of the MOS device is used for controlling the inversion level, with the bulk terminal is tied to its own well. But this bulk terminal can be used to decrease or increase the effective inversion layer charge by applying some potential to it with respect to source, although it comes at the cost of the mismatch in drain to source current I_{DS}. If we consider a pMOS device, then effective inversion layer can be increased by applying a negative potential to the n-type bulk with respect to p-type source which holds an exponential relationship with I_{DS}. The exponential relation between I_{DS}, V_{GS} and V_{BS} has been exploited to implement

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some of the arithmetic circuits (e.g. $\sinh(x)$ [20], $^1/_x$ [21], $\sin(x)$ [22] etc.). Here we have presented a novel multiplier which uses the gate of the MOS device for biasing and bulk terminal for applying input, to obtain the four quadrant multiplication. It has higher linear dynamic range and very low voltage and low power usage. This work is organized as; in Sect. 2 the basic and full operation of the circuit is described, in Sect. 3 mismatch of the bulk input devices has been analyzed and formulated and followed by the simulated result, Sect. 4 describes the complete simulation, results about the operations of the proposed multiplier and comparison of results, and conclusion in Sect. 5.

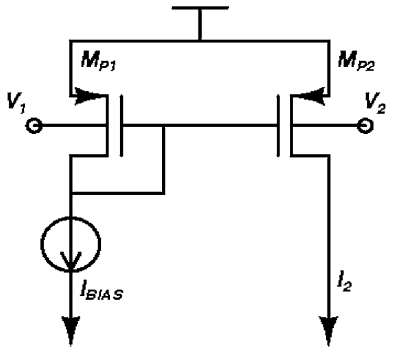

Fig. 1 Exponential approximation circuit

2 Operation of the proposed multiplier

2.1 MOS in weak inversion with active bulk terminal

Considering a p-MOS device operated in weak inversion the drain to source current (ignoring the early effect $V_{DS} \ll V_E$) can be given by [23, 24]

$$I_{DS} = I_{D0} e^{\frac{-V_{gs}}{\eta U_T}} e^{\frac{-(\eta-1)V_{bs}}{\eta U_T}} \left[1 - e^{\frac{-V_{ds}}{\eta U_T}}\right] \quad (1)$$

Where $I_{D0} = I_S \times e^{\frac{V_{TH}}{\eta U_T}}$ and $I_S = 2 \times \eta \times \beta \times U_T^2$ and $U_T = \frac{kT}{q}$. η is the subthreshold slope parameter which varies between 1 and 2 [18, 23], and $\beta = \mu \times C'_{ox} \frac{W}{L} \times V_E$ is the Early voltage which is nearly 10 V. As we have to operate the device in weak inversion so each pMOS has been designed to operate below the V_{TH} where $I_{DS} \ll I_S$. Ignoring the second order effects, for a given size of the device inversion coefficient $\left(IC = \frac{I_{DS}}{I_S}\right)$ should be less than 0.1 [19, 24, 25]. The trans-conductance parameter for the bulk input device is represented as [17, 25]; $g_{mb} = \frac{\partial I_{DS}}{\partial V_{bs}} = \frac{-(\eta-1)}{\eta U_T} I_{DS}$. Since we are using bulk terminal, threshold voltage for the MOS device will be affected, which can be given by the expression [23];

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|V_{SB} + \phi_0|} - \sqrt{|\phi_0|}\right) \quad (2)$$

V_{TH0} represents the threshold voltage when V_{SB} is zero, $\phi_0 = 2\phi_F + \nabla\phi$; $\nabla\phi$ is nearly $6U_T$ at room temperature and γ is the body effect parameter which depends on the process and given by $\gamma = \frac{-\sqrt{2 \times q \times \in_{si} \times N_D}}{C'_{ox}}$, where N_D the donor concentration per unit volume and C'_{ox} is the oxide capacitance per unit area of the device in a given process.

2.2 Exponential approximation circuit

The exponential function can be obtained by using a bulk input current mirror where gate is used for biasing and bulk is used for applying differential input and each device is operated in saturated weak inversion. If two devices are biased in weak inversion in saturation ($V_{DS} \gg 4U_T$) with an initial assumption of matched devices, (mismatch is considered in Sect. 3) the current expressions for the circuit shown in Fig. 1 can be written based on the Eq. (1) as;

$$I_{DS1} = I_{D0} e^{\frac{-V_{gs1}}{\eta U_T}} e^{\frac{-(\eta-1)V_{bs1}}{\eta U_T}} \quad (3)$$

And

$$I_{DS2} = I_{D0} e^{\frac{-V_{gs2}}{\eta U_T}} e^{\frac{-(\eta-1)V_{bs2}}{\eta U_T}} \quad (4)$$

$$I_{DS2} = I_{BIAS} e^{\frac{-(\eta-1)(V_{bs2}-V_{bs1})}{\eta U_T}} \quad (5)$$

Assuming V_{bs2}, V_{bs1} are very small i.e $|V_{bs2}|, |V_{bs1}| \ll \frac{\eta U_T}{(\eta-1)}$ i.e. taking $\eta = 1.2$, it comes out to be nearly 155 mV. This helps us to get more dynamic range as compared to gate input multiplier circuits [11, 15]. Equation (5) can also be written as;

$$I_{DS2} = I_{BIAS} e^{\frac{-(\eta-1)V_{bs2}}{\eta U_T}} e^{\frac{(\eta-1)V_{bs1}}{\eta U_T}} \quad (6)$$

It can be expanded with the help of Taylor's series for

$$= I_{BIAS}\left[1 - \left(\frac{(\eta-1)V_{bs2}}{\eta U_T}\right) + \frac{1}{2!}\left(\frac{(\eta-1)V_{bs2}}{\eta U_T}\right)^2 - \ldots\right] \times \left[1 + \left(\frac{(\eta-1)V_{bs1}}{\eta U_T}\right) + \frac{1}{2!}\left(\frac{(\eta-1)V_{bs1}}{\eta U_T}\right)^2 \ldots\right] \quad (7)$$

The exponential i.e. Eq. (6) and its approximated series expansion i.e. Eq. (7) will follow closely each other only when $\left|\left(\frac{(\eta-1)V_{bs2,1}}{\eta U_T}\right)\right| \ll 1$. To quantify the above fact the two expressions and the difference between these two are plotted against $\frac{(\eta-1)(V_{bs2}-Vbs1)}{\eta U_T}$ which is shown in Figs. 2 and 3 respectively. The error between these two is less than .01 i.e. 1 % when $\left|\left(\frac{(\eta-1)V_{bs2,1}}{\eta U_T}\right)\right| < 0.2$.

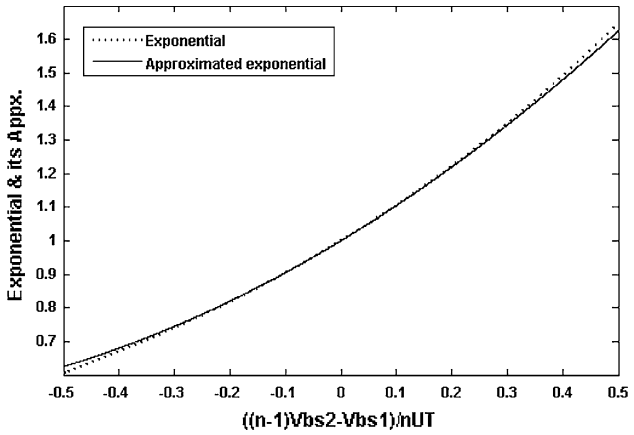

Fig. 2 Error between exponential and its approximation

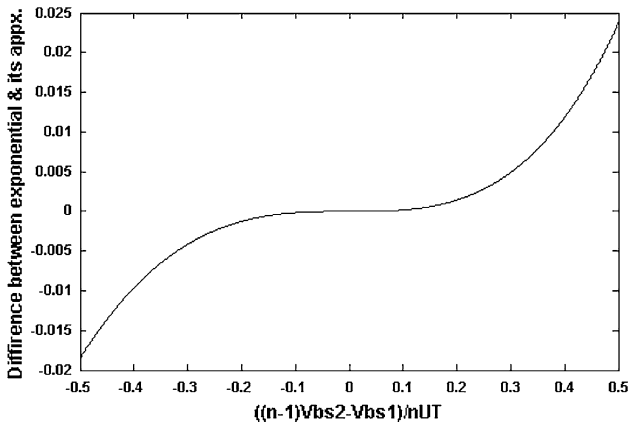

Fig. 3 Difference between exponential and its approximation

2.3 Numerical explanation of the proposed multiplier

The approximated exponential function circuit can be used to apply single quadrant input polarity. For four quadrant multiplication we can arrange four such circuits interconnected in a fashion as shown in Fig. 4 with both the inputs $|V_{in2}|, |V_{in1}| \ll \frac{\eta U_T}{(\eta-1)}$. The mathematical expression of four quadrant multiplications is illustrated below. Assuming the bulk to source voltage of respective devices as V_1, V_2, V_3, V_4, V_5, V_6, V_7, V_8, the input voltages can be written of the form similar to [11]; $V_1 = V_7 = V_b + V_{in1}$; $V_2 = V_4 = V_b - V_{in2}$; $V_3 = V_5 = V_b - V_{in1}$; $V_6 = V_8 = V_b + V_{in2}$. The current expression for I_{DS2}, I_{DS4}, I_{DS6}, I_{DS8} can be written as follows;

$$I_{DS2} = I_{BIAS} e^{\frac{-(\eta-1)(V_2-V_1)}{\eta U_T}} = I_{BIAS} e^{\frac{(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \tag{8}$$

Neglecting the higher order terms Eq. (8) can be approximated as;

$$\begin{aligned} &\cong I_{BIAS}\left[1 + \frac{(\eta-1)V_{in2}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2\right] \\ &\times \left[1 + \frac{(\eta-1)V_{in1}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2\right] \end{aligned} \tag{9}$$

Similarly, I_{DS4}, I_{DS6}, I_{DS8} can be written as;

$$\begin{aligned} I_{DS4} &= I_{BIAS} e^{\frac{-(\eta-1)(V_4-V_3)}{\eta U_T}} = I_{BIAS} e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \\ &\cong I_{BIAS}\left[1 + \frac{(\eta-1)V_{in2}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2\right] \\ &\times \left[1 - \frac{(\eta-1)V_{in1}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2\right] \end{aligned} \tag{10}$$

$$\begin{aligned} I_{DS6} &= I_{BIAS} e^{\frac{-(\eta-1)(V_6-V_5)}{\eta U_T}} = I_{BIAS} e^{\frac{-(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \\ &\cong I_{BIAS}\left[1 - \frac{(\eta-1)V_{in2}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2\right] \\ &\times \left[1 - \frac{(\eta-1)V_{in1}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2\right] \end{aligned} \tag{11}$$

$$\begin{aligned} I_{DS8} &= I_{BIAS} e^{\frac{-(\eta-1)(V_8-V_7)}{\eta U_T}} = I_{BIAS} e^{\frac{-(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \\ &\cong I_{BIAS}\left[1 - \frac{(\eta-1)V_{in2}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2\right] \\ &\times \left[1 + \frac{(\eta-1)V_{in1}}{\eta U_T} + \frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2\right] \end{aligned} \tag{12}$$

As shown in Fig. 3 differential output voltage of the proposed multiplier is written as;

$$V_{out} = I_{out} \times R = [(I_{DS2} + I_{DS6}) - (I_{DS4} + I_{DS8})]R \tag{13}$$

So the output current is approximated to be

$$I_{out} \cong 4 \times \left[\frac{(\eta-1)}{\eta U_T}\right]^2 V_{in2} V_{in1} \tag{14}$$

From the above expression, we have mathematically shown that the proposed multiplier can perform four quadrant multiplications. It can be observed that linear dynamic range of the multiplier is increased by a factor of $\frac{(\eta-1)}{\eta U_T}$ due to the bulk input terminal. Since the devices have been biased in the weak inversion the total power is quite low.

3 Formulation of mismatch for the multiplier

The whole mismatch in the proposed circuit can be analyzed by considering variations due to the process dependent parameters and the mismatch in the bias voltages and

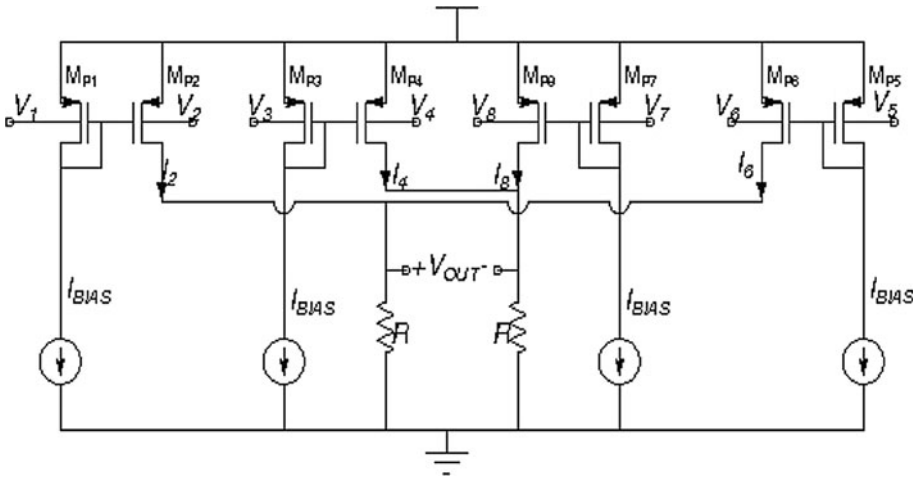

Fig. 4 Proposed multiplier circuit diagram

currents. Process dependent mismatch in drain current can be considered in the parameter I_{D0} which can include β mismatch (in weak inversion its effect can be neglected [18]), V_{TH} mismatch which exponentially vary the current [26] and η due to V_{BS} (ignoring the effect of η in the exponential terms). These mismatches can be included by taking a term $I_{D0}(1 + \Delta I_{D0})$ and the bias mismatch can be included at later stage simply writing $I_{BIAS} + \Delta I_{BIAS}$ to the final current expression involving mismatch. The mismatch in V_{DS} for each transistor pair can also be included for each current expression i.e. Eqs. (8), (10–12) by introducing a factor $\delta_{i,j}$ where i and j represents transistor pair. From Eq. (1) it can be written as;

$$I_{DS2} = I_{BIAS} \times \xi_{2.1} \times e^{-\frac{(\eta-1)V_{bs2,1}}{\eta U_T}} \times \delta_{2,1} \tag{15}$$

where $\xi_{2.1} = \frac{(1+\Delta I_{D02})}{(1+\Delta I_{D01})}$ the term that incorporates the mismatch for I_{D0} between two devices i.e. M_{P1} and M_{P2} having variation of $\Delta I_{D01}, \Delta I_{D02}$ respectively. And $V_{bs2,1} = V_{bs2} - V_{bs1}$ and $\delta_{2,1} = \left[1 - e^{\frac{-V_{ds2}}{\eta U_T}}\right] / \left[1 - e^{\frac{-V_{ds1}}{\eta U_T}}\right]$ takes care of the mismatch due to V_{ds} between the two devices. The Eq. (15) can be rewritten in the form of input voltages [with reference to Eq. (8)] and a single mismatch term ρ that gives rise to equation of the form;

$$I_{DS2} = \rho_2 \times I_{BIAS} \times e^{\frac{(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \tag{16}$$

where $\rho_2 = \xi_{2,1} \times \delta_{2,1}$ and similar expression for other current equations can be written as [with reference to Eqs. (10–12) for I_{DS4}, I_{DS6}, and I_{DS8} respectively];

$$I_{DS4} = \rho_4 \times I_{BIAS} \times e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \tag{17}$$

$$I_{DS6} = \rho_6 \times I_{BIAS} \times e^{\frac{-(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \tag{18}$$

$$I_{DS8} = \rho_8 \times I_{BIAS} \times e^{\frac{-(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \tag{19}$$

Now the sum of I_{DS2} and I_{DS6} can be written as;

$$= I_{BIAS}(\rho + \Delta\rho_{2,6}) \left[e^{\frac{(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} - e^{\frac{-(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \right] \tag{20}$$

In a same way I_{DS4} and I_{DS8} can be summed up to form,

$$= I_{BIAS}(\rho + \Delta\rho_{4,8}) \left[e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} - e^{\frac{-(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \right] \tag{21}$$

From Eq. (4) I_{out} can be expanded with Taylor's series and final current expression can be written as;

$$I_{out} \cong I_{BIAS} \times \rho \times 4 \left[\frac{(\eta - 1)}{\eta U_T} \right]^2 V_{in2} V_{in1} + \lambda I_{BIAS} \tag{22}$$

where λ accounts for the mismatch expressions due to multiplied terms with $\Delta\rho$. Equation (22) gives the approximated expression for the process dependent mismatch. If bias dependent mismatch is to be included then, I_{BIAS} can be simply replaced by $I_{BIAS}(1 + \Delta I_{BIAS})$. ΔI_{BIAS} accounts for the variation due to bias current between four different pairs of the exponential approximation circuits. The bias dependent mismatch can be significantly reduced by providing proper biasing circuitry. To test the mismatch effects on the circuit, Monte Carlo Simulation is performed for 100 runs with 30 % variation between the devices; the result of DC error is limited within 5 %. It is also performed with mismatch in I_{BIAS}, the error comes within 5 %.

4 Results

To test the performance of the proposed multiplier, 0.18 μm 1P6M CMOS technology has been used. It has threshold

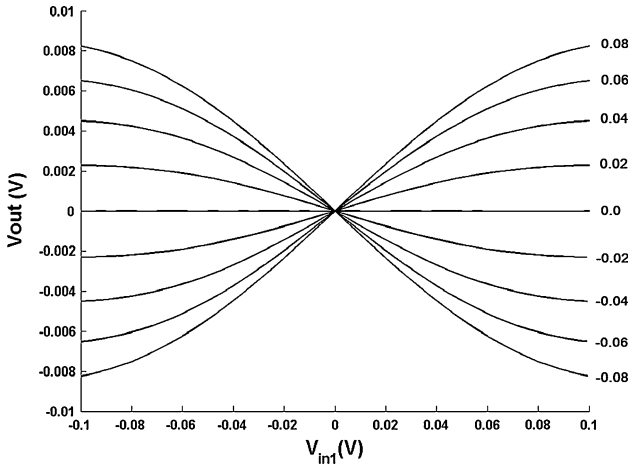

Fig. 5 DC characteristics $V_{out} - V_{in2}$

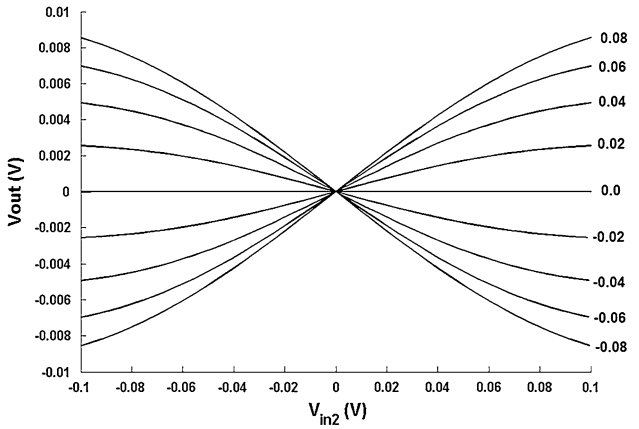

Fig. 6 DC characteristics $V_{out} - V_{in2}$

voltage is −0.44 V. Two equal resistors, with resistance 1.5 MΩ is used and the supply voltage is 0.5 V. To bias the devices in weak inversion the bias current is taken 300 nA. The devices are of equal size with (*W/L*) 50 µm/2 µm. The bias voltage V_b is of 400 mV. To test the DC characteristic V_{in1} is varied from −100 to 100 mV with V_{in2} varied from 80 to −80 mV through a step of 20 mV.

Simulations are performed using Spectre simulator and BSIM 3v3 model. The simulated DC transfer characteristic $V_{out} - V_{in1}$ is shown in Fig. 5. Similar characteristic is obtained for $V_{out} - V_{in2}$ and is shown in Fig. 6. Maximum nonlinearity is obtained when V_{in1} exceeds ±80 mV for Fig. 6 and for Fig. 5, maximum nonlinearity is obtained when V_{in2} exceeds ±60 mV. The nonlinearity error has been calculated by applying a DC voltage to V_{in2} and connecting an external gain stage with adjustable gain to the output to calculate $V_{out} - V_{in1}$, percentage of error obtained is 5.6 % which clearly indicates the effect of mismatch which is mainly due to the exponential effect of V_{TH} mismatch between the identically designed and identically biased device pairs.

Table 1 Summary of results

Parameters	Results
V_{DD}	0.5 V
V_b	400 mV
I_{BIAS}	300 nA
Input dynamic range	60 mV (V_{in1}), 80 mV (V_{in2})
−3 dB bandwidth	221 kHz at C = 10 pF, 50 mV DC, 80 mV, 10 kHz
THD %	5.82 (at 50 mV DC, 80 mV, 1 kHz)
	5.76 (at 50 mV DC, 80 mV, 10 kHz)
	3.13 (at 50 mV DC, 80 mV, 100 kHz)
	7.79 (at 80 mV, 1 kHz, 50 mV DC)
	7.71 (at 80 mV, 10 kHz, 50 mV DC)
	4.11 (at 80 mV, 100 kHz, 50 mV DC)
Linearity error	5.6 %
Power	714.3 nW
Process used	0.18 µm 1P6M CMOS

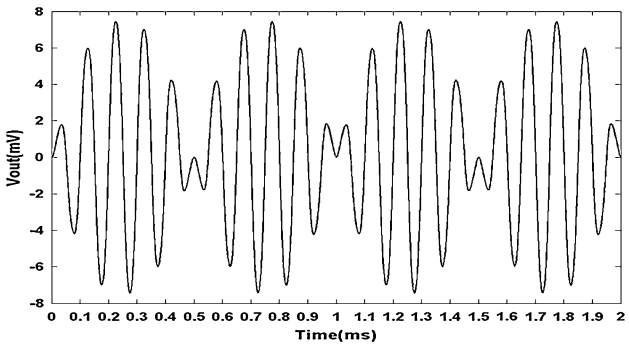

Fig. 7 Multiplication performance of the multiplier

Transient nonlinearity is checked by applying 50 mV DC at the input V_{in1} and 80 mV, 10 kHz sinusoidal signal at V_{in2} maximum THD comes nearly 5.8 % as frequency is increased to 100 kHz THD decreases. Simulations performed for the other input are shown in the Table 1, which has a maximum THD of 7.7 %, the reason behind this is the large mismatch in V_{TH} which creates even order distortion. Transient response of the circuit is shown in Fig. 7, when two sinusoidal signals of amplitude 80 mV, 1 and 10 kHz are applied to the inputs. The proposed circuit can also operate as a frequency doubler when both V_{in1} and V_{in2} of 80 mV, 1 kHz are applied, the output is shown in Fig. 8. The curve is doubled in frequency and amplitude appears to be very small. Frequency response of the multiplier is evaluated with a capacitor of 10 pF connected to the differential output; −3 dB band width comes nearly 221 kHz shown in Fig. 9. This restricts its applications to low frequency range operations which suitable for hardware implementation of artificial neural networks where mismatch

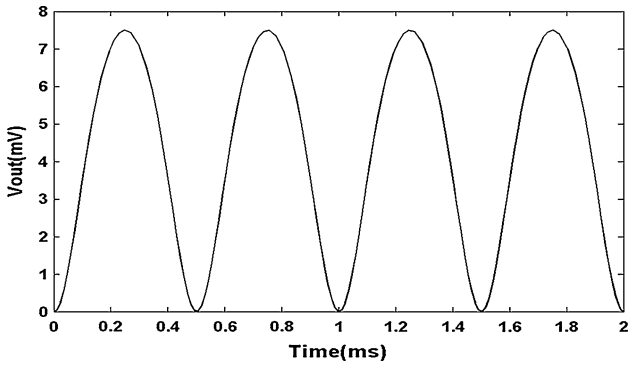

Fig. 8 Frequency multiplier operation of the multiplier

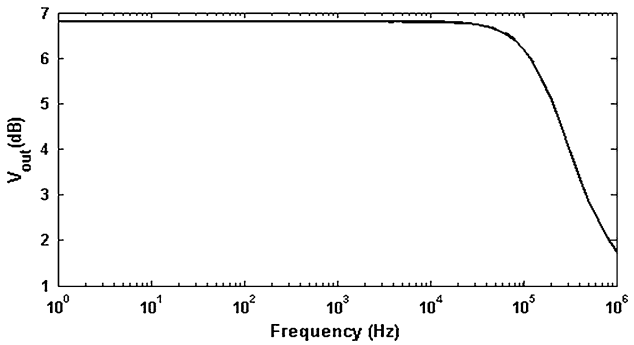

Fig. 9 Frequency response of the multiplier

Table 2 Comparison of Performance

Parameters	This work	Liu and Liu [11]	Pesvento and Kosh [12]
Process	0.18 μm 1P6M CMOS	0.35 μm n-well 2P4M	1.2 μm n-well CMOS
V_{DD}	0.5	1.5	5
V_b	400 m	800 m	NA
I_{BIAS}	300 nA	100 nA	NA
Input range	±80 mV	±120 mV	±2 V
Linearity error	5.6 %	5.2 %	NA
THD %	5.8	4.2	2.8
−3 dB band width	221 kHz	268 kHz	10 kHz
Power	714.3 nW	6.7 μW	1 μW

also can be overlook by the parallel operation. Total static power of the circuit is 714.3 nW. A brief comparison of performances is presented in Table 2 based on the results of the reported works.

5 Conclusion

A novel four quadrant multiplier suitable for very low voltage and very low power requirements is presented. Although mismatch degrades the performance of this bulk input multiplier (distortion, as well as nonlinearity being bit higher), bulk terminal has been efficiently used to perform the four quadrant multiplication and it is shown that it can also operate as a frequency doubler. It has a high dynamic range but the voltage swing is limited due to the DC mismatch effects .The degradation in mismatch can be compensated with the low voltage and low power it offers for suitable applications.

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References

1. Spencer, R. (1991). Analog implementations of artificial neural networks. *IEEE International Symposium on Circuits and Systems*, *2*, 1271–1274.
2. Saxena, N., & Clark, J. J. (1994). A four-quadrant CMOS analog multiplier for analog neural networks. *IEEE Journal of Solid-State Circuits, 29*(6), 746–749.
3. Blakiewicz, G. (2009). Analog multiplier for a low-power integrated image sensor. In *16th International Conference 'Mixed Design of Integrated Circuits and Systems, Jun. 2009, Loaz, Poland.*
4. Gilbert, B. (1968). A precise four-quadrant multiplier with sub nanosecond response. *IEEE Journal of Solid State Circuits, sc-3*(4), 365–373.
5. Babanezhad, J. N., & Temes, G. C. (1985). A 20-V Four-Quadrant CMOS analog multiplier. *IEEE Journal of Solid State Circuits, sc-20*(6), 1158–1168.
6. Chen, C., & Li, Z. (2006). A low power CMOS analog multiplier. *IEEE Transactions on Circuits and Systems-II: Express Briefs*, *53*(2), 100–104.
7. Ibaragi, E., Hyogo, A., & Sekine, K. (2000). A CMOS analog multiplier free from mobility reduction and body effect. *Analog Integrated Circuits and Signal Processing, 25*, 281–290.
8. Colli, G., & Montecchi, F. (1996). Low-voltage low-power CMOS four-quadrant analog multiplier for neural network applications. *International Symposium on Circuits and Systems, 1*, 496–499.
9. Naderi, A., Khoei, A., Hadidi, K., & Ghasemzadeh, H. (2009). A new high speed and low power four-quadrant CMOS analog multiplier in current mode. *International Journal of Electronics and Communications, 63*(9), 769–775.
10. Tanno, K., Ishizuka, O., & Tang, Z. (2000). Four quadrant CMOS current mode multiplier independent of device parameters. *IEEE Transactions on Circuits and Systems: II, 47*(5), 473–477.
11. Liu, W., & Liu, S. (2010). Design of a CMOS low-power and low voltage 4 quadrant analog multiplier. *Analog Integrated Circuits and Signals Processing, 63*, 307–312.
12. Pesavento, A., & Kosh, C. (1999). A wide linear range 4 quadrant multiplier in sub-threshold CMOS. *International Symposium on Circuits and Systems, 2*, 240–243.

13. Liu, S. I., & Chang, C. C. (1992). CMOS subthreshold four quadrant multiplier based unbalanced source-coupled pair. *International Journal of Electronics, 78*(2), 327–332.
14. Gravati, M., Valle, M., Guerrini, N., & Reyes, L. (2005). A novel current-mode very low power analog CMOS four quadrant multiplier. In *Proceedings of ESSCIRC*, Grenoble, France.
15. Coue, D., & Wilson, G. (1996). A 4 quadrant subthreshold mode multiplier for analog neural-network applications. *IEEE Transactions on Neural Networks, 7*(5), 1212–1219.
16. Vittoz, E. A., & Fellarth, J. (1977). CMOS analog integrated circuits based on weak inversion operation. *IEEE Journal of Solid State Circuits, sc-12*(3), 224–231.
17. Enz, C. C., & Vittoz, E. A. (1997). MOS transistor modeling for low-voltage and low-power analog IC design. *Journal of Microelectronic Engineering, 39*(1–4), 59–76.
18. Vittoz, E. A. (1985). The design of high-performance analog circuits on digital CMOS chips. *IEEE Journal of Solid State Circuits, sc-20*(3), 657–665.
19. Vittoz, E. A. (2003). Weak inversion in analog and digital circuits. In *CCCD Workshop. Lund, 2–3 Oct. 2003*.
20. Glaros, K. N., Katsiamis, A. G., & Drakakis, E. M. (2008). *Harmonic vs. geometric mean sinh integrators in weak inversion CMOS* (pp. 2905–2908). ISCAS: Seattle, WA.
21. van de Gevel, M., & Kuenen, J. C. (1994). Simple low-voltage weak inversion MOS l/x circuit. *IEEE Electronics Letters, 30*(20), 1639.
22. Mulder, J., van der Woerd, A. C., Serdijn, W. A., & van Roermund, A. H. M. (1995). *Translinear sin(x)-circuit in MOS technology using the back gate* (pp. 82–85). ESSCIRC: Lille.
23. Tsividis, Y. P. (2003). *Operation and modeling of the MOS transistors* (2nd ed., pp. 170–175). New York: Oxford University Publications.
24. Andreau, A. G., Boahen, K. A., Pouliquen, P. O., Pavasovic, A., Jenkins, R. & Strohbhen, K. (1991). Current mode subthreshold MOS circuits for analog VLSI neural systems. *IEEE Transactions on Neural Networks, 2*(2), 205–213.
25. Chamorro, J. P., Seguin, C., Lahuec, F., & Jezequel, M. (2006). Design rules for subthreshold MOS circuits. In *5th Analogue Decoding Workshop*. Torino, Italy.
26. Chen, M. J., Ho, J. S., & Huang, T. H. (1996). Dependence of current match on back-gate bias in weakly inverted MOS transistors and its modeling. *IEEE Journal of Solid State Circuits, 31*(2), 259–262.

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