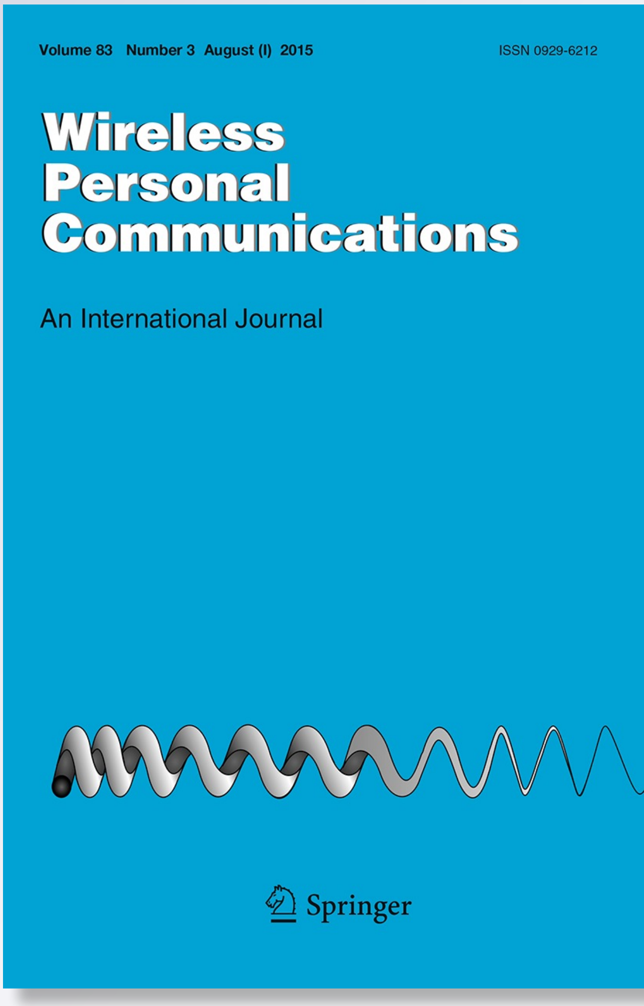
An Optimized Regulator with 290 nA Quiescent Current and $$115\,\upmu \hbox {W}$$ 115 μ W Power Consumption for UHF RFID Tags Using TLBO Algorithm

Ebrahim Abiri, Rezvan Dastanian, Mohammad Reza Salehi & Sajad Nejadhasan

Wireless Personal Communications
An International Journal

ISSN 0929-6212
Volume 83
Number 3

Wireless Pers Commun (2015)
83:2177-2192
DOI 10.1007/s11277-015-2507-y



Springer

Wireless Pers Commun (2015) 83:2177–2192
DOI 10.1007/s11277-015-2507-y

An Optimized Regulator with 290 nA Quiescent Current and 115 μW Power Consumption for UHF RFID Tags Using TLBO Algorithm

Ebrahim Abiri[1] · Rezvan Dastanian[1] · Mohammad Reza Salehi[1] · Sajad Nejadhasan[1]

Published online: 15 March 2015

Abstract In this paper a low power and low output ripple regulator is designed with teaching-learning-based optimization (TLBO) for radio frequency identification applications. In order to decrease the power consumption the voltage of regulator sub-blocks is supplied from elementary stages. In the proposed operational amplifier employed to the regulator, adaptive biasing is used and bandgap reference of the regulator is totally designed by MOSFET. To optimize the proposed regulator after modeling the regulator with the help of neural network, TLBO algorithm is used. The outputs of TLBO are output voltage, ripple value and power consumption. By using this algorithm the output voltage is 0.8 V with 2.78 mV ripple and 115 μW power consumption. Also the quiescent current of this design is decreased to 290 nA. The chip area of the layout design in Cadence software is about $0.00124\,mm^2$. The operation frequency of this circuit is 960 MHz and the simulation is done in 0.18 μm CMOS technology.

Keywords TLBO algorithm · RFID · Regulator · Neural network · Power consumption

1 Introduction

Given the fact that RFID technology has the numerous advantages such as high reading range, high speed and appropriate operation in various environment conditions, this technology can be a good replacement of barcode system. In general RFID tag is categorized into three active, passive and semipassive groups. In passive tag the sent wave from reader is received with tag antenna and this AC wave can be converted to the DC voltage by rectifier. Due to this fact that output voltage of rectifier has ripple, the regulator is applied after rectifier to decrease ripple.

✉ Ebrahim Abiri
abiri@sutech.ac.ir

[1] Department of Electronics, Shiraz University of Technology, P.O. Box 16315-1618, Shiraz, Iran

In [1] for decreasing the output voltage ripple of the rectifier, first large ripple of the input voltage is attenuated with series diodes, then this voltage is compared with reference voltage and the output voltage of the regulator is produced. But the disadvantage of this circuit is the sensitivity of the temperature variations. Reference [2] presents a regulator with 110 nA quiescent current, but it has excessive output ripple. Reference [3] uses MOSFET transistors instead of two resistors exist in output voltage sampling circuit in order to decrease the chip area. In most of the designed voltage reference circuits, one or some BJT transistors are used for creating a voltage which is insensitive to the temperature [3–6]. BJT transistors have not only high power dissipation, but also high fabrication cost.

In this paper for decreasing the power dissipation, the regulator sub-blocks are supplied with elementary stages of the rectifier and the designed sub-blocks are designed based on this voltage level. In addition the OPA biasing is done by adaptive biasing circuit. Also in BGR circuit, the total MOSFET structure is used. These two factors decrease the power dissipation. For providing the most optimized case and having the lowest power consumption and output voltage ripple, the proposed regulator is modeled by neural network and TLBO algorithm is used.

This paper is categorized as follow: the regulator structure is described in Sect. 2. Neural network and employed TLBO algorithm are studied in Sect. 3. Finally the simulation results, comparison and circuit layout are presented in Sect. 4.

2 The Regulator Structure

The block diagram of the regulator structure proposed in Ref. [7], which is included three BGR, OPA and SVR basic parts, is shown in Fig. 1. In this design in order to decrease the power consumption, two supply voltages are used that one of them is supplied from elementary stages $(V_{in,low})$ and the other is supplied from the extremity stages of the rectifier $(V_{in,high})$. In the proposed regulator, the sampled output voltage is compared with reference voltage. This comparison is done by OPA block and controls the pass current of $M_{p,pass}$ transistor.

If the difference of sampled voltage from $R_2(V_x)$ is more than V_{ref}, the OPA output is increased and decreases gate–source voltage V_{sg} of $M_{p,pass}$ transistor. Therefore drain

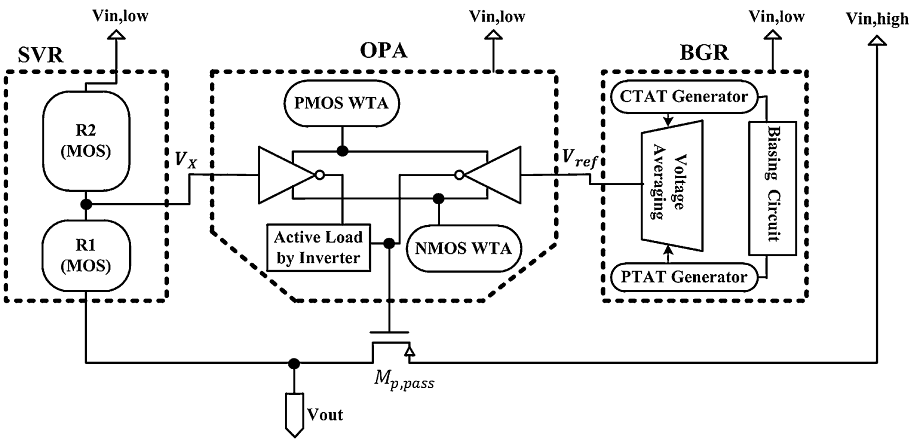


Fig. 1 The general block diagram of the proposed regulator

current of this transistor employed to the resistors is decreased and attenuates the output voltage. On the other hand, if V_x is smaller than V_{ref}, then the OPA output voltage is decreased and consequently V_{sg} is increased. Thus the drain current of $M_{p,pass}$ transistor becomes more and increases the output voltage. Therefore by increasing or decreasing the supply voltage, this circuit creates the negative feedback loop and produces the almost fixed voltage.

2.1 The Proposed BGR

The proposed BGR is shown in Fig. 2. This circuit consists of four parts: biasing circuit insensitive to the voltage variations, Proportional To Absolute Temperature (PTAT) voltage generator, Complementary To Absolute Temperature (CTAT) voltage generator and the voltage averaging circuit.

The voltage averaging block combines two PTAT and CTAT voltages which have proportional and Complementary relationship with temperature, respectively, and creates independent voltage to the temperature.

2.1.1 The Biasing Circuit

The fixed bias current circuit, which is insensitive to the input voltage variation, is used [8]. In this circuit, three NMOS transistors, M_{b5}, M_{b6} and M_{b7}, which exist in biasing circuit structure, works in sub-threshold region and leads to decreasing power dissipation.

2.1.2 PTAT and CTAT Voltage Generator Circuit

PTAT voltage generator consists of two connected M_1 and M_2, NMOS transistors [9]. Due to the circuit supply voltage and its design, the transistors work in sub-threshold region.

If W/L of M_1 transistor is K $(K > 1)$ times of the one of M_2 transistor and $V_{ds1}, V_{ds2} > 4V_T$, V_{PTAT} is calculated as (1).

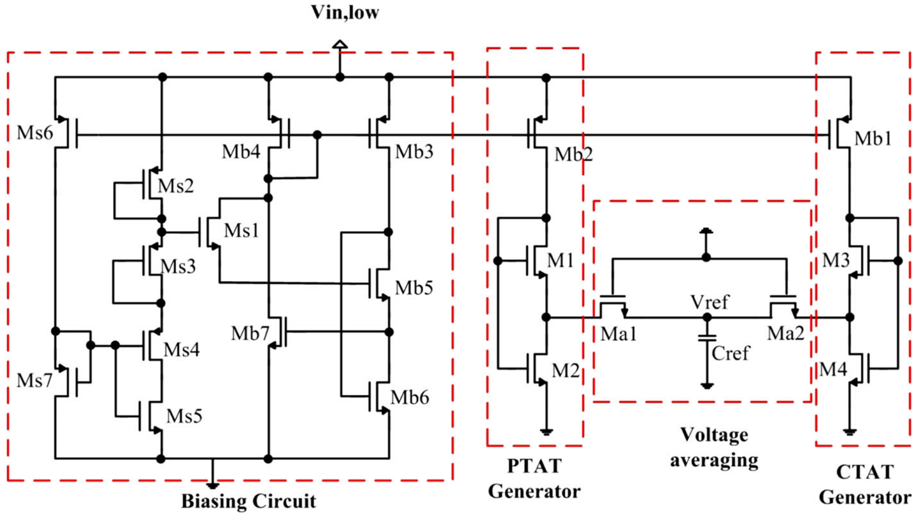


Fig. 2 The proposed reference voltage circuit [7]

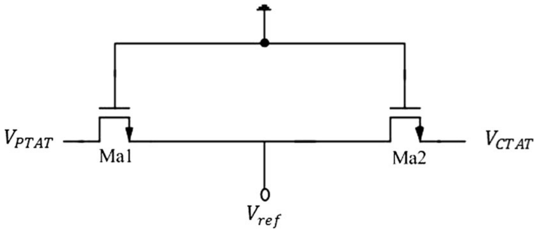


Fig. 3 The voltage averaging circuit

$$V_{PTAT} = V_{gs2} - V_{gs1} = \eta V_T ln(K) \tag{1}$$

Also with $M3$ and $M4$ transistors, CTAT voltage can be produced [10]. In this case if W/L of M_4 transistor is K' ($K' > 1$) times of the one of M_3 transistor and $V_{ds3}, V_{ds4} > 4V_T$, V_{CTAT} can be calculated as Eq. (2).

$$V_{CTAT} = V_{gs4} - V_{gs3} = -\eta V_T ln(K') \tag{2}$$

2.1.3 The Voltage Averaging Circuit

For combining two PTAT and CTAT voltages, the voltage averaging circuit shown in Fig. 3 is used. By this simple combination, the average of two V_{PTAT} and V_{CTAT} voltages is achieved at the output of the circuit [7].

2.2 The Proposed OPA

The complete designed OPA of Ref. [7] is shown in Fig. 4. This circuit includes three parts: circuit core, two adaptive biasing blocks, PMOS WTA (Winner Take All) and NMOS WTA, and active load.

2.2.1 OPA Circuit Core

The differential amplifier inputs of the proposed OPA circuit core shown in Fig.4 are as inverters. By using this topology the high gain can be achieved with the low current dissipation.

Based on Eq. (3) and by considering the sizes of transistors and the value of supply voltage, the transconductance and the gain are significantly increased [11]. One of the disadvantages of this circuit is the low bandwidth as low bias current passes through the inverter amplifier. This problem can be solved with the help of the adaptive biasing blocks.

$$G_m = G_{mn} + G_{mp} \tag{3}$$

where G_{mn} and G_{mp} is the transconductance of the NMOS and PMOS transistors, respectively.

2.2.2 The Adaptive Biasing Blocks

The limited biasing currents confine the maximum of output currents and decrease the gain. On the other hand using high biasing currents increase the power consumption. For overcoming this difficulty the adaptive biasing blocks are employed to the design for biasing the amplifier.

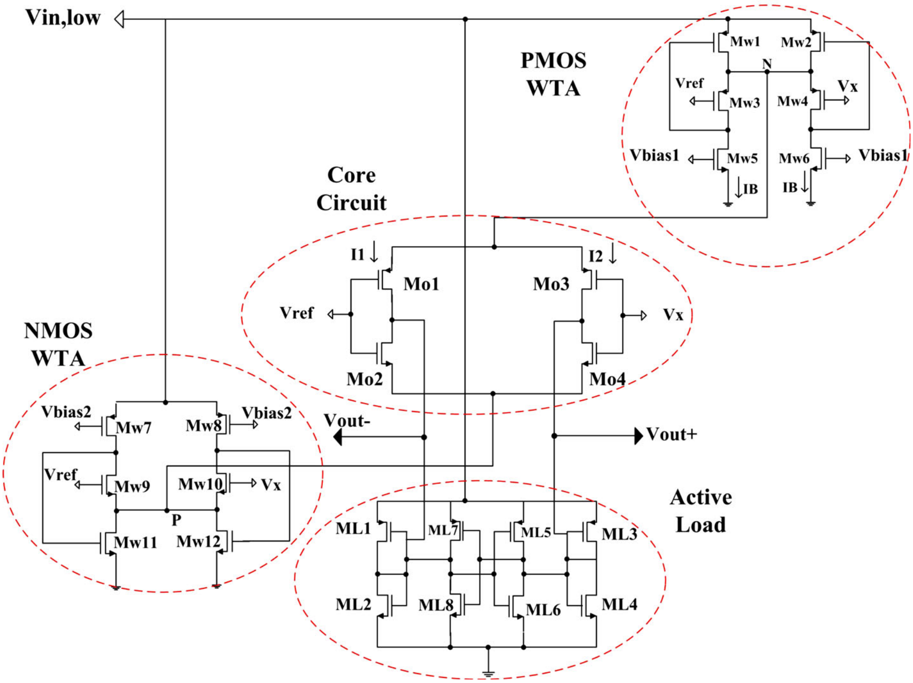


Fig. 4 The complete proposed OPA circuit

Since high inputs are exerted to the circuit, it increases the bias current automatically. For adaptive biasing, based on Fig. 4, NMOS WTA and PMOS WTA are used to bias NMOS and PMOS transistors of inverters, respectively [12, 13].

The output of the PMOS WTA circuit is based on the higher input voltage. If the steady state is established, then the input voltages are the same and equal to the common mode voltage $(V_{ref} = V_x = V_{cm})$ and the bias current equals to I_B.

If V_{ref} is more than V_x, the gate–source voltage of transistor M_{w4} is increased and consequently the drain voltage is increased and M_{w4} transistor enters the triode region. Also the voltage of N node is equal to the summation of V_{ref} and source–gate voltage of M_{w3} transistor. Under this condition I_2 becomes much more than I_B and I_1 is the same as I_B. on the other hand if V_x is more than V_{ref}, V_N is gained from the sum of V_x and source–gate voltage of M_{w4} transistor. In this case I_1 is much more than I_B and I_2 equals to I_B.

The output of NMOS WTA is based on the lower input voltage and the analysis similar to that of PMOS WTA can be done for NMOS transistors bias of inverters. Therefore by using the adaptive biasing circuits, the passing current of inverter amplifier transistors can be increased as the high gate–source voltage is created. Consequently the bandwidth and the amplifier gain are improved.

2.2.3 Active Loads as Inverter at the Output

The active load shown in Fig. 4 includes four inverters [11]. Two outermost inverters (M_{L1}–M_{L4}), which are connected to each other as a diode, create positive resistor equal to $2/g_{mo}$. Two innermost inverters (M_{L5}–M_{L8}) are cross coupled. This configuration creates a

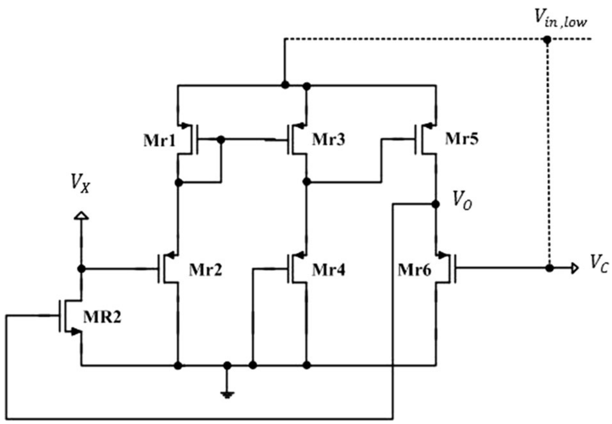


Fig. 5 The voltage controlled grounded resistor circuit

positive feedback and a negative resistor equal to $-2/g_{mi}$ is produced. By the combination of these two resistors, the natural instability of negative resistor is eliminated. If two innermost and outermost inverters are compatible with each other, the high output impedance is achieved and causes the increment of amplifier gain.

2.3 The SVR Implementation

Employing common resistors to the regulator structure increases the power dissipation and chip area. Thus NMOS diode connected transistor is used in the structure of Fig. 1 instead of R_1 resistor. The circuit of Fig. 5 which is the voltage controlled grounded resistor is used as R_2 resistor [14].

3 Neural Network and TLBO Algorithm

To produce a mathematic function from the considered outputs related to the circuit inputs, neural network is used. In order to optimize the circuit, the trained function from the neural network is used in TLBO algorithm. For the designed circuit, 16 inputs and 3 outputs are considered based on Table 1.

The inputs are selected due to their effects on the outputs, such as output voltage (V_{out}), output voltage ripple (V_{ripple}) and power dissipation (P_{diss}). Given the fact that the sizes of W and L of the output block transistors $(M_{R1}, M_{R2}$ and $M_{p,pass})$ effect on the outputs distinctly, they are separately considered as the circuit inputs. On the other hand, as W/L of the OPA block load transistors also effect on the outputs, $(W/L)_{M_{L1}}$ to $(W/L)_{M_{L8}}$ are considered as the other inputs. For defining the least $V_{in,low}$ and $V_{in,high}$ that the circuit has appropriate operation, $V_{in,low}$ and $V_{in,high}$ are considered as the inputs.

Since the aim of the optimization is to reach the minimum of the power consumption and output voltage ripple from the distinguished output, the output voltage (V_{out}), output voltage ripple (V_{ripple}) and power dissipation (P_{diss}) are chosen as the neural network outputs.

Table 1 The used inputs and outputs in the neural network and TLBO algorithm

Input					
$L_{M_{p,pass}}$	$L_{M_{R1}}$	$L_{M_{R2}}$	$W_{M_{p,pass}}$	$W_{M_{R1}}$	$W_{M_{R2}}$
$(W/L)_{M_{L1}}$	$(W/L)_{M_{L2}}$	$(W/L)_{M_{L3}}$	$(W/L)_{M_{L4}}$	$(W/L)_{M_{L5}}$	$(W/L)_{M_{L6}}$
$(W/L)_{M_{L7}}$	$(W/L)_{M_{L8}}$	$V_{in,low}$	$V_{in,high}$		
Output					
	V_{out}		V_{ripple}		P_{diss}

3.1 Neural Network

By the variation of the defined inputs during the 140 times simulation of the proposed regulator, the circuit outputs are measured and the data is used for achieving the desired function of the neural network. For doing this purpose, three steps of normalization, training and testing are done. From the 140 simulated data, 110 are used for the training step and 30 data are kept for testing step.

In the first step, all of the inputs and outputs are normalized in order to put in the range of [0, 1]. In the next, the nonlinear perceptron neural network with a hidden layer is used. logsig(x) function is used as Eqs. (4) and (5) for hidden and output layer.

$$Y = logsig(Xu) \tag{4}$$

$$Z = logsig(Yw) \tag{5}$$

where X is the normalized data, Y is the hidden layer output and Z is the last layer output, u and w are the hidden and output layer coefficients, respectively. Different neural network layers and the method of using logsig function are shown in Fig. 6. In this figure, S is the number of inputs, N is the number of hidden layer neuron and H is the number of outputs. In the design these values are 16, 300 and 3, respectively. Finally, the training function, which its error is lower than 0.04, is achieved in this step. In the last step for testing the achieved function, the last 30 data of inputs are employed to the function and the gained output of this function is unnormalized. These outputs are compared with the basic outputs, if the average error percent is low, then the training function is appropriate for TLBO algorithm.

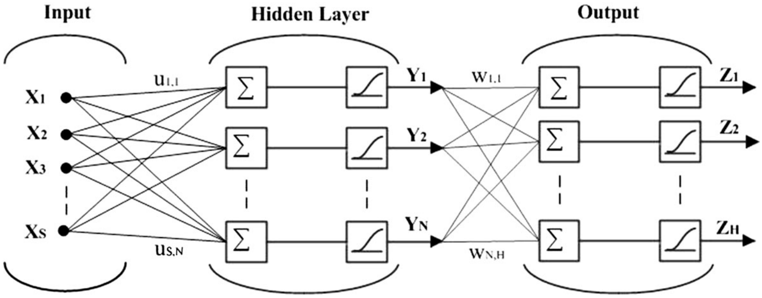


Fig. 6 The method of using logsig function in the hidden and output layer

3.2 TLBO Algorithm

TLBO algorithm is one of the novel optimization techniques that have been presented based on the teachers influence on his students and the students knowledge. This method has been first mentioned in Ref. [15]. In this algorithm the students and different lessons are considered as the population and variable of function or inputs, respectively. The member which has the best output of the objective function is considered as the teacher.

Since the knowledge of students depends on the teaching quality, students talent and data transmission between each other, TLBO algorithm is divided into two phases, teacher and student. After generating the initial population and achieving the output from the objective function, teacher and student phase are arranged, respectively.

In the teacher phase, the teacher tries to bring students knowledge near to his knowledge. This process repeats based on Eq. (6) randomly for generating a new member.

$$X_{new,i} = X_{old,i} + r_i(X_{tch,i} - T_F M_i) \tag{6}$$

where i is the number of inputs, $X_{old,i}$ is the old member of population that should learn from the teacher to advance his knowledge, r_i is a random number in the range of [0, 1] and $X_{tch,i}$ is the best member of population which means teacher that tries to bring the average of class near to his knowledge. T_F is the factor of teaching that is experimentally considered equal to 1 or 2, M_i includes the average of students marks in each lesson, $X_{new,i}$ is acceptable only when it is better than $X_{old,i}$.

In the student phase, if a student has the lower knowledge than the other student, he can improve his knowledge with the help of the other student, this process is done based on the Eq. (7).

$$X_{new,i} = X_{old,i} + r_i(X_j - X_k) \tag{7}$$

For the comparison of all the members, i index is utilized, $X_{old,i}$ is the old member that doesnt use the interchange of data transmission. r_i is a random number in the range of [0, 1] and X_j and X_k are two students who are selected randomly under the condition of $j \neq k$, $f(X_j) > f(X_k)$, if the new member of $X_{new,j}$ is better than the old member of $X_{old,i}$, it is accepted.

Most of the optimization algorithms require not only the common controlling parameters such as the number of population and variations, but also the special parameters which need precise setting. But it takes too long and has high sensitivity. TLBO algorithm does'nt have these special parameters and in compare with the other algorithms it is the advantages of TLBO algorithm. Considering the fact that T_F and r_i have defined values and are chosen randomly, they are not existed in the parameters algorithm's parameters. TLBO algorithm flowchart is shown in Fig. 7.

3.3 The Employed TLBO Algorithm

In this paper for designing the proposed regulator with the optimized power dissipation, output voltage and output ripple voltage, TLBO algorithm is used. Due to the fact that the training function achieved from the neural network and presented in Eqs. (4) and (5) have the normalized inputs and outputs, and consequntly the initial population is selected randomly in the range of [0, 1]. Finally for returning the inputs and outputs from the objective function, they should be unnormalized. The maximum and minimum values of inputs and outputs are presented in Table 2.

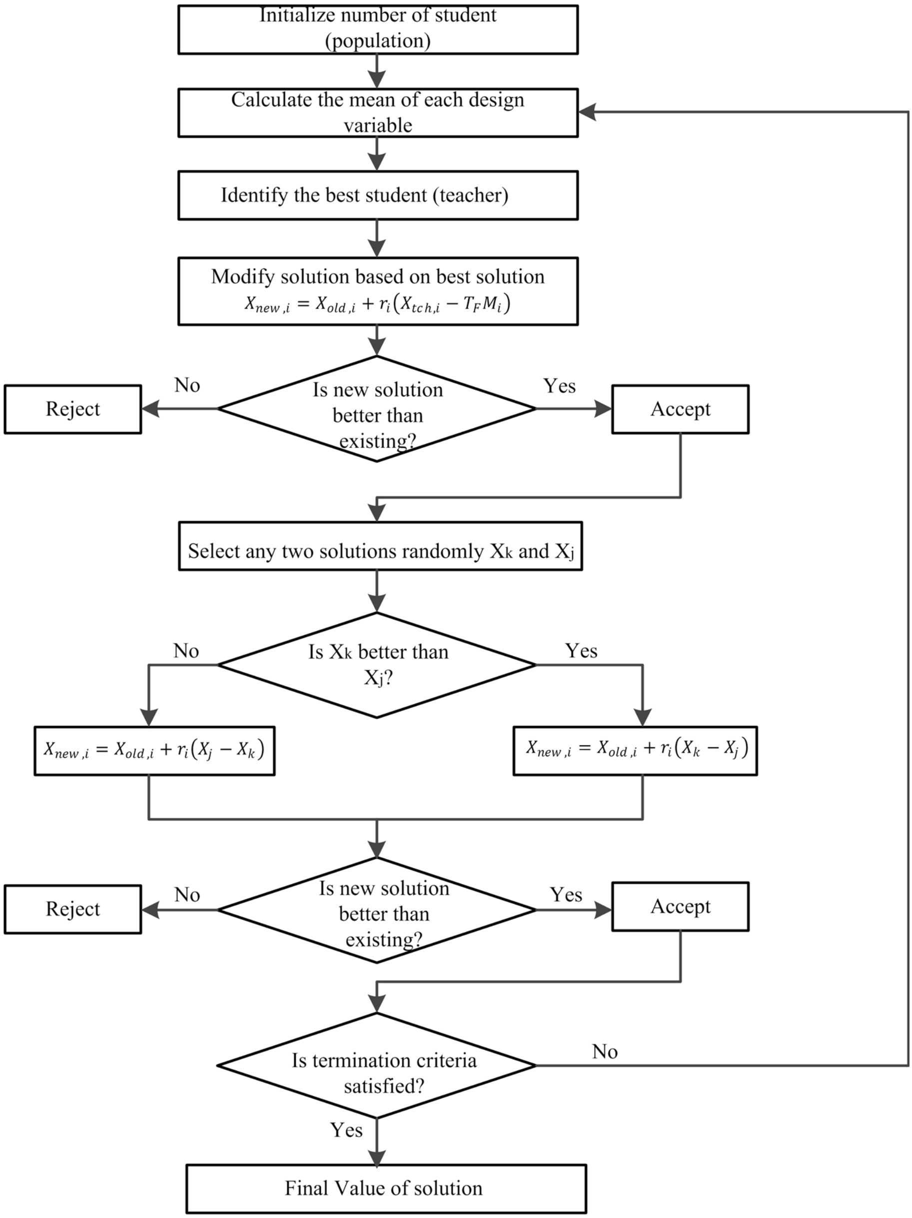


Fig. 7 The flowchart of the TLBO algorithm

The maximum and minimum values of inputs, which are related to the W and L of transistors, are achieved experimentally, because in this range, the outputs (power, output ripple and output voltage) are gained properly for regulator. For having low power dissipation, the maximum values of $V_{in,low}$ and $V_{in,high}$ inputs are considered same as those of Ref. [7]. The regulator not only has the lower power consumption, but also has the appropriate operation even with lower supply voltage. In addition for the best comparison

Table 2 The maximum and minimum defined inputs and outputs in TLBO algorithm

	$L_{M_{p,pass}}$ (μm)	$L_{M_{R1}}$ (μm)	$L_{M_{R2}}$ (μm)	$W_{M_{p,pass}}$ (μm)	$W_{M_{R1}}$ (μm)
Min	0.18	0.18	0.18	3	0.22
Max	1	6	6	8	6
	$W_{M_{R2}}$ (μm)	$(W/L)_{M_{L1}}$	$(W/L)_{M_{L2}}$	$(W/L)_{M_{L3}}$	$(W/L)_{M_{L4}}$
Min	0.22	1	1	1	1
Max	7	17	17	17	17
	$(W/L)_{M_{L5}}$	$(W/L)_{M_{L6}}$	$(W/L)_{ML7}$	$(W/L)_{ML8}$	$V_{in,low}$ (V)
Min	1	1	1	1	0.2
Max	17	17	17	17	0.5
	$V_{in,high}$ (V)	V_{out} (V)	V_{ripple} (V)	P_{diss} (μW)	
Min	1.2	0.8	0.002	100	
Max	1.5	0.82	0.005	150	

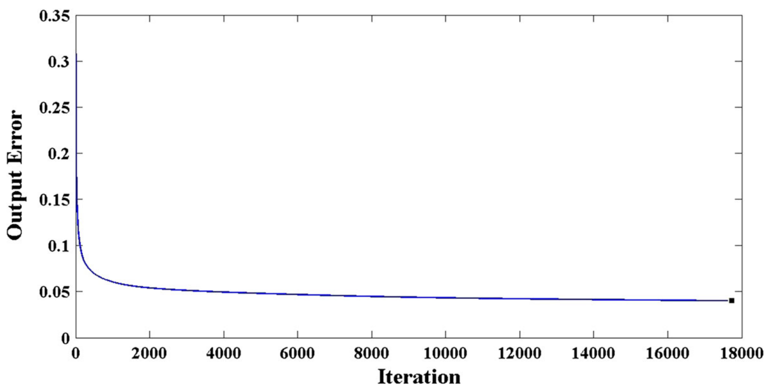


Fig. 8 The error curve of the achieved function from neural network based on the iteration

of the results before and after using TLBO algorithm, V_{out} is considered same as the one of Ref. [7].

In the presented algorithm the output is the multi-objective function. On the other hand the optimization is done based on the minimum output. Thus in order to optimize all three outputs, the weighted summation like Eq. (8) is used. In this case the output is achieved as one objective function.

$$F = \sqrt{\left(\frac{0.8}{Z_1}\right)^2 + \left(\frac{Z_2}{0.005}\right)^2 + \left(\frac{Z_3}{150}\right)^2} \tag{8}$$

The achieved results from the neural network and TLBO algorithm and also the comparison of the outputs simulations before and after using TLBO algorithm are evaluated in the following sections.

4 Simulation and Comparison Results

4.1 The Simulation Results of Neural Network

The error curve of the achieved function from the training step, based on the iteration in the done simulation, is shown in Fig. 8. As it is clear from the figure, generally by increasing the iteration the error is decreased and the value of error reaches to 0.04 in the 1774th iteration. Table 3 presents the mean and maximum errors related to the testing step, for the three considered outputs. The worst error is related to the output voltage ripple that the mean and maximum of this error are 7.72 and 24.41 %, respectively.

4.2 The Simulation Results of TLBO Algorithm

In Table 4 the results achieved from the TLBO algorithm that is related to the defined inputs are shown with the used values in the present design and the proposed regulator in Ref. [7].

By comparing the data related to the TLBO output and the used values in the proposed design, it is clear that the most used inputs in the proposed design almost similar to the output of TLBO algorithm just with a minimum error.

Table 3 The mean and maximum errors related to the testing step for three outputs

	V_{out}	V_{ripple}	P_{diss}
MeanError (%)	2.21	7.72	3.32
MaxError (%)	6.93	24.41	10.73

Table 4 The achieved results from TLBO algorithm, the used values in the proposed circuit and Ref. [7]

	TLBO algorithm output	Designing value of this paper	Designing value without TLBO ([7])
$L_{M_{p,pass}}$ (μm)	0.99	1.025	0.59
$L_{M_{R1}}$ (μm)	2.42	2.45	5
$L_{M_{R2}}$ (μm)	1.37	1.37	0.18
$W_{M_{p,pass}}$ (μm)	6.85	6	4
$W_{M_{R1}}$ (μm)	2.32	2.45	5
$W_{M_{R2}}$ (μm)	6.58	6.57	3.4
$(W/L)_{M_{L1}}$	13.86	13.88	11.11
$(W/L)_{M_{L2}}$	5	4.16	11.11
$(W/L)_{M_{L3}}$	13.26	13.33	11.11
$(W/L)_{M_{L4}}$	4.98	5	11.11
$(W/L)_{M_{L5}}$	2.64	2.66	11.11
$(W/L)_{M_{L6}}$	10.41	10.55	11.11
$(W/L)_{M_{L7}}$	15.86	15.83	11.11
$(W/L)_{M_{L8}}$	4.13	4.11	11.11
$V_{in,low}$ (V)	0.28	0.3	0.5
$V_{in,high}$ (V)	1.37	1.4	1.5

4.3 The Simulation Results of the Proposed Regulator

Figure 9 shows the optimized regulator output. The output is about 800 mV and its ripple is 1.39 mV. Therefore the LIR value of this circuit equals to 6.95(mV/V).

The Monte Carlo simulation of the regulator output is shown in Fig. 10 for process variations and mismatch, by 500 times run. The average value (μ) and standard deviation

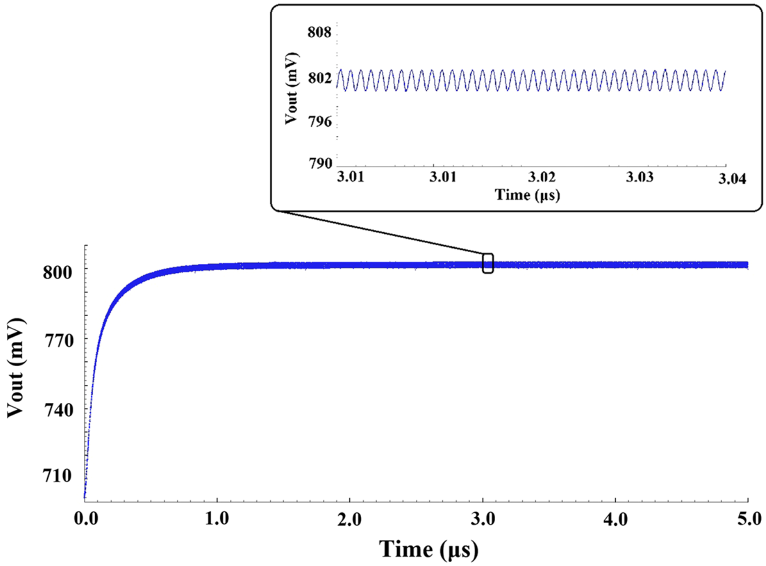


Fig. 9 The optimized regulator output voltage

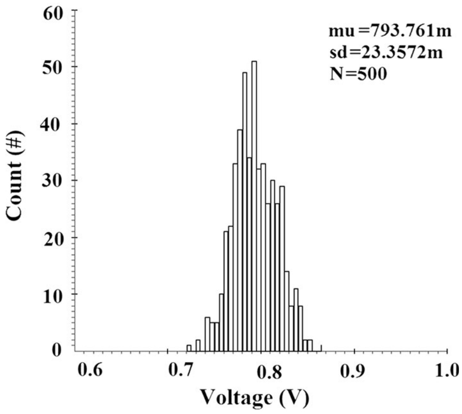


Fig. 10 The regulator output of the Monte Carlo simulation for the process variation and mismatch

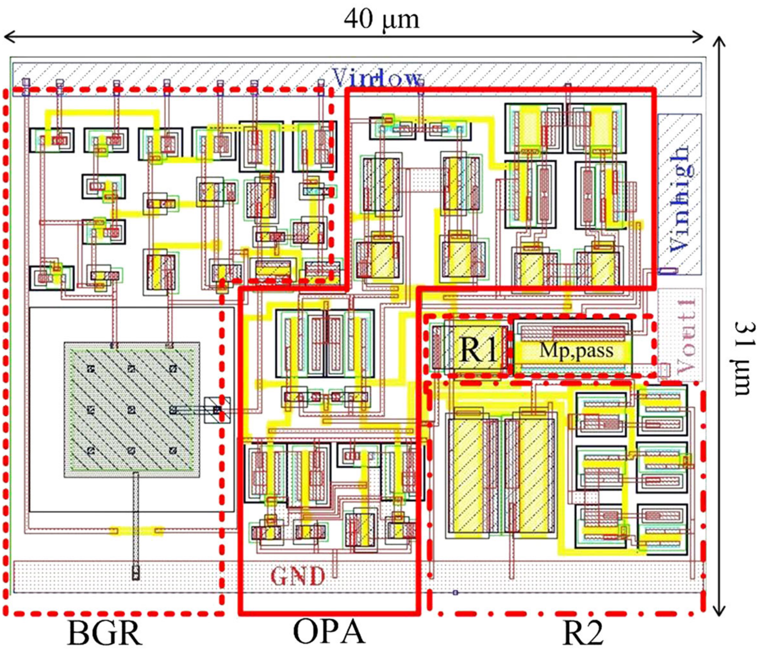


Fig. 11 The layout of the complete proposed voltage regulator

Table 5 The comparison of different parameters of the proposed regulator with Ref. [7] and two other voltage regulator

	This work	[7]	[3]	[5]
Technology (µm)	0.18	0.18	0.35	0.18
$V_{in,1}$ @ $\Delta V_{in,1}$ (V)	0.3 @ 0.1	0.5 @ 0.1	–	–
$V_{in,2}$ @ $\Delta V_{in,2}$ (V)	1.4 @ 0.4	1.5 @ 0.4	2.2 @ –	– @ 0.4
V_{out} (V)	0.8	0.81	1	1.5
ΔV_{out} (mV)	2.78	3	–	7
Efficiency (%)	57.14	53.33	45.45	–
I_L (μA)	0.8	80	500	–
$I_{quiescent}$ (μA)	0.29	27	35.5	–
P_{diss} (µW)	115	147	1200	–
LIR (mV/V)	6.95	7.5	39	12
PSRR (dB)	42.88	42.5	38	35.1
Freq (MHz)	960	960	10	1
Chip area (mm^2)	0.00124	0.00125	–	–

(σ) equal to 793.76 and 23.36 mV, respectively. Consequently the variation coefficient (σ/μ) is achieved 2.9 %.

Figure 11 shows the layout of the designed voltage regulator. The total area occupied by this circuit is $31 \times 40\,\mu m^2$.

Table 5 compares the different parameters of the proposed regulator with that of circuit of Ref. [7] and the two other voltage regulators. As it is clear the output voltage of the designed regulator is similar to the output voltage of the presented regulator in Ref. [7], while the output ripple of the optimized circuit is decreased. Due to the fixed ripple of the input voltage, LIR is also decreased. On the other hand the power dissipation and the steady current are ameliorated in compare with that of circuit of Ref. [7]. In addition the designed regulator has the more improved power dissipation, voltage efficiency and LIR than the other regulator ([3] and [5]). The other parameters of the circuit have the appropriate value.

5 Conclusion

In this paper the regulator, which is supplied from the elementary and extremity stages, is designed and optimized for RFID applications. The optimization is done with TLBO algorithm. 16 inputs and 3 outputs, V_{out}, ΔV_{out} and P_{diss}, are used in this algorithm and for optimizing the multi-objective function, weight summation of three outputs is employed. Based on the achieved results, by considering the fixed output voltage and load, the power dissipation is attenuated about 32 μW and reached to 115 μW. in addition, the values of steady current and LIR equal to 290 nA and 6.95 mV/V, respectively. The chip area of the design is 0.00124 mm^2 in 0.18 μm CMOS.

References

1. Yao, Y., Wu, J., Shi, Y., & Dai, F. F. (2009). A fully integrated 900-MHz passive RFID transponder front end with novel zero-threshold RFDC rectier. *IEEE Transactions on Industrial Electronics*, *56*(7), 2317–2325.
2. Balachandran, G. K., & Barnett, R. E. (2006). A 110 nA voltage regulator system with dynamic bandwidth boosting for RFID systems. *IEEE Journal of Solid-State Circuits*, *41*(9), 2019–2028.
3. Cesar, P., Crepaldi, C., Pimenta, T. C., Moreno, R. L., & Rodriguez, E Ch. (2012). A low power CMOS voltage regulator for a wireless blood pressure biosensor. *IEEE Transactions on Instrumentation and Measurement*, *61*(3), 729–739.
4. Lee, M. Ch., Hu, Ch. Ch., & Lin., Z. W. (2012). Implementation of low dropout regulator with low bandgap reference voltage circuit for RFID tag applications. In *Cross strait quad-regional radio science and wireless technology conference (CSQRWC)*, pp. 40–43.
5. Liu, C. E., Hsieh, Y. J., & Kiang, J. F. (2010). RFID regulator design insensitive to supply voltage ripple and temperature variation. *IEEE Transactions on Circuits and Systems-II: Express Briefs*, *57*(4), 255–259.
6. De Vita, G., & Iannaccone, G. (2006). Ultra-low-power series voltage regulator for passive RFID transponders with subthreshold logic. *Electronics Letters*, *42*, 1350–1351.
7. Salehi, M. R., Dastanian, R., Abiri, E., & Nejadhasan, S. (2015). A 147 μW, 0.8V and 7.5 (mV/V) LIR regulator for UHF RFID application. *International Journal of Electronics and Communications (AEU)*, *69*(1), 133–140.
8. Magnelli, L., Crupi, F., Corsonello, P., Pace, C., & Iannaccone, G. (2011). A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference. *IEEE Journal of Solid-State Circuits*, *46*(2), 465–474.
9. Anvesha, A., & Baghini, M. Sh. (2013). A Sub-1V 32 nA process, voltage and temperature invariant voltage reference circuit. In *IEEE 12' th international conference on VLSI design and 26th international conference on embedded systems (VLSID)*, pp. 136–141.
10. Ma, H., Zhou, F. (2009). A Sub-1V 115 nA 0.35 μm CMOS voltage reference for ultra low power applications. *IEEE 8' th International conference on ASIC*, pp. 1074–1077.
11. Wilson, W., Chen, T., & Selby, R. (2013). A current-starved inverter-based differential amplifier design for ultra-low power applications. In *IEEE 4' th Latin American symposium on circuits and systems (LASCAS)*, pp. 1–4.

12. Lopez-Martin, A. J., Baswa, S., Ramirez-Angulo, J., & Carvajal, R. G. (2005). Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency. *IEEE Journal of Solid-State Circuits*, *40*(5), 1068–1077.
13. Bernal, M. R. V., Celma, S., Medrano, N., & Calvo, B. (2012). An ultralow-power low-voltage class-AB fully differential OpAmp for lond-life autonomous portable equipment. *IEEE Transactions on Circuits and Systems-II*, *59*(10), 643–647.
14. Dejhan, K., Suwanchatree, N., Prommee, P., Piangprantong, S., & Chaisayun, I. (2004). A CMOS voltage-controlled grounded resistor using a single power supply. *IEEE ISCIT*, *1*, 124–127.
15. Rao, R. V., Savsani, V. J., & Vakharia, D. P. (2011). Teaching-learning-based optimization: A novel method for constrainedmechanical design optimization problems. *Computer-AidedDesign*, *43*, 303–315.

Ebrahim Abiri received the B.Sc. degree in Electronics Engineering from Iran University of Science and Technology (IUST) in 1992, M.Sc. degree from Shiraz University in 1996 and the Ph.D. degree in electronic from Iran University of Science and Technology (IUST) in 2007. He has authored more than 50 published technical papers in electronics and power electronics and 4 books. He has been with the Department of Electrical Engineering, Shiraz University of Technology (SUTECH), since 2007. His current research activities include analog circuit design and power electronic.

Rezvan Dastanian was born in Iran, Ahvaz, in 1986. She received the B.Sc. and M.Sc. degrees in electrical engineering from Iran University of Science and Technology (IUST), Iran, Tehran in 2008 and 2011 respectively and is currently working toward the Ph.D. degree in electrical engineering at Shiraz University of Technology (SUTECH). Her research interests include RFIC design, low power circuit design, sensor, DC–DC converter and microelectronics.

Mohammad Reza Salehi received the B.Sc. degree in electrical engineering from Amirkabir University of Technology (Tehran Polytechnique), Tehran, the M.Sc. degree in electrical engineering from Shiraz University, Shiraz, Iran, and the Ph.D. degree in opto-electronics at the ENSERG/INPG, France. He has authored and co authored over 70 journal and conference papers and 7 books. He is currently a Member of IEEE. My research interests include optoelectronics, optomicrowaves and optical systems.

Sajad Nejadhasan was born in Iran, Bushehr, in 1987. He received the B.S. degree in the department of engineering from Persian Gulf University in 2011 and is currently working toward the M.Sc. degree in electrical engineering at Shiraz University of Technology (SUTECH). His research interests include design of power management block in RFID tags.