Controllable Current and Voltage Power sources using FPGA

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Abstract: This paper deals with the development and design of digitally controllable, three-phase current and voltage power sources. The main, digitally controlled parameters of the power source are frequency, phase-shift and amplitudes of two separate sine-wave systems. Possibilities and means of implementation are discussed and a verified solution is described. The reason why this development was done is the lack of power sources on the market. The three-phase voltage and the tree-phase current systems are isolated by power transformers. Among many possibilities of voltage and current control, the method based on direct digital synthesis was selected. Control circuits of the power sources are described in VHDL and implemented in an FPGA device.

Keywords: VHDL, programmable logic array, FPGA, voltage source, current source, direct digital synthesis, DDS

1. INTRODUCTION

This work deals with the design of numerically controlled three-phase voltage and current sources. The main requirement is the independent controllability and mutual phase-shift adjustability of the two three-phase systems. At present there are several companies that produce similar devices. Still, it is very difficult to find a power source on the market that satisfies the requirements for technical parameters. Professionally produced power sources are very expensive, unique devices. There are many needs for AC sources usage, such as setting of power equipment parameters, testing of over-current protection relays, etc.. The motivation for our research was designing a controllable power source that can be used as a component of a real-time simulator of a synchronous generator behavior. The outputs of these power sources are three-phase signals representing the output voltage and output current of a synchronous generator. In order to connect the power sources in a feedback, the system also includes digital and analog inputs and outputs compatible with the excitation regulator input and output circuits.

1.1 Required parameters

The required parameters of the power sources are: voltage, adjustable in the range from 0 to 120 volts RMS and current, adjustable in the range from 0 to 8 amperes RMS. The frequency range is adjustable from 40 to 90 Hz; the phase-shift must be adjustable in the range from 0 to 360°. The control of power sources is done via PC. The basic step in the output voltage is 0.1 volt, the basic step in the output current is 0.01 ampere, the basic step in the phase-shift is 0.01°, and the basic step in the frequency is 0.0001 Hz. The described sources are part of the simulator of three-phase synchronous generators.

The system also includes:

- a single-phase AC voltage source with independently adjustable amplitude (from 0 to 120 V RMS with 0.1 V resolution) and with independently adjustable frequency (40 to 90 Hz with a resolution of 0.0001 Hz). This power source simulates the voltage and frequency in one phase of a distribution system and makes it possible to simulate synchronization.

- four independent DC voltage sources

- one analog input

- sixteen digital inputs, and sixteen digital outputs

2. POSSIBILITIES OF IMPLEMENTATION

There are two basic approaches:

- higher-power supply sources
- lower-power supply sources

By a “higher” power supply voltage is meant the voltage whose DC value exceeds the maximum value of the required output AC voltage. When using this concept, each individual phase voltage (or current) source must be galvanically separated. One possible design of electrical insulation of a three-phase power source from the network is shown in Fig. 1. The picture shows a design with power supplies (PS + Source) individually isolated from others and from the power network (PN). The design of the three-phase current sources, individually isolated, would look alike. Independent power

supplies with electrically separated secondary sections are used. Another possibility is to use a transformer with electrically separated windings. Essential and probably the only advantage of this concept is the possibility of generating a very low-frequency or even a DC output voltage/current.

The main disadvantages of this approach include:

-more difficult power system design

-the necessity of higher voltage components in the power circuit. It means a limited choice of components and significantly higher price.

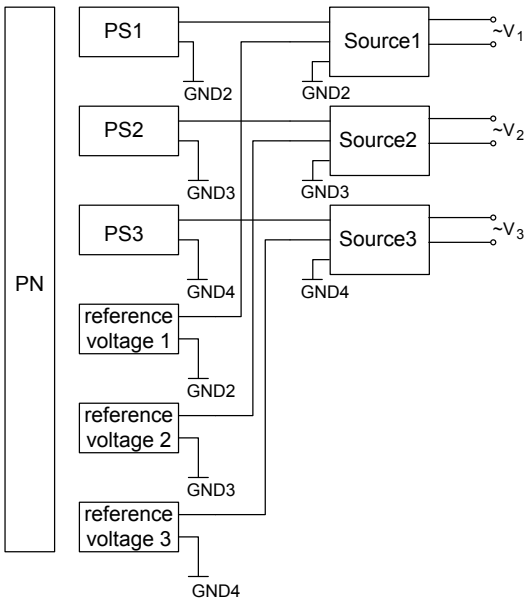

Fig. 1. Three-phase voltage source with galvanic separation (PN – power network, PS – power source)

By a "lower" supply voltage is meant the voltage whose DC value is smaller than the maximum value of the desired output voltage. In this concept, it is possible to use a common power supply. The method of the galvanic separation of the three-phase sources with a common power supply is shown in Fig. 2. The design of the three-phase current sources would look alike. In this case, it is not necessary to isolate the reference voltage sources. The main advantage of this concept is the use of only one low-voltage DC power supply, simpler design, and better availability of low-voltage components with lower costs.

The main disadvantages of this approach include:

- necessity of the galvanic separation of feedback circuits

- restricted lower limit of the output frequency and increased demands on the output transformer size and its price

- necessity to eliminate the DC voltage at the output of the amplifiers

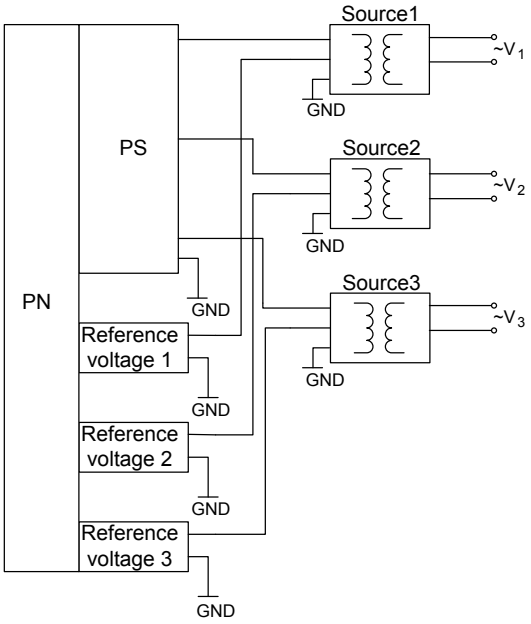

Fig. 2. Three-phase voltage source with galvanic separation of common power supply (PN – power network, PS – power source)

As the result of the above analysis, the second described approach, i.e. the lower power supply voltage, was chosen.

3. SOLUTIONS OF CIRCUITS

3.1 Alternating voltage regulator

The principle of voltage sources is shown in Fig. 3. The feedback loop is isolated by a voltage measuring transformer.

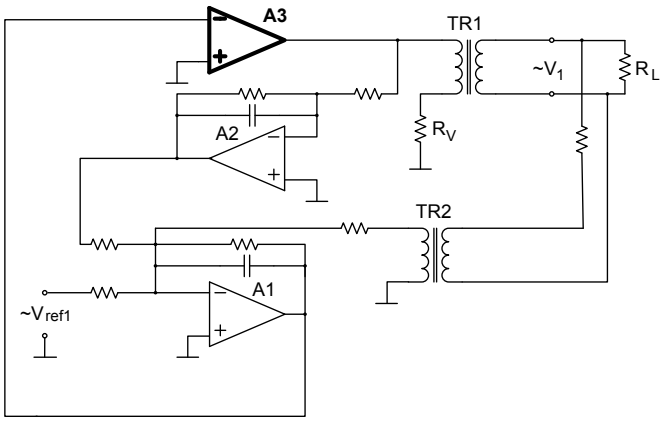

Fig. 3. Alternating voltage regulator

Other possibility of the feedback isolation might be an isolation amplifier. In this case it is necessary to electrically separate the amplifier power supply using a DC/DC

converter. This option would require more complicated circuit solution; it would be less reliable and probably more expensive. Therefore, this solution was not considered. The acceptable types of power amplifiers are only those operating in the Class B or in the Class D. The Class D amplifier was chosen because of its superior efficiency. The current regulator was designed in a similar way. Its principle is shown in Fig. 4. The feedback is derived from an output current using a current transformer. The required parameters are adjusted at the reference inputs V_{ref}.

3.2 Alternating current regulator

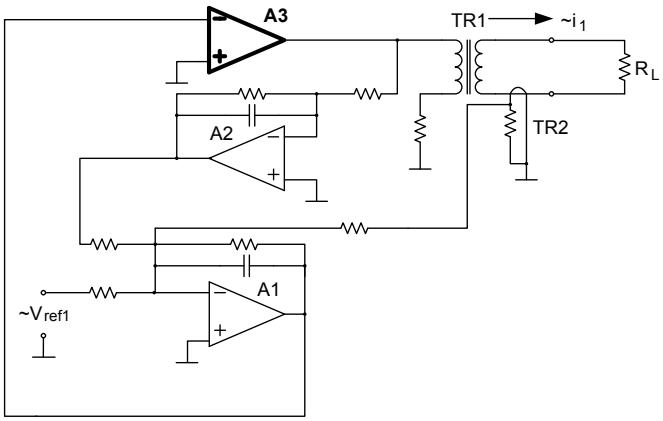

Fig. 4. Alternating current regulator

3.3 Reference voltage sources

The main requirements on the reference voltage source are the digital frequency adjustability in the frequency range from 40 to 90 Hz with a resolution 0.0001 Hz, digital phase shift adjustability in the range from 0 to 360° with a resolution 0.01°, and independent setting of the amplitude. In real-time applications, the parameters should be changed continuously every millisecond. Considering these requirements it is necessary to use the principle of generation of digital signal samples and their subsequent conversion into an analog form by D/A converters.

3.4 Digital signal generator

Digital samples can be generated directly in real time by calculating the trigonometric functions or by using the principle of direct digital synthesis. Especially with regard to minimum design time, the direct digital synthesis method was chosen. The block diagram of the units used in DDS method is shown in the Fig. 5. The direct digital synthesis is a method that allows creating the frequency- and phase-modulated signal. The generator is composed of the following blocks: precise source of the synchronization signal with constant frequency, memory for a look-up table containing the signal samples, D/A converters, digital logic which addresses the memory using the synchronization signal, and the unit generating required output signal parameters. Only one period of signal is usually stored in the memory; a quarter of period is sufficient for the sinusoidal signal.

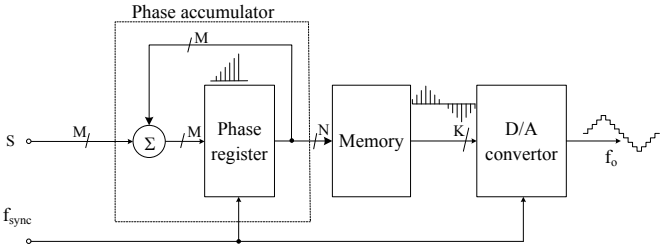

Fig. 5. DDS logic block diagram

The addresses of memory cells are generated by the phase accumulator. The phase register with the synchronization signal f_{sync} works as a M-bit counter incremented by number S which was preset. The dependence of the output frequency on the preset number S can be expressed as:

$$f_o = \frac{S \cdot f_{sync}}{2^M} \tag{1}$$

The frequency resolution can be expressed as:

$$\Delta f = \frac{f_{sync}}{2^M} \tag{2}$$

The DDS method includes several sources of noise which produce undesirable spectral lines. Only N upper bits of the phase accumulator are used for memory addressing (see Fig. 5). The rest (M-N) of the phase accumulator bits are ignored. Reduction of the phase accumulator bits decreases the size of the memory. Finite address resolution causes quantization distortion of the phase in the time domain. This distortion is periodic and it appears as spectral lines (called spurs [Cordesses, 2004]) in the frequency domain. A difference between the output frequency and maximum level of spurs is dependent on the number of phase accumulator bits (M), number of address bits (N) and value of preset number S. No quantization distortion appears when the greatest common divisor of preset number S and 2^{M-N} is equal to 2^{M-N}. On the other hand, the maximum quantization distortion appears when the greatest common divisor of preset number S and 2^{M-N} is equal to 2^{M-N-1}. The maximum quantization distortion causes maximum level of phase truncation spurs S_{MAX} in the frequency domain. Other values of preset number S yield spurs lower then maximum spurs S_{MAX}. Maximum level of spurs (called SFDR – "spurious free dynamic range") can be expressed as:

$$S_{MAX} = -SFDR = -6.02 \cdot N[dB] \tag{3}$$

This equation is true only if $M - N \geq 4$. This condition is met for any practical DDS design [Kroupa, 2000]. Finite resolution of D/A converter (K-bits) causes quantization distortion of amplitude in the time domain (see Fig. 5).

Noise-to-signal ratio as a result of quantization distortion can be expressed as:

$$NSR = -SNR = -6.02 \cdot K - 1.761[dB] \qquad (4)$$

3.5 Control unit of power sources

In order to meet the requirements defined in chap. 1.1, it is necessary to use hardware with large amount of inputs and outputs controlled at the same time. Integrated circuits for the direct digital synthesis implementation exist. They are usually optimized for radio-electronics. They are not suitable for the design of the controlled low-frequency AC sources. As a core of the control unit, a programmable logical array was chosen. The control module was designed and manufactured with the FPGA EP1C6 Cyclone circuit. This module is interconnected via two 50-pin connectors with the basic control plate. The selected FPGA circuit meets the requirements for the number of parallel inputs/outputs and meets the requirements for the size of the memory and calculation power. The block diagram of the control unit is shown in the Fig. 6. The photo of the control unit is in the Fig. 7.

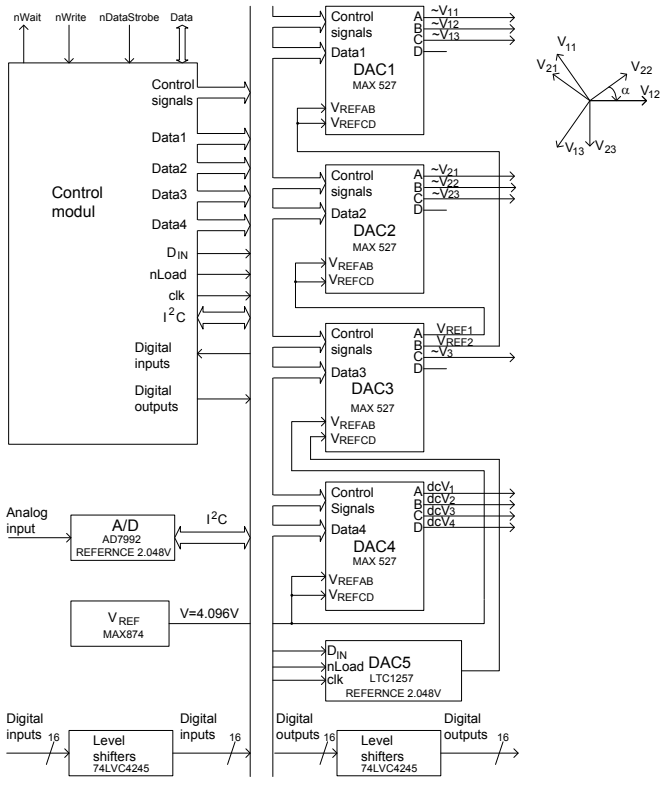

Fig. 6.Control unit block diagram

The sinusoidal signal samples are stored in the memory of the control module. The main function of this module is the DDS implementation and generation of control signals for the D/A converter. The parameters of the reference voltage sources are transferred from the control computer via the parallel printer port in EPP (Enhanced Parallel Port) mode. The schematic diagram of the source module (see Fig. 6) shows the converters DAC1, DAC2, DAC3 as reference voltage sources. MAX 527 circuits were selected. The converter MAX 527 contains four 12-bit D/A converters (named A, B, C, D). The amplitudes of the converter output voltages are derived from the reference voltage V_{REFAB} which is common for converters (A) and (B) or V_{REFCD} common for converters (C) and (D). Change of the amplitude is achieved by changing V_{REFAB} or V_{REFCD} voltage generated by the DAC3 converter. The output voltage V_{REF2} of DAC3 represents the amplitude of the first three-phase system named V_{11}, V_{12}, V_{13} (generated by the converter DAC1). Converter DAC3 output voltage V_{REF1} represents the amplitude of the second three-phase system named V_{21}, V_{22}, V_{23} (generated by the converter DAC2). The DAC3 output voltages V_{REF1} and V_{REF2} which represent the amplitude of the three-phase system are derived from the source of precise reference voltage 4.096 V (circuit MAX874).

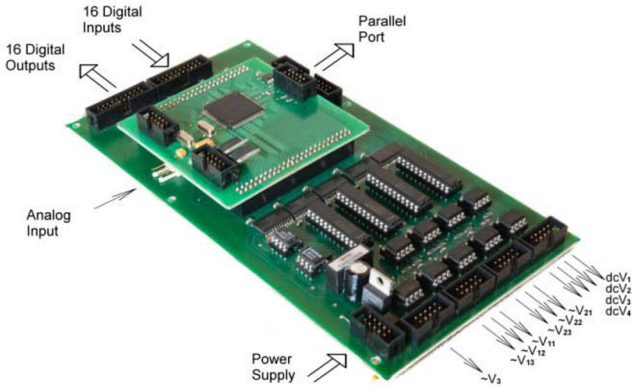

Fig. 7. Control unit photo

The voltage V_3 is an independent AC reference voltage generated by DAC3 converter. The amplitude of voltage V_3 is derived from the reference voltage V_{REFCD}. The voltage V_{REFCD} is set by the DAC5 converter output. As the DAC5 converter a LTC1257 circuit is used. This circuit contains one 12-bit D/A converter with a serial interface. The V_3 voltage source allows setting a voltage and frequency independently from the three-phase reference voltages systems. This source can be synchronized with the three-phase systems. The synchronization starts when the synchronization request is received from the control PC. Other parts of the source control unit are four adjustable DC voltages dcV_1, dcV_2, dcV_3, dcV_4. These four adjustable DC voltages are generated by a converter DAC4 (MAX527). The DAC4 output voltages are derived from the precise source of reference voltage 4.096 V (MAX874). As an analog input the circuit AD7992 is implemented. The circuit AD7992 contains one dual-channel A/D 12-bit serial (I2C) interfaced converter. One input of this converter is used as an analog input of the control unit. The second input of the converter is used as a reference input; it is connected with the source of precise reference voltage 2.048 V (circuit LTC1257).

3.6 Implementation in VHDL

The block diagram of the control unit designed with an FPGA is shown in Fig. 8. A table of sine wave signal values for the first three-phase system (V_{11},V_{12},V_{13}) is stored in a memory block ROM1, a table of sine wave signal values for the second three-phase system (V_{21},V_{22},V_{23}) is stored in a memory block ROM2. Both tables include 3072 values of sine wave signal. The number 3072 is the greatest number which is both divisible by three and less than 2^{12}. This number was chosen for the precise calculation of the phase shifts between single phases. Only a quarter of sine wave signal period is saved in the memory block ROM1 or ROM2 in order to reduce the necessary memory size. Generation of other samples is done by calculation in the block Control. Parameters of the power source control unit are transmitted from the PC to the EPP mode block via a parallel port. The received data port is saved in sixteen registers. The registers of amplitudes of the two three-phase systems are transformed into the data signal (data3) for the D/A converter DAC3. Addresses for memories ROM1 and ROM2 are calculated in the Control block using the value from the phase shift register and the frequency register 1.

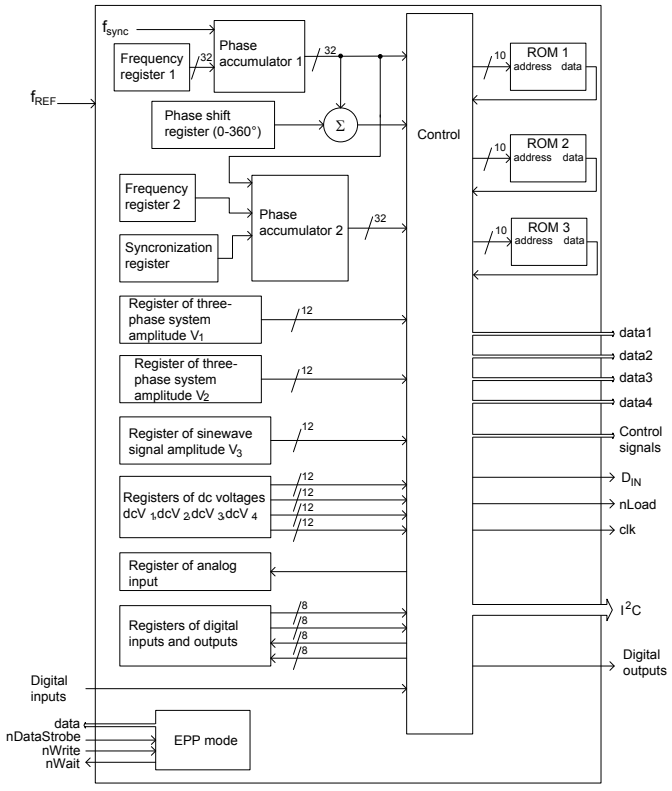

Fig. 8. Control unit – block diagram of FPGA design

Maximum output frequency depends on required resolution in time (i.e. 3072 samples) and characteristics of the D/A converter. Minimum timing characteristics of D/A converter write-cycle and output settling time of D/A converter restrict maximum speed of output voltage modification. D/A converter MAX 527 was used. Maximum frequency of setting output value of MAX 527 D/A converter is 444kHz. This frequency is used as synchronization signal of the phase accumulator 1. Maximum output frequency can be expressed as:

$$f_{MAX} = \frac{f_{sync}}{3072} = \frac{444 \cdot 10^3}{2^{32}} = 144Hz \qquad (5)$$

The dimension of the phase accumulator 1 is 32 bits. Frequency resolution can be expressed as:

$$\Delta f = \frac{f_{sync}}{2^M} = \frac{444 \cdot 10^3}{2^{32}} = 0.0001Hz \qquad (6)$$

The dimension of the phase shift register is 16 bits. Resolution of the phase shift can be expressed as:

$$\Delta f = \frac{360}{2^{16}} = 0.01° \qquad (7)$$

Parameters of the independent AC voltage source V_3 are saved in two registers – frequency register 2 and register of sine wave signal amplitude V_3. The independent source of AC voltage can be synchronized with three-phase systems. The requirement for synchronization is saved in the synchronization register. The samples of the sine signal V_3 are stored in the memory block ROM3. Address for the memory ROM3 is calculated in the Control block using the frequency register 2, the synchronization register and the output value from the phase accumulator 1. Organization of the memory ROM3 is the same as organization of the memories ROM1 and ROM2. Consequently the values of maximum frequency, frequency resolution, and phase shift resolution are the same. Register of the sine signal amplitude V_3 is transformed into the data signals (DIN, nLoad a clk) for D/A converter DAC5 (see Fig. 6).

The values of DC voltages are saved in registers dcV_1, dcV_2, dcV_3, dcV_4. Registers of DC voltages are transformed into data signals for the D/A converter DAC4.

A sequential algorithm for A/D converter (AD7992) read-cycle is implemented in the control block. The result of A/D conversion is saved in a register of analog input.

4. VERIFICATION AND MEASUREMENT

4.1 FPGA design

Design of the control unit was written in VHDL language. Final design was synthesized to FPGA device Cyclone EP1C6. The design contains 1666 logic elements (28%), 27648 bits of on-chip memory (30%). 91 input and output pins (93%) are controlled.

4.2 Test application

In order to test the source control unit, special software applications were developed to allow setting the parameters using PC (see Fig. 9). The application provides a comfortable

environment to set the individual parameters of the control unit. It allows a common setting of all the controllable source parameters which are stored in the initialization file. After the required parameters setting, all the control unit registers parameters are calculated and transferred in the control unit via the parallel port.

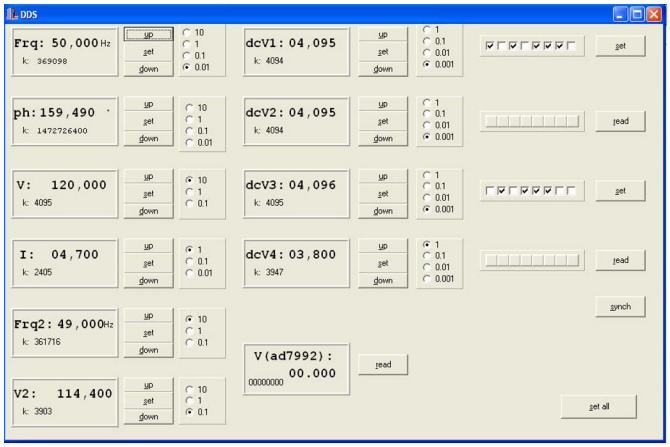

Fig. 9. Test application

The frequency spectrum was measured for the output frequency 60 Hz (see Fig. 10).

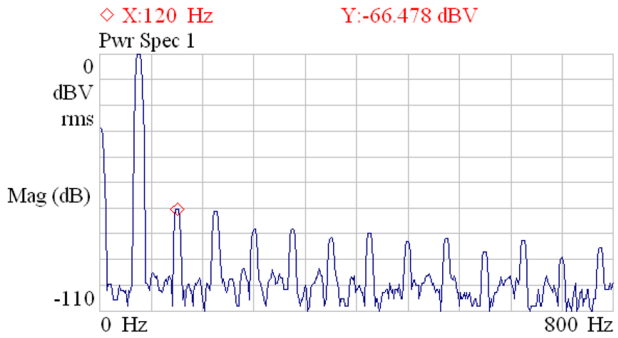

Fig. 10. Spectrum of output signal 60Hz

The measurement was performed for the maximum value of the reference voltage. The low-frequency spectrum analyzer Agilent 35670A was used. The measured range was chosen from 0 to 800Hz. The measured level of signal-to-noise ratio is 66 dB.
The noise-to-signal ratio as a result of quantization distortion of amplitude can be expressed as:

$$NSR = -SNR = -6.02 \cdot K - 1.761 \\ = -6.02 \cdot 12 - 1.761 = -74dB \quad (8)$$

where K is a number of D/A converter bits.

The maximum noise-to-signal ratio as a result of quantization distortion of phase can be expressed as:

$$S_{MAX} = -SFDR = -6.02 \cdot N = -6.02 \cdot 11.6 \\ = -69.7dB \quad (9)$$

where N is an effective number of address bits.

5. CONCLUSIONS

The requirements specified in Chap. 1.1 were achieved. The first version of controllable current and voltage power sources was developed and verified. The control unit and the test application can be used as a laboratory current and voltage power source or as a component of a real time synchronous generator simulator. The measured level of voltage source efficiency is 87 %. The measurement was performed for 50 % input value and maximum load. The measured level of current source efficiency is 86 %. The measurement was performed for 50 % load value. The following development in this field should aim to increasing the power sources efficiency. The connection of the control unit to the control computer could be done via USB.

REFERENCES

Cordesses, L. (2004). Direct Digital Synthesis: A Tool for Periodik Wave Generation. *IEEE signal processing magazine.*

Kroupa, V., Čížek, V., Štrusa, J., Švandová, H. (2000). Spurious signals in direct digital frequency synthesizers due to phase truncation. *IEEE Trans. on Ultrason., Ferroelect., and Freq. Contr.*, vol. 47, no.5, pp.1166-1172.