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Full Length Article

Analysis and implementation of impedance source based Switched Capacitor Multi-Level Inverter

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ABSTRACT

In recent years, a numerous Multi-Level Inverter (MLI) topologies are proposed with reduced number of switches and control complexity. An Impedance source based MLI structure with ability of additional boost is proposed in this work. The proposed topology requires one source, one impedance network and reduced number of switches when compared to recently reported inverter literature. Due to Self-voltage Balancing circuit (SBC), the fixed boost of 1.5 times the input and equal voltage across all the capacitors are achieved. An additional boost is obtained by placing impedance network between input source and SBC. The proposed Inverter is compared with existing topologies with respect to a number of sources, number of impedance networks, control switches, voltage balancing and boost capability. A simple level shifted based sinusoidal pulse width modulation technique is adopted for generating gate pulses. Further theoretical analysis and computer aided simulation results are validated with the experimental results.

1. Introduction

Novel MLI topology has significant advancement in the field of power electronics, because of numerous advantages over conventional inverters. The conventional two level inverters are facing difficulty in meeting present scenario. The most popular conventional MLI structures are: Diode Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI) and Cascaded H Bridge MLI (CHMLI) [1–3]. In DCMLI, (n-1) capacitors are used as potential dividers, the voltage unbalancing across these capacitors is a serious concern. Additionally, it requires (n-1)(n-2) clamping diodes. For FCMLI, (n-1)(n-2)/2 bulky capacitors are required. In CHMLI, separate sources are required for each H Bridge and each bridge produces three levels. These H Bridges are connected in series for generating the required number of levels in output voltage where n is number of levels in output waveform.

A numerous MLI topologies are proposed to address the drawbacks of conventional MLI's. In recent years the focus is made on:

Increasing the number of levels in output with asymmetrical voltage sources as reported in [4–6]. These inverters require more than one source with different voltage magnitudes. To obtain different voltages, different turn's ratio transformers are used. The asymmetrical MLI requires DC sources with different magnitudes and switches of different rating.

A few topologies are proposed by reducing the number of switches [4,7–9] and sources [10–12]. To reduce the number of input sources, series connected capacitors are used as a potential dividers. To achieve balanced voltage across all DC-link capacitors, a separate feedback circuit is used [13,14]. Inverter circuit will become complex due to this approach.

With the conventional or transformer based MLI's [15–18], in case of any shoot through or miss gating, entire circuit will get damaged. The cost and losses increases due to transformer present in the circuit.

In aforementioned topologies, the maximum available voltage is limited by the input or DC link voltage. In applications like: Photovoltaic system, Electrical vehicles, Dynamic voltage restorer, etc. requires both boost and buck operations [19]. To meet this normally DC-DC converter or Z Source Inverter (ZSI) is used. If a DC-DC converter or Z Source network is integrated with MLI, then separate DC-DC converter or Z network is required across each source [20]. This leads to increased size and cost.

This paper proposes a modified MLI topology, which addresses the drawbacks of conventional inverters and recently reported

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inverters. The proposed system consists of single DC source with the single impedance network to enable boost operation. A bank of series connected capacitor is used as potential dividers without any feedback circuit. To overcome the limitations with asymmetrical voltage, simple self-voltage balancing technique [21] is used for maintaining equal voltage across DC-link capacitors.

The rest of the paper is organized as follows. In Section 2, working of proposed topology along with the modes of operation is explained. Section 3 deals with extended proposed structure. The analysis of the entire inverter circuit is discussed in Section 4. Detailed comparison is presented in Section 5. Simulation and experimental results are shown in Section 6 followed by conclusion in Section 7.

2. Proposed topology

The proposed topology shown in Fig. 1 consists of two parts.

Part 1 is Self-voltage Balancing Circuit (SBC), composed of capacitors C_1 – C_5, out of which C_1 & C_2 are the DC bus capacitors and C_3 – C_5 are flying capacitors and clamping switches S_{C1} to S_{C6}. Part 2 is 7-level inverter topology with level generating switches S_5 – S_7 and H Bridge switches S_1 – S_4.

The working of part 1 is shown in Fig. 2. The switches used in SBC are divided into two groups. Group 1 consists of S_{C1}, S_{C3} and S_{C5} and Group 2 consists of S_{C2}, S_{C4} and S_{C6}. SBC operates in two modes. In mode I, Group 1 switches are gated and in mode II, Group 2 switches are gated. The gate pulses should develop such

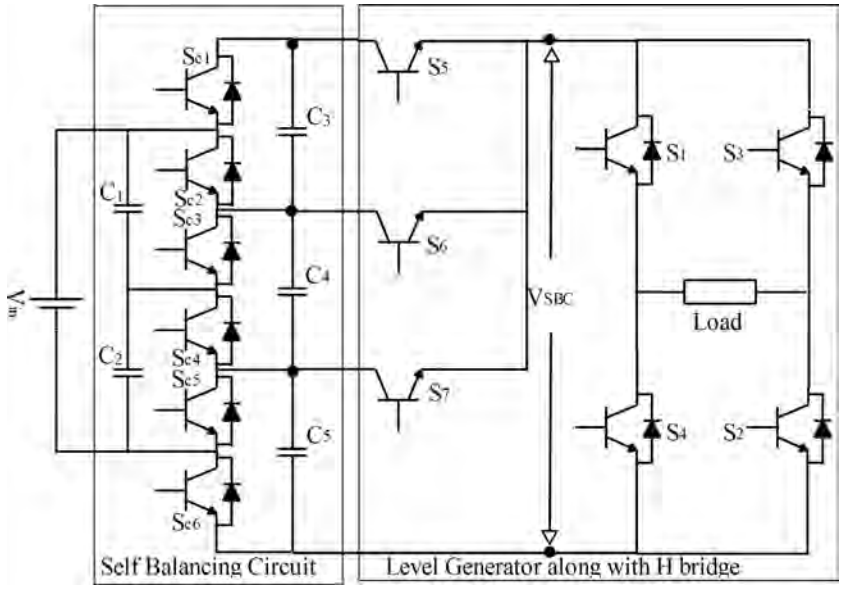

Fig. 1. Proposed Topology.

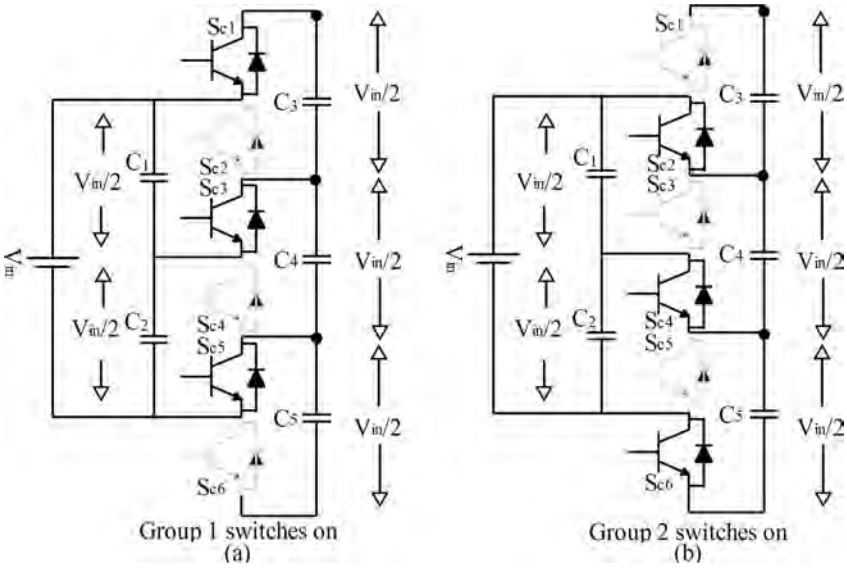

Fig. 2. Mode of operations of SBC. (a) Mode 1 and (b) Mode 2.

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that, when Group 1 switches are turned on Group 2 switches are turned off and vice versa. In this process, all the capacitors are charged to half of the input voltage.

The mode – I operation is shown in Fig. 2(a). In this mode, C_1 is parallel with C_3 and C_2 is parallel with C_4. Thus $V_{C1} = V_{C3}$ and $V_{C2} = V_{C4}$. In mode II, C_1 is parallel with C_4 and C_2 is parallel with C_5 shown in Fig. 2(b). Thus $V_{C1} = V_{C4}$ and $V_{C2} = V_{C5}$.

Due to periodic on and off of Group 1 and Group 2 switches in mode I and mode II respectively, results in equal voltage across all capacitors used in part 1 i.e., all capacitors are charged to half of the input voltage.

Fig. 3 shows the level generating circuit. The proposed topology requires (1/2)(n-1) level generating switches. For generating each level, one level generating switch is turned on as shown in Fig. 3(a), (b) and (c).

All level generating switches along with the SBC part will synthesize balanced positive stepped waveform across H Bridge shown in Fig. 3(d). For generating both positive and negative levels in the output, H Bridge is used. The peak voltage across the inverter is given in (1) and (2).

$$V_{SBC} = V_{C3} + V_{C4} + V_{C5} \tag{1}$$

But, $V_{DC} = V_{C3} = V_{C4} = V_{C5}$

$$V_{SBC} = 3 \times V_{DC}$$

$$V_{SBC} = \frac{3}{2} \times V_{in} \tag{2}$$

where, $V_{DC} = \frac{1}{2} \times V_{in}$

Thus the peak voltage across the inverter is boosted to 1.5 times the input voltage (2).

3. Proposed extended structure with additional boost

Fig. 4 shows the circuit configuration of the proposed MLI, named as Impedance Source based Switched Capacitor MLI (ISSCMLI) for single phase circuit. The extended structure is composed of three parts, part 1 composed of a single voltage source and impedance network, part 2 is voltage balancing circuit and part 3 is level generator with H Bridge. SBC alone is capable of giving a constant boost of 1.5 times the input voltage and additional boost is achieved with impedance network.

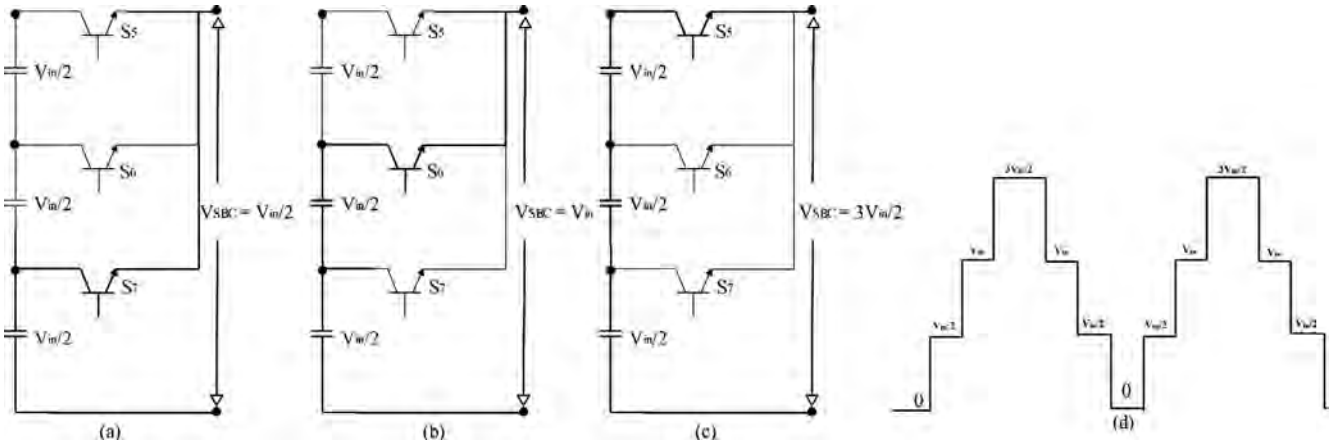

Fig. 3. Operating modes of level generating switches. (a). Lower switch (S_7) turned on for generating + $V_{in}/2$, (b). Middle switch (S_6) turned on for generating + V_{in}, (c). Top switch (S_5) turned on for generating + $3V_{in}/2$ and (d). Positive stepped waveform across inverter.

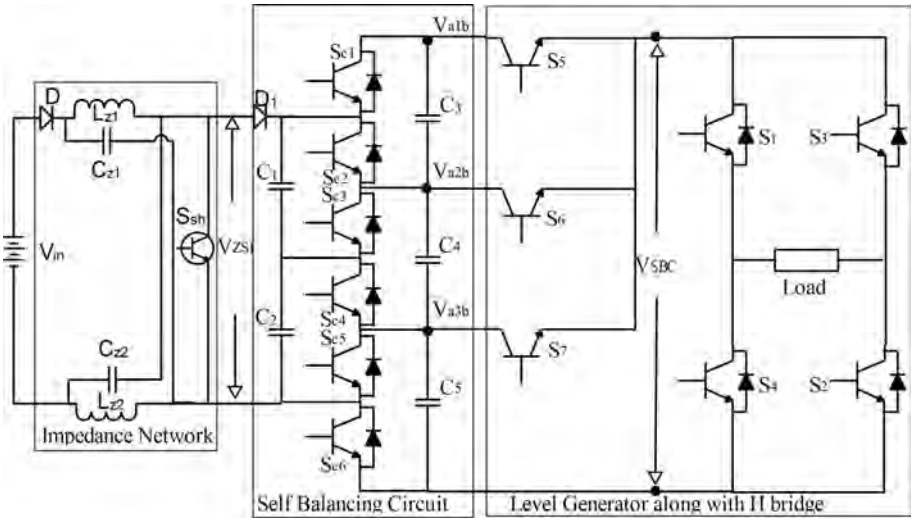

Fig. 4. Extended proposed structure.

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Inverter with impedance source network will operate in three states [22]. State 1 is null state, in this state the capacitor charges from the source voltage. State 2 is shoot through state, in this state the impedance network is short circuited. Capacitors C_{Z1} and C_{Z2} discharges the stored energy into inductors L_{Z1} and L_{Z2} respectively. State 3 is an active state, in this state proposed circuit operates as normal inverter, but the voltage across inverter is boosted. The output voltage of impedance network is given by (3)

$$V_{ZSI} = 2V_L - V_{in} \tag{3}$$

The boost factor for a conventional impedance source inverter (B) is given by (4)

$$B = \frac{1}{1 - 2 \times D_{sh}} \tag{4}$$

Boost factor for proposed topology with impedance network and SBC (B') is given by (5)

$$B' = 1.5 \times B \tag{5}$$

Peak output ($\widehat{V}$) voltage is given by (6)

$$\widehat{V} = B' V_{in} \tag{6}$$

where: D_{sh} is shoot through duty ratio, V_L is the voltage across inductor and V_{in} is input voltage.

In proposed circuit, the shoot through is generated by turning on the switch S_{sh} for a very short time duration over one switching cycle. A simple boost technique [23,24] is used for generating shoot through pulses with switching frequency of 1000 *Hz*.

4. Analysis of proposed inverter

In this section, inverter analysis is reported with respect to pulse generation, voltage stress across the switches, DC link voltage, switching losses and design of circuit parameters.

4.1. Modulation technique

For generating seven level output, three Phase Disposition carriers are used along with sine reference wave having frequency of 50 Hz. All three carrier signals are in phase having same frequency and amplitude with level shift. To generate shoot through pulses for impedance network, a constant signal is compared with carrier signal. When the magnitude of carrier exceeds the constant value shoot through pulses are obtained. A group of pulses are generated by comparing carrier with reference and the generated pulses are combined by using logical gates before applying to respective switches. Fig. 5(a) shows the PWM generation and Fig. 5(b) shows the gate pulses.

4.2. Voltage stress across each switch

Fig. 6 shows the voltage stress across all switches for the proposed circuit with modulation index (M_a) = 1.

For all the clamping switches the blocking voltage is 50% of V_{ZSI} (output voltage of impedance network). The switches S_5, S_7 and S_1 to S_4 have to block the 100% and S_6 has to block 50% of V_{SBC} (output voltage of SBC). The device ratings are chosen based on blocking voltage. Finally, the blocking voltage will depends on maximum boost required.

4.3. DC link voltage

The voltage across the inverter is positive stepped waveform. Along with '0' voltage, 4 steps are produced in each quarter cycle. The magnitude of each step is given by

$$V_{a1b} = (1 - S_5) \times 3 \times \frac{1}{2} \times V_{ZSI} \tag{7}$$

$$V_{a2b} = (1 - S_6) \times 2 \times \frac{1}{2} \times V_{ZSI} \tag{8}$$

$$V_{a3b} = (1 - S_7) \times 1 \times \frac{1}{2} \times V_{ZSI} \tag{9}$$

S_j = 0, when corresponding switch is on; = 1, when corresponding switch is off

The generalized expression for voltage across H Bridge is given by

$$V_{a(J-4)b} = (1 - S_J) \times (8 - J) \times \frac{1}{2} \times V_{ZSI} \tag{10}$$

J = 5, 6 and 7.

4.4. Total switching losses

The losses occur in semiconductor during three instants: when switch is in blocking mode, switch is conducting and switch is changing from on to off or from off to on. The off state losses are insignificant, hence they are neglected [26]. Losses during conduction and switching are considered.

4.4.1. Conduction losses

In proposed topology the number of devices in the current path are always 3, i.e., two from H Bridge and one from level generator (excluding capacitor balance circuit). The instantaneous conduction losses in diode and switch is given by

$$P_{cond,D} = [V_{on,D}(t) + R_D I(t)] I(t) \tag{11}$$

$$P_{cond,T} = \left[V_{on,T}(t) + R_T I^{\alpha}(t)\right] I(t) \tag{12}$$

where $V_{on,D}$, $V_{on,T}$ and R_D, R_T are the on-state voltage drop and on-state resistance of diode and switch respectively and α is constant related to switch characteristics.

Assuming the output current of the inverter is sinusoidal. $I(t) = I_m sin(\omega t)$

In H Bridge structure, a diode will conducts for ø rad in one half cycle and for a period of $(\pi$-ø$)$ switch conducts. The conduction losses are derived as follows

$$P_{cond} = \frac{1}{\pi}\left\{\int_0^{\phi} (V_{on,D}(t) + R_D I(t)) I(t) dwt + \int_{\phi}^{\pi} (V_{on,T}(t) + R_T I^{\alpha}(t)) I(t) dwt\right\} \tag{13}$$

$$P_{cond} = \frac{1}{\pi}\left\{V_{on,D}(t) I_m (1 - cos\phi) + \frac{R_D I_m^2}{2}\left(\phi - \frac{1}{2} sin2\phi\right) + V_{on,T}(t) I_m (1 + cos\phi) + R_T I_m^{\alpha+1} \int_{\phi}^{\pi} sin^{\alpha+1} d(wt)\right\} \tag{14}$$

4.4.2. Switching losses

To evaluate switching losses, initially the switching losses in one switch is calculated, the same analysis is extended for all switches. To calculate switching losses in one device, the linear approximation of voltage and current during switching instant is

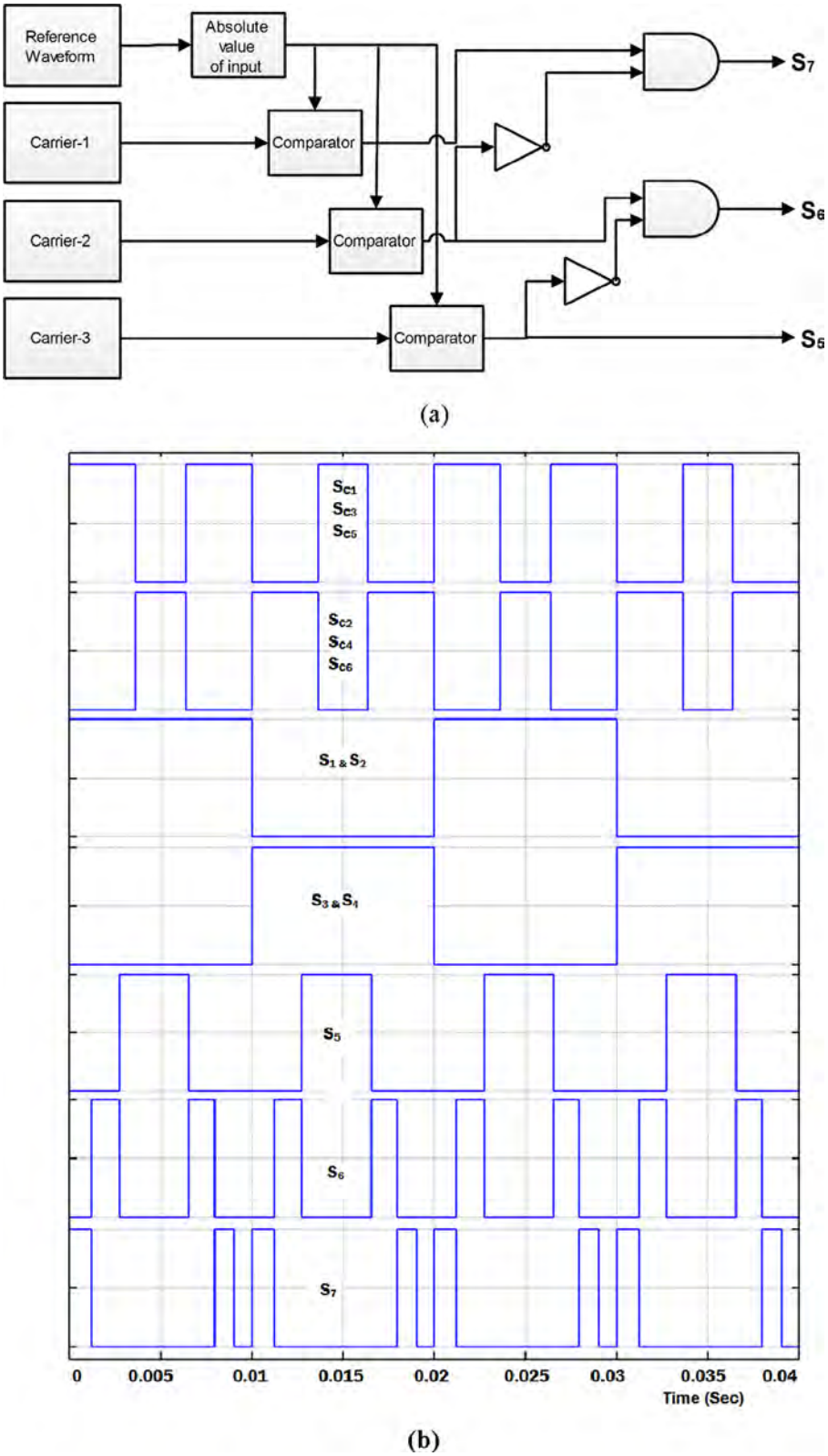

Fig. 5. (a) Logic for PWM. (b) ON/OFF Pulses.

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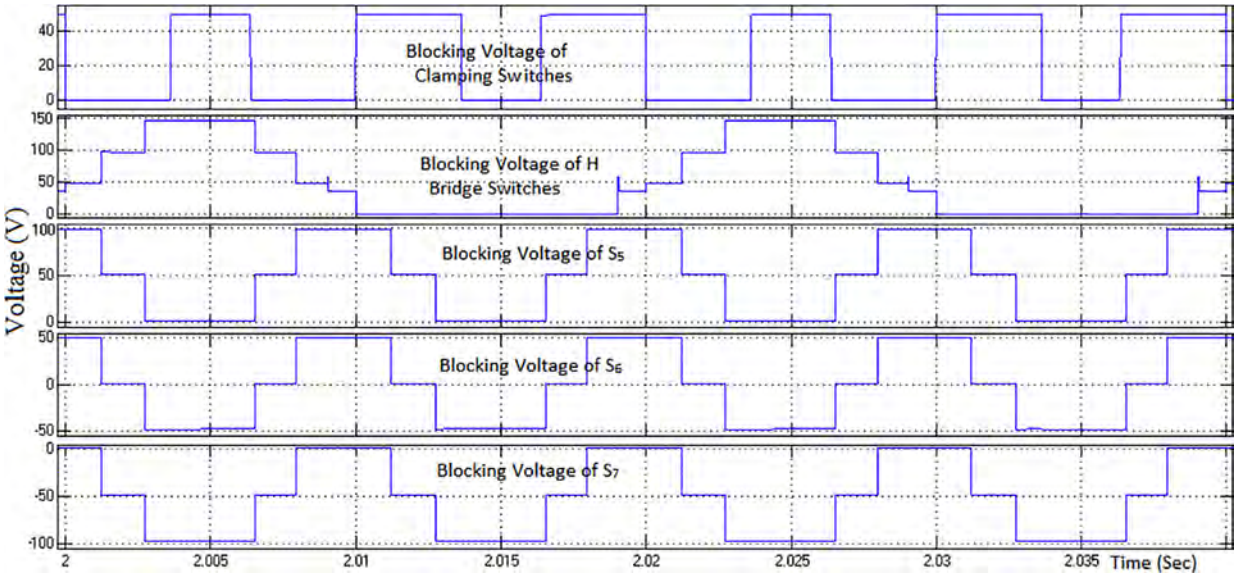

Fig. 6. Blocking voltage across switches.

considered. Power losses when switch is in turn-on period is calculated as follows

$$P_{on} = \int_0^{T_{on}} v(t)i(t)dt = \int_0^{T_{on}} \left\{ \left(\frac{V_{Tr}.t}{T_{on}} \right) \left(-\frac{I(T - T_{on})}{T_{on}} \right) \right\} d(t)$$

$$= \frac{V_{Tr}.I.T_{on}}{6} \quad (15)$$

where, T_{on}, V_{Tr} and I are the turn-on time of the switch, voltage across the switch and current flowing through when it is turned-on respectively.

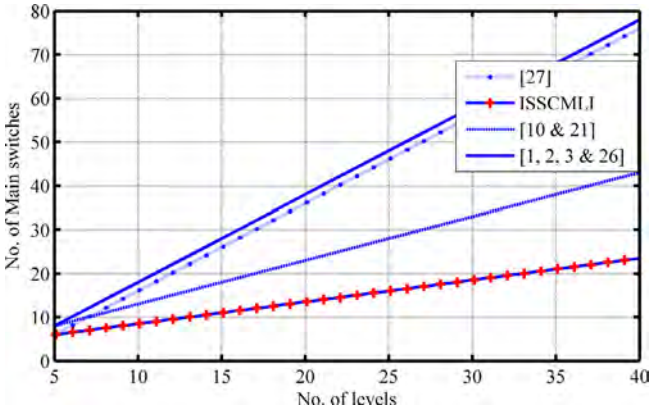

Fig. 7. Number of switching devices required.

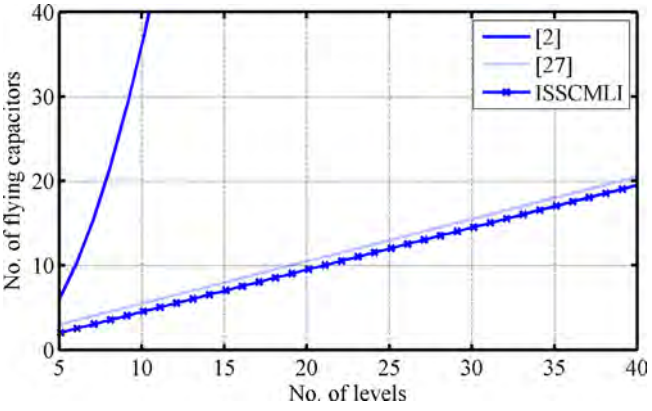

Fig. 9. Number of flying capacitors required.

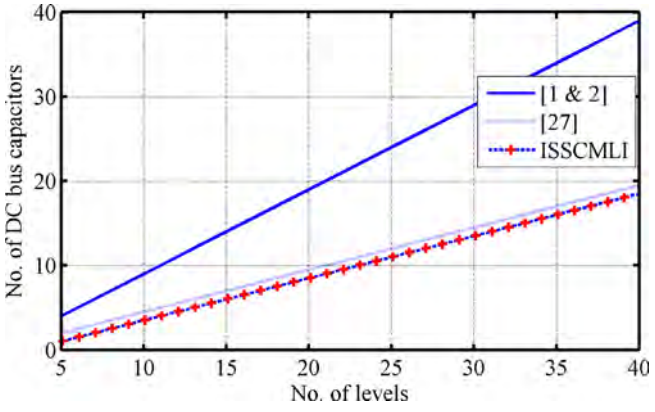

Fig. 8. Number of DC bus capacitors required.

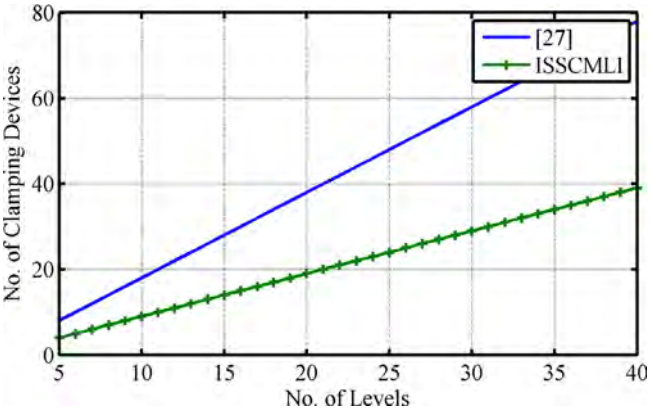

Fig. 10. Number of clamping devices required.

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Power losses when switch is in turn-off period is calculated as follows

$$P_{off} = \int_0^{T_{off}} v(t)i(t)dt = \int_0^{T_{off}} \left\{ \left(\frac{V_{Tr}.t}{T_{off}} \right) \left(-\frac{I(T - T_{off})}{T_{off}} \right) \right\} d(t)$$

$$= \frac{V_{Tr}.I.T_{off}}{6} \quad (16)$$

where T_{off} and I are the period during which the device is turned-off and current during turned-off.

The average switching losses in the device are given by

$$P_{sw} = 2.f.(P_{on} + P_{off}) = \frac{1}{3} fI(T_{on} + T_{off}).V_{Tr} \quad (17)$$

where, f is the switching frequency. The switching and conduction losses in the individual power switch is evaluated using above relations.

4.5. Design of circuit elements

4.5.1. Design of impedance circuit parameters

The relation between input and output voltage of IS network in terms of shoot through duty ratio (D_{sh}) is given by

$$\frac{V_{ZSI}}{V_{in}} = \frac{1}{1 - 2D_{sh}} \quad (18)$$

The maximum ($D_{sh,\max}$) and minimum ($D_{sh,\min}$) values of shoot through duty ratio is evaluated based on minimum and maximum output voltage required from Impedance network using Eq. (1):

$$D_{sh} = \frac{1}{2} - \frac{V_{in}}{2 \times V_{ZSI}}$$

$$D_{sh,max} = \frac{1}{2} - \frac{100}{2 \times 300} = 0.33$$

$$D_{sh,min} = \frac{1}{2} - \frac{100}{2 \times 100} = 0$$

The maximum and minimum values of shoot through duty ratio are 0.33 and 0.0 respectively. Based on maximum value of shoot through duty ratio, the L and C values of impedance network are designed.

4.5.1.1. Design of inductor used in impedance network. The inductor (L_{z1} and L_{z2}) used in impedance network is evaluated as,

$$L_Z = L_{Z1} = L_{Z2} = \frac{(D_{sh,max} \times V_c)}{(F_{sh} \times \Delta I)} \quad (19)$$

Table 1
Comparison of Number of Components Required for ISSCMLI and Other Topologies.

	[1]	[2]	[3]	[9]	[20]	[21]	[25]	ISSCMLI
Main Switches	$2(n-1)$	$2(n-1)$	$2(n-1)$	$(n+3)$	$(n+3)$	$2(n-1)-2$	$2(n-1)$	$((n+7) \div 2)$
Main Diode	$2(n-1)$	$2(n-1)$	$2(n-1)$	$(n+3)$	$(n+3)$	$2(n-1)-2$	$2(n-1)$	$((n+7) \div 2)+2$
Clamping device	0	0	0	0	0	$2(n-2)$	0	$(n-1)$
Clamping Diode	$(n-1)(n-2)$	0	0	0	0	$(n-3)(n-2)$	0	0
Flying capacitors	0	$(n-1)(n-2) \div 2$	0	0	0	$(n+1) \div 2$	0	$(n-1) \div 2$
DC Bus capacitors	$(n-1)$	$(n-1)$	0	0	0	$(n-1) \div 2$	0	$(n-3) \div 2$
DC source	1	1	$(n-1) \div 2$	$(n-1) \div 2$	$(n-1) \div 2$	1	1	1
Impedance network	0	0	0	0	$(n-1) \div 2$	0	1	1
Voltage Balancing	Poor	Moderate	NA	NA	NA	Perfect	NA	Perfect
DC link voltage	= input voltage	= input voltage	= input voltage	= sum of all input	$=2V_L - V_{in}$	= 1.5 times input voltage	$=2V_L - V_{in}$	$= 1.5(2V_L - V_{in})$

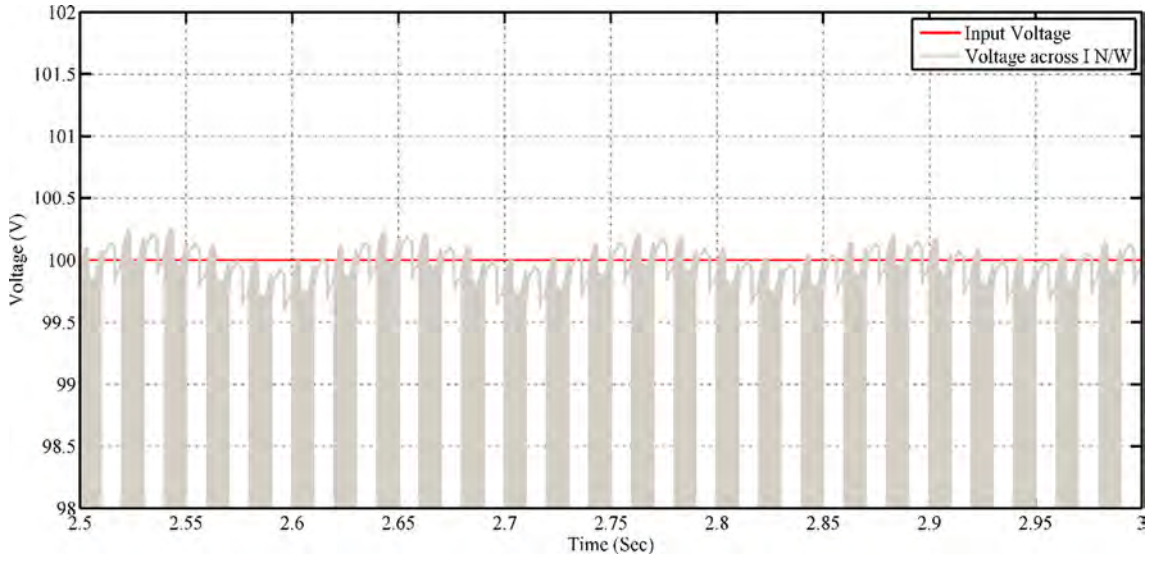

Fig. 11. Input voltage and voltage across impedance network.

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V_c is voltage across the capacitor C_{Z1} or C_{Z2} at (D_{shmax}). V_c is obtained using Eq. (20)

$$V_c = \frac{(1 - D_{sh,max})}{(1 - 2 \times D_{sh,max})} \times V_{in} \tag{20}$$

$$V_c = \frac{(1 - 0.33)}{(1 - 2 \times .33)} \times 100 = 197V$$

F_{sh} is switching frequency of switch S_{sh}, which is having a frequency of 1000 Hz and ΔI is ripple current in the inductor. ΔI is obtained as follows,

$$\Delta I = (4 \text{ to } 5)\% \times I_{out,max} \times \frac{V_{ZSI}}{V_{in}} \tag{21}$$

where, $I_{out,max}$ is maximum output current of inverter and it is fixed to 15 A.

$$\Delta I = 0.04 \times 15 \times \frac{300}{100} = 1.8A$$

The inductance value is $L_Z = L_{Z1} = L_{Z2} = \frac{(0.33 \times 197)}{(1000 \times 1.8)} = 36.11\ mH$

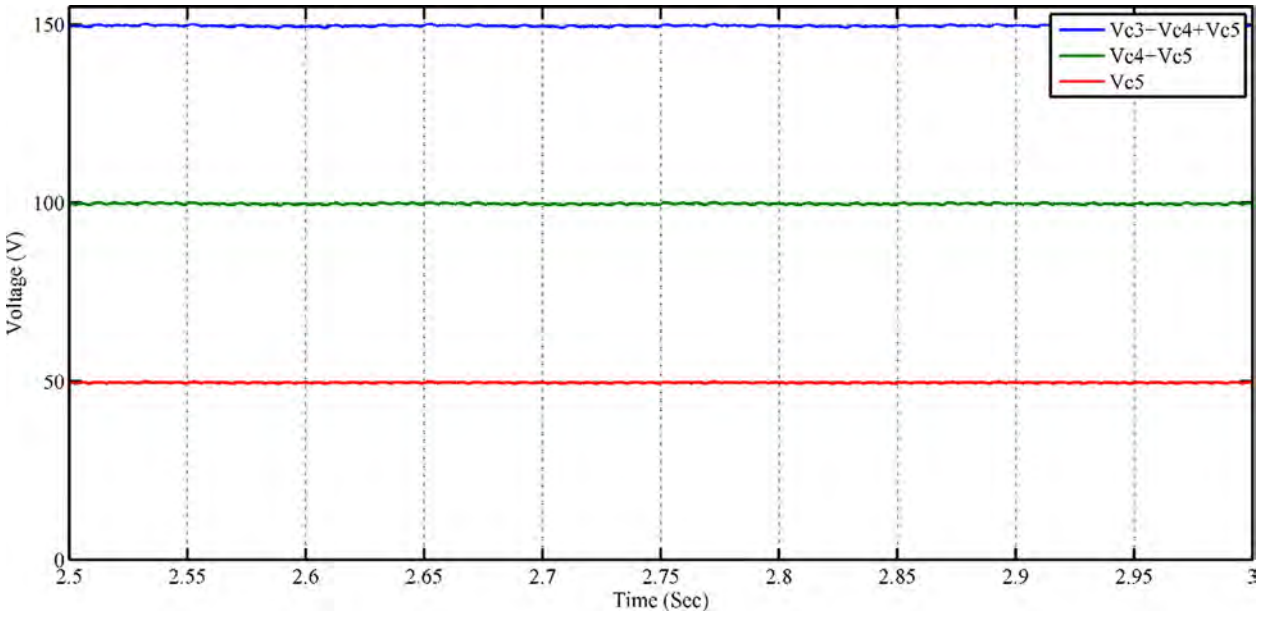

Fig. 12. Voltage across capacitors C_3 to C_5.

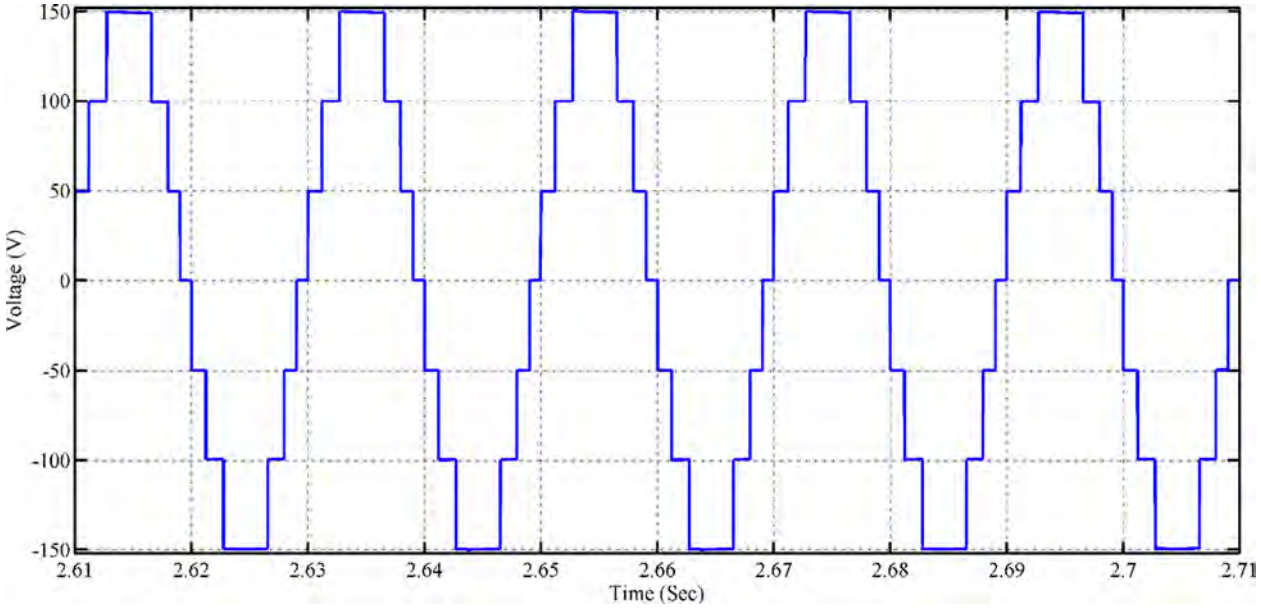

Fig. 13. Voltage across the load.

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4.5.1.2. Design of capacitor used in impedance network. The capacitor (C_{Z1} and C_{Z2}) value used in impedance network is evaluated as:

$$C_Z = C_{Z1} = C_{Z2} = \frac{(I_{out,max} \times D_{sh,max})}{(F_{s1} \times \Delta V_{out})} \quad (22)$$

where ΔV_{out} is ripple voltage of capacitor,

$\Delta V_{out} = (1-3)\%\ of\ V_{in}$

$\Delta V_{out} = 0.02 \times 100 = 2.0V$

$C_z = C_{z1} = C_{z2} = \frac{(15 \times 0.33)}{(1000 \times 2)} = 2.475\ mF$

4.5.1.3. Design of capacitor used in self-balancing capacitor. The capacitor value used in SBC is evaluated as:

$$C_{sbc}(C_1 to\ C_5) = \frac{(I_{out,max} \times D_{sbc})}{(F_{sbc} \times \Delta V_{out})} \quad (23)$$

where ΔV_{out} is ripple voltage of capacitor, D_{sbc} is duty cycle of switches used in SBC and F_{sbc} is switching frequency used for SBC switches.

$\Delta V_{out} = (1-3)\%\ of\ V_{ZSI}$

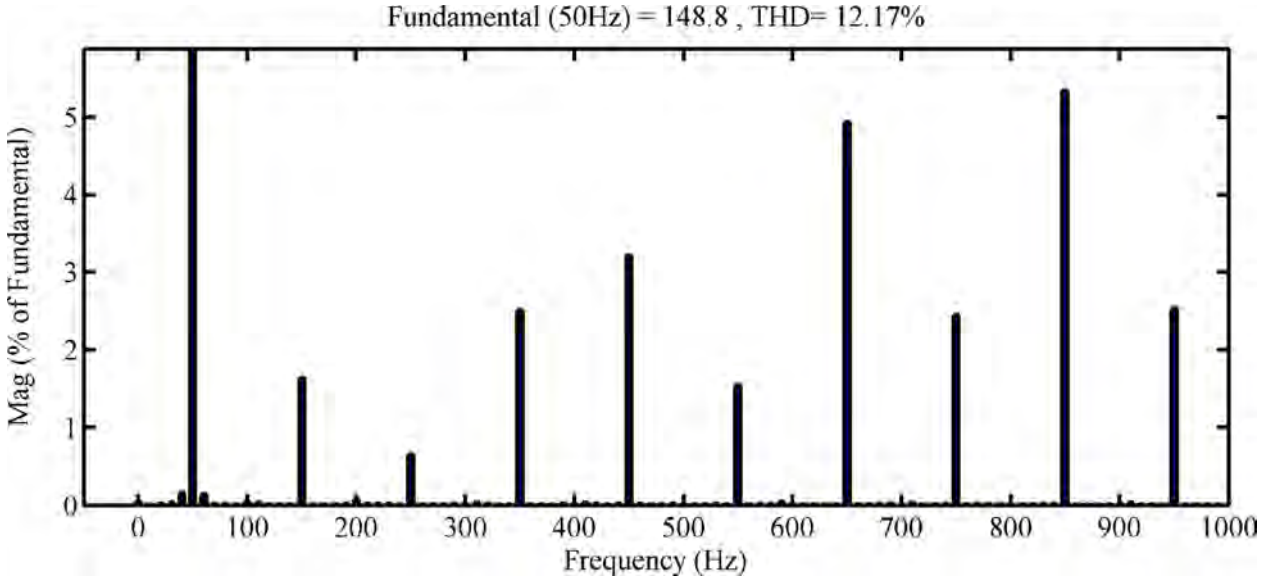

Fig. 14. Total Harmonic Distortion.

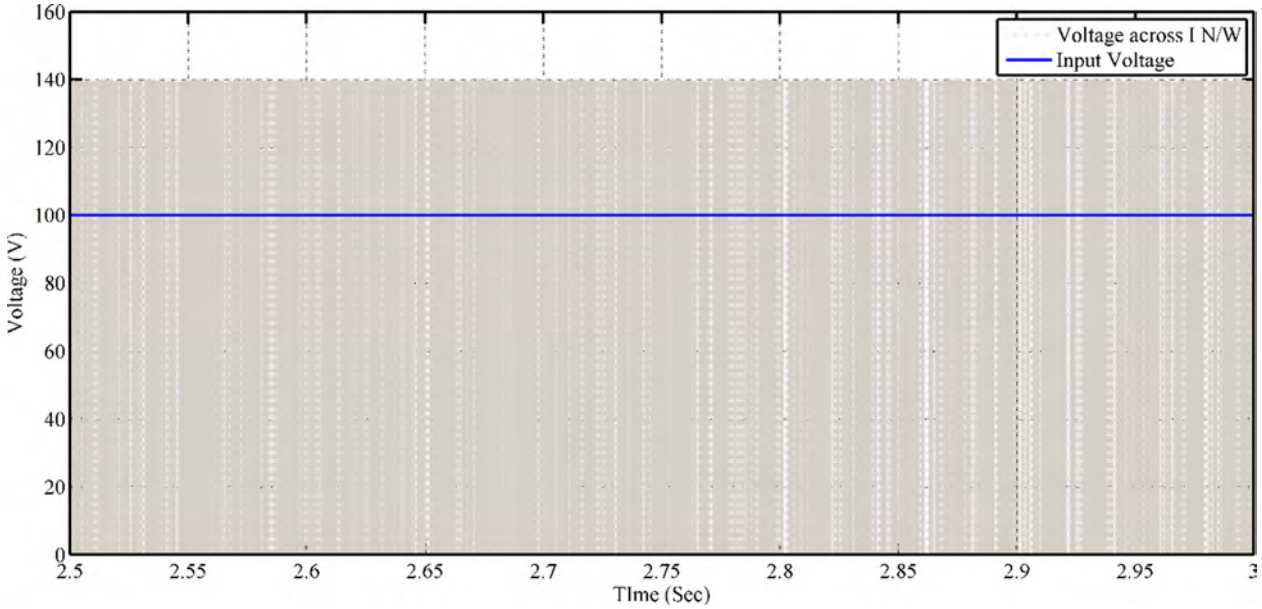

Fig. 15. Input voltage and voltage across impedance network.

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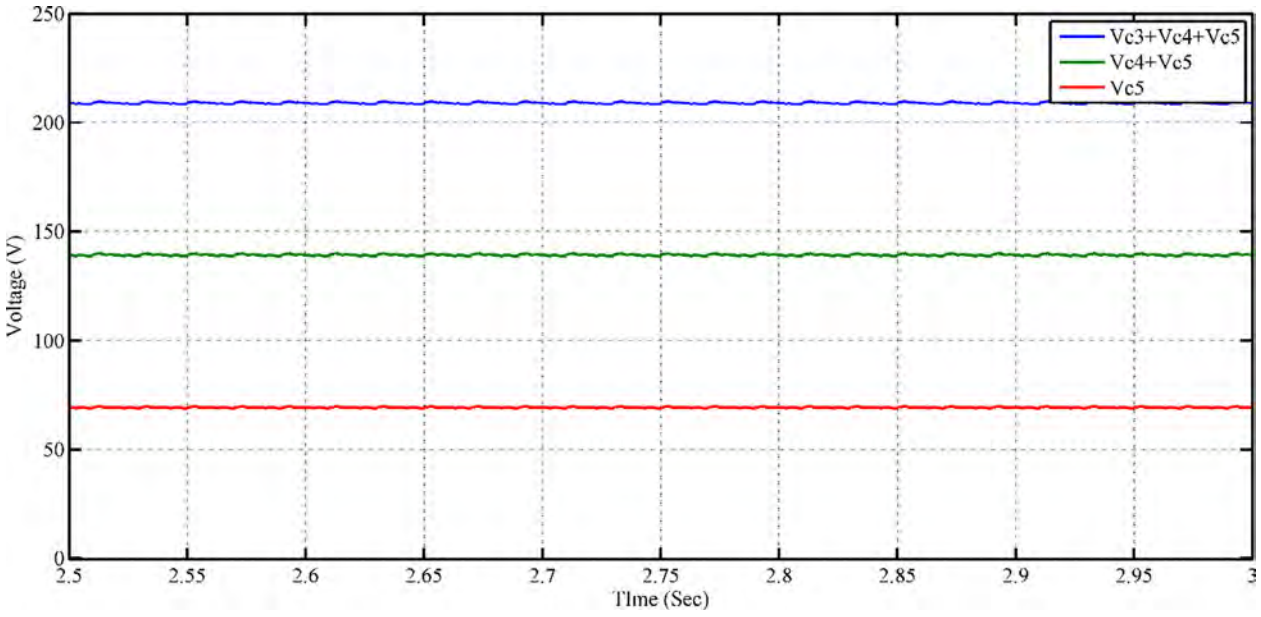

Fig. 16. Voltage across capacitors C_3 to C_5.

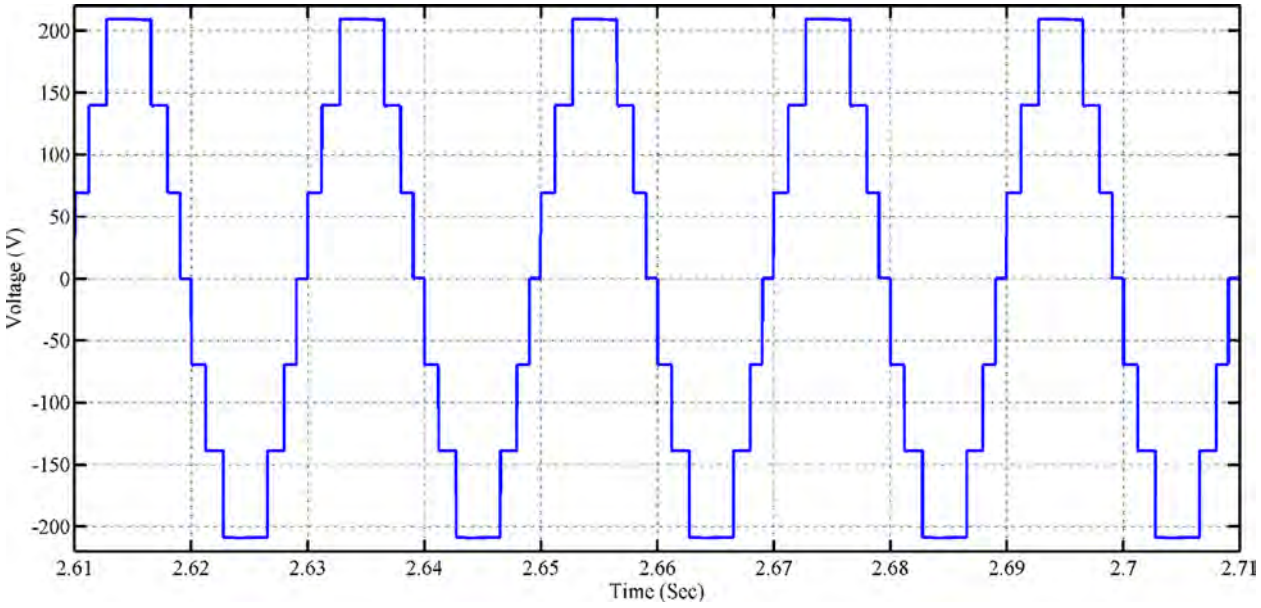

Fig. 17. Voltage across the load.

$$\Delta V_{out} = 0.02 \times 300 = 6V$$

$$C_{sc} = C_{sc1} = C_{sc2} = \frac{(15 \times 0.5)}{(100 \times 6)} = 12.5\ mF$$

5. Comparison with other topologies

For highlighting the originality and benefits with the proposed topology, the comparison is made with conventional and with recent topologies. In MLI's, the consistency and control difficulty is directly proportional to number of switching devices used. Fig. 7 shows the number of switching devices required for conventional, recently reported and proposed inverters. The proposed structure requires a comparatively very less number of switches and a single impedance network. Fig. 8 represents the number of DC bus capacitors required and the voltage unbalance issues increases with increase in number of capacitors. Fig. 9 shows the number of flying capacitors required, in proposed 7-level MLI the number of flying capacitors required are three. Fig. 10 illustrates

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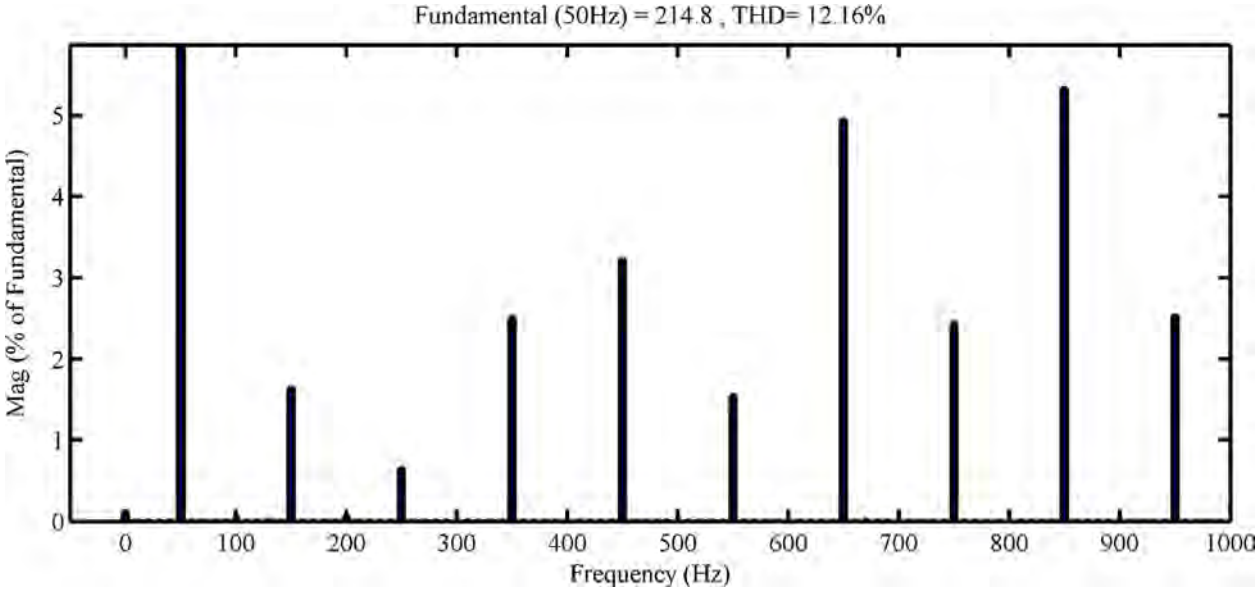

Fig. 18. Total Harmonic Distortion.

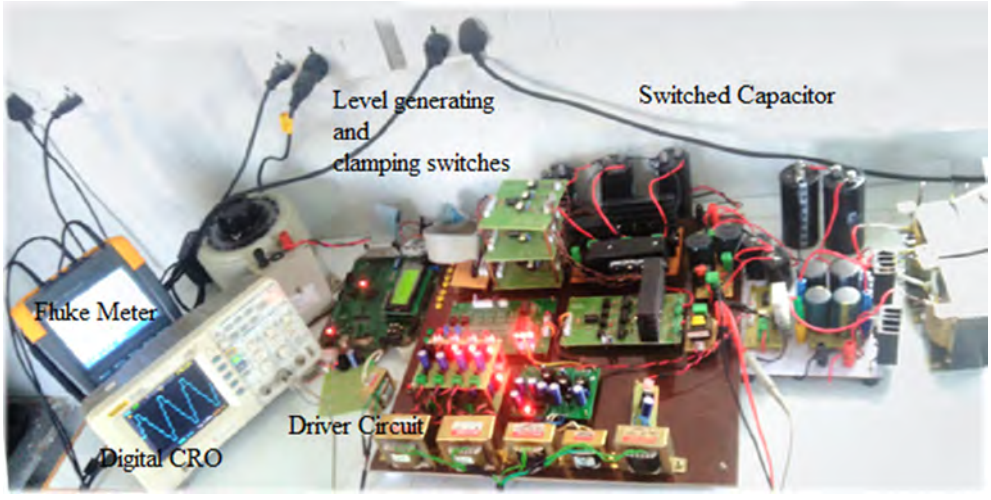

Fig. 19. Experimental setup of proposed inverter.

the number of clamping switches required for maintaining equal voltage across flying capacitors. With proposed topology at any instant only (*n*-1) switches (3 from SBC, 1 from level generation and 2 from H Bridge) conducts. The detailed comparison is listed in Table 1.

6. Simulation and experimental results

To validate theoretical analysis and MATLAB results, the experimental setup is developed for the circuit shown in Fig. 4. The parameters used for the simulation are as follows: Input voltage 100 *V*; Inductance of L_{Z1} and L_{Z2} is 36.11 *mH*; Capacitance of C_{Z1} and C_{Z2} 2.475 *mF*; switches S_1 to S_7 are operated at 50 *Hz*, S_{C1} to S_{C6} are operated at 1000 *Hz* and RL load with resistance of 100 Ω and inductance of 2 *mH*. Figs. 11–14 shows the simulation results of ISSCMLI without shoot through (D_{sh} = 0).

Input voltage along with output voltage of impedance network (I N/W) is shown in Fig. 11. As per Eq. (4) if D_{sh} is zero, the input voltage and output voltage of impedance network is same. All DC link capacitors are charges to equal voltage (50 *V*) as shown in Fig. 12. A seven level output waveform with equal step size of 50 *V* is achieved as shown in Fig. 13. The peak output voltage is 1.5 times the input voltage (1.5 × 100 *V*) is achieved according to Eqs. (5) and (6). The harmonic spectrum for output voltage is shown in Fig. 14. Except shoot through duty ratio (D_{sh}), aforementioned simulation parameters are maintained constant. Figs. 15–18 shows the simulation results of ISSCMLI with shoot through duty ratio (D_{sh}) of 0.14.

Input voltage along with output voltage of impedance network is shown in Fig. 15. As per Eqn. (4) if D_{sh} is 0.14, output voltage of impedance network is boosted by 1.39 times the input voltage (139 *V*). All switched capacitors are charged to equal voltages

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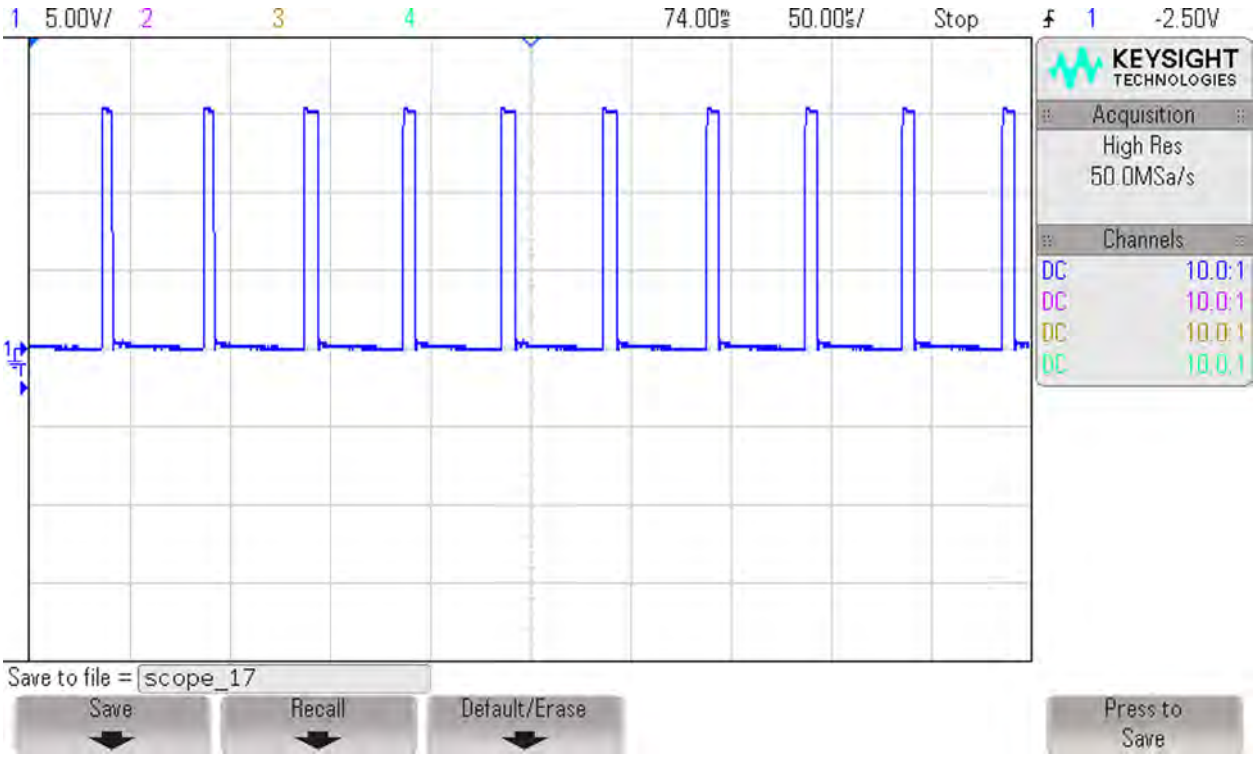

Fig. 20. Gate pulses for $S_{sh.}$

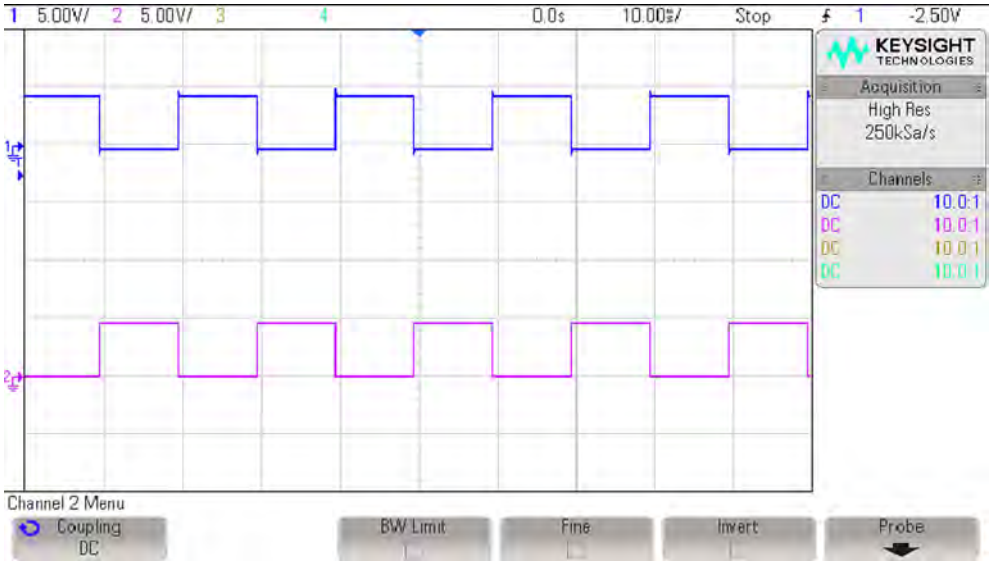

Fig. 21. Gate pulses for SBC.

(68 *V*) as shown in Fig. 16. A seven level output waveform with an equal step size of 68 *V* is achieved as shown in Fig. 17. According to Eqns. (5) and (6), the peak output voltage will be 1.5 times the V_{ZSI} (1.5×139 *V*). The harmonic spectrum of output voltage is shown in Fig. 18.

Experimental setup of ISSCMLI was developed in the laboratory is shown in Fig. 19. The following components are used for experimental setup: three unidirectional IGBT's (S_5 to S_7) IGU04N60T, 10 no. of FGA15N120 IGBT's with anti-parallel diodes. FPGA SPARTAN 6 is used to execute inverter controller, IR2110 driver circuit and TLP250 opto coupler is used. Switching frequency in simulation and hardware setup are identical. All the waveforms are measured and recorded with the help of a power quality analyzer (Fluke 434 series II) and RIGOL dual channel oscilloscope. Figs. 20–23 shows

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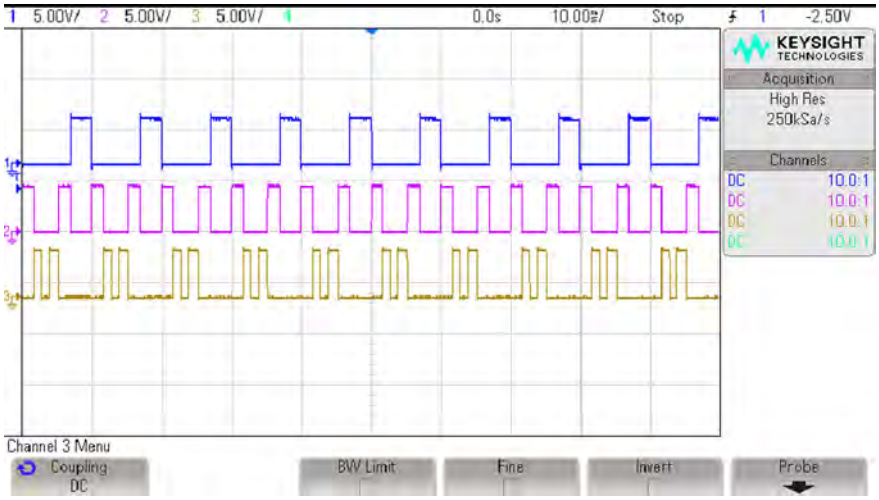

Fig. 22. Gate pulses for level generating circuit.

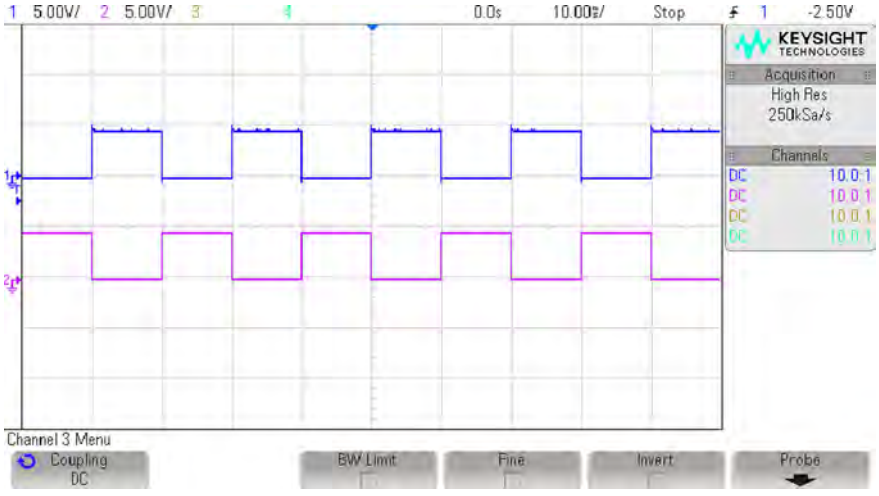

Fig. 23. Gate pulses for H bridge switches.

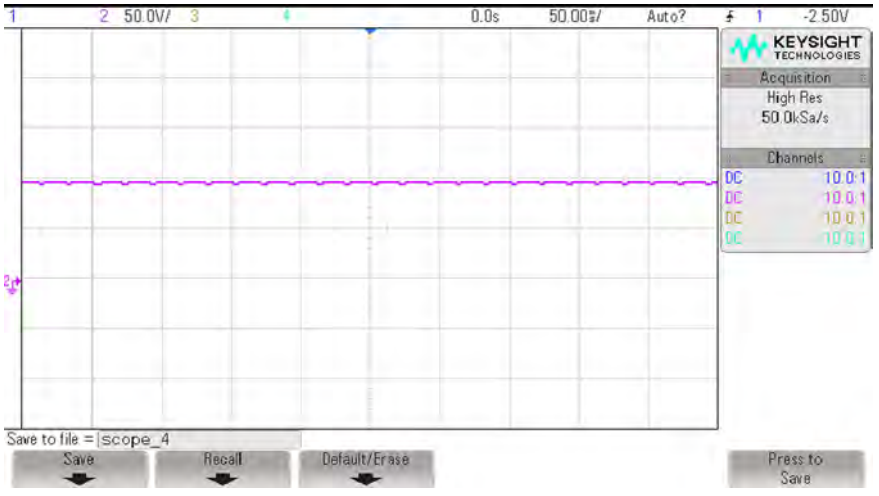

Fig. 24. Voltage across impedance network.

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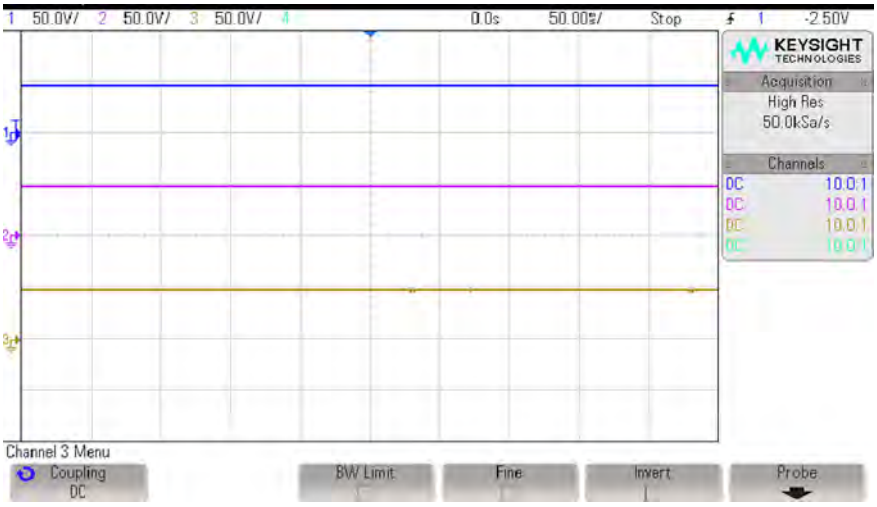

Fig. 25. Voltage across capacitors C_3 to C_5.

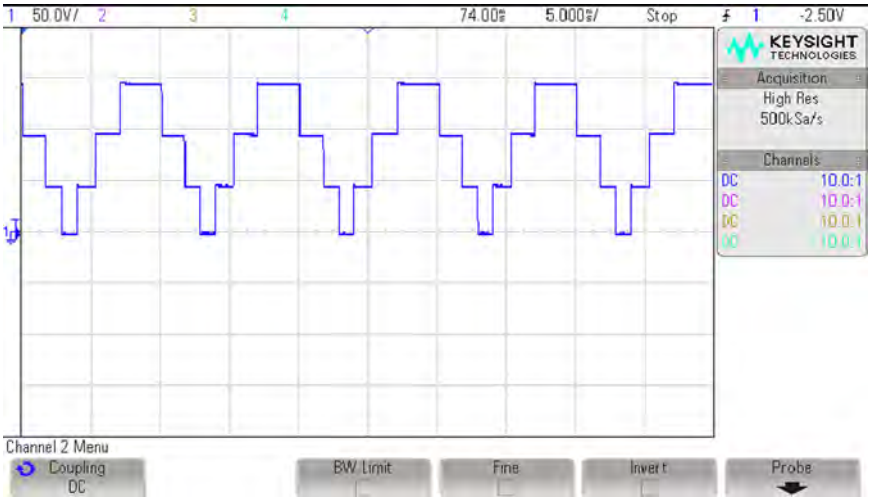

Fig. 26. Output voltage of level generating circuit.

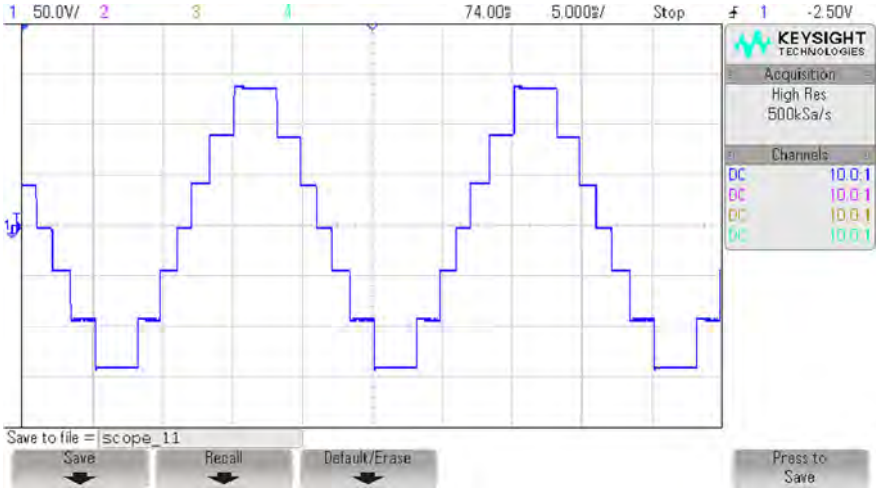

Fig. 27. Voltage across the load.

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the complete gate pulses. Figs. 24–28 shows the experimental results of ISSCMLI without shoot through. Voltage waveforms and Total Harmonic Distortion (THD) are almost same with the respective simulation results.

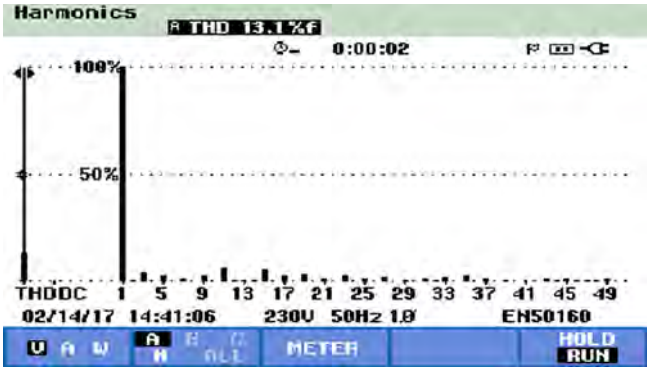

Fig. 28. Total Harmonic Distortion.

The shoot through pulses with magnitude of 5 V (5 V/div) for switch S_{sh} with shoot through duty ratio of 0.14 is shown in Fig. 20. The Fig. 21 shows the gate pulses for the switches present in the balancing circuit. The pulse waveform shown in channel 1 is used to drive the odd numbered switches and pulse shown in channel 2 is used to drive the even numbered switches. The switching pulses for switches used in level generation unit are shown in shown in Fig. 22. The pulses shown in channel 1 is used to drive the switch S_5 and pulses shown in channels 2 and 3 are used to drive the switches S_6 and S_7 respectively. Fig. 23 shows gate pulses for switches used in polarity generation unit. The pulse shown in channel 1 is used to drive the switches S_1 and S_2. The switches S_3 and S_4 are gated with the pulses shown in channel 2.

Fig. 24 shows the output voltage of Impedance network. Fig. 25 shows the voltage distributed across Switched capacitors C_3 to C_5. The output voltage of level generating circuit is shown in Fig. 26. The peak voltage across the load is 1.5 times the V_{ZSI} shown in Fig. 27 and harmonic spectrum is represented in Fig. 28.

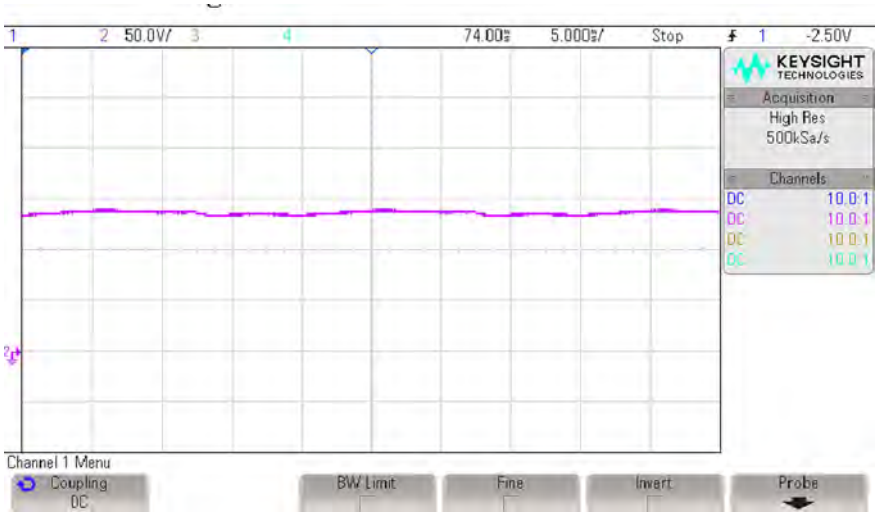

Fig. 29. Voltage across impedance network.

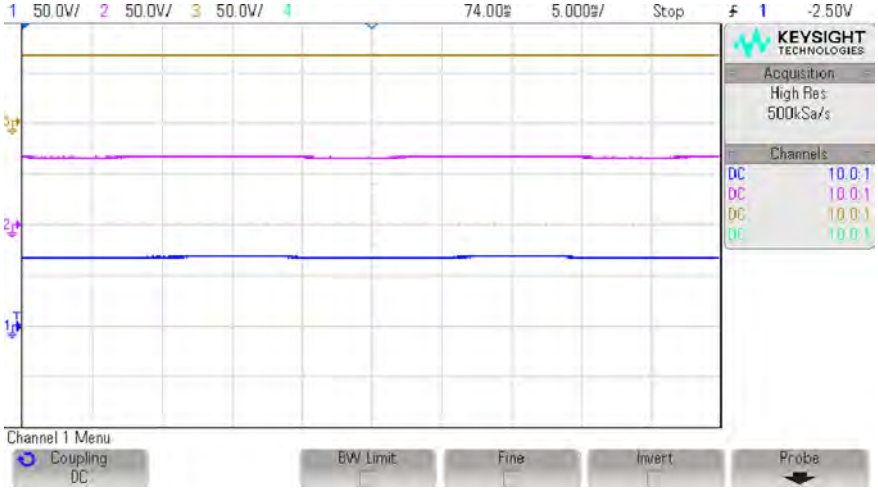

Fig. 30. Voltage across capacitors C_3 to C_5.

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Figs. 29–33 shows the experimental results of ISSCMLI with shoot through duty ratio (D_{sh}) of 0.14. Fig. 29 shows the output voltage of Impedance network, it is boosted to 1.39 times the input voltage. Fig. 30 shows the voltage distributed across capacitors C_3 to C_5. The output voltage of level generating circuit is shown in Fig. 31. Fig. As shown in Fig. 32, the peak voltage across the load is boosted to 1.5 times the output voltage of impedance network. Fig. 33 represents the harmonic spectrum.

The percentage of fundamental and harmonic content is obtained from FFT analysis tool. By using Eq. (24), the THD is calculated. Theoretical THD = 13.4%.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n_r ms}^2}}{V_{Fund_r ms}} \tag{24}$$

where: V_{n_rms} is the RMS voltage of the n^{th} harmonic,

V_{Fund_rms} is the RMS voltage of the fundamental component.

The efficiency of proposed inverter from Eqn. (25) is 93%, which is higher than the inverter presented in [27].

$$Efficiency = \frac{V_{out_r ms} \times I_{out_r ms} \times PF}{V_{in} \times I_{in_a vg}} \tag{25}$$

Fig. 34 shows the peak output voltage obtained with theoretical calculation, simulation and experimental results and it is observed that peak value obtained for different shoot through ratios are equal. The suggested range of Shoot through duty ratio (D_{sh}) is 0–0.33. The switching losses in the individual switch is given in Table 2.

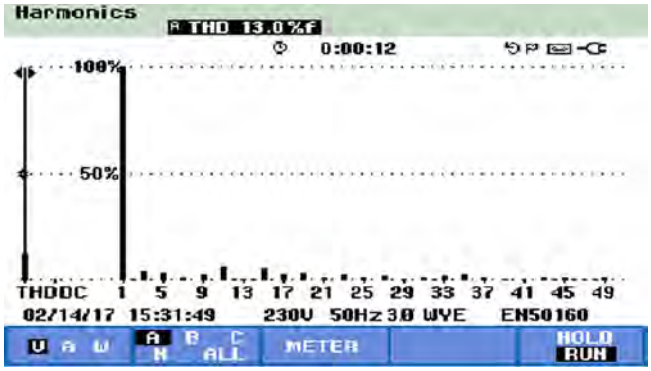

Fig. 33. Total Harmonic Distortion.

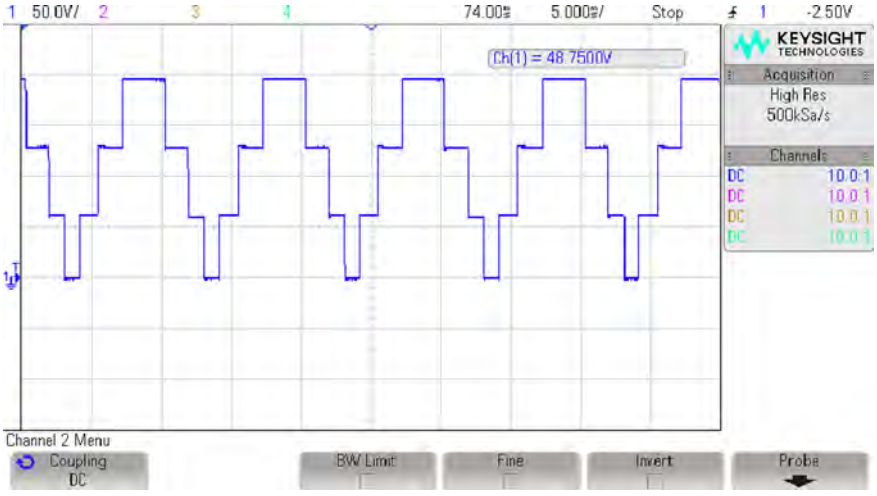

Fig. 31. Output voltage of level generating circuit.

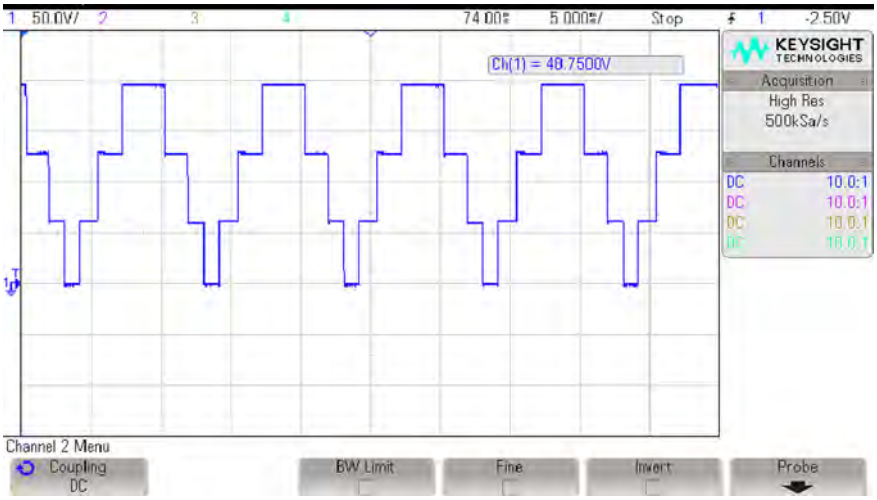

Fig. 32. Voltage across the load.

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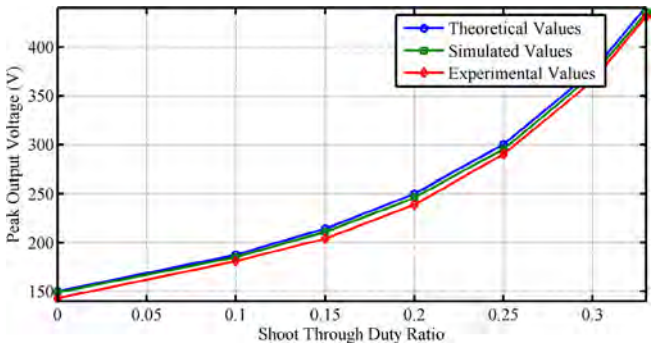

Fig. 34. Comparison of results.

Table 2
Losses in individual switch during non-shoot through and shoot through states.

Sl. No.	Switch No.	Losses during non-shoot through state	Losses during shoot through state
1	S_{sh}	0	0.38 W
2	SBC switches S_{c1} to S_{c6}	0.65 W/switch	0.9 W/Switch
3	S_5	0.46 W	1.1 W
4	S_6	0.16 W	0.4 W
5	S_7	0.29 W	0.6 W
6	H Bridge switches S_1 to S_4	0.75 W/switch	1.27 W/switch
Total Losses		7.81 W	12.96 W
Output power		112.5 W	200 W
Efficiency of Inverter		93.5%	93.91%

7. Conclusions

This paper proposes Impedance Source Switched Capacitor Multilevel Inverter with enhanced boost capability with less number of switching devices compared to conventional and recently reported multilevel inverters. Seven level output is achieved by using one input source and one impedance network. The balanced voltage across all the capacitors is obtained by using self-voltage balance circuit. All the capacitors are charged to half of the input voltage. At any instant (n-1) switches are conducting, which is far less than conventional MLI. All the switches are operated at the lower frequency result in lower switching losses. The experimental setup is developed based on simulation parameters and it is observed that both results are closely identical.

References

[1] M. Fracchia, et al., Optimized modulation techniques for the generalized N-level converter, in: Power Electronics Specialists Conference, 1992. PESC'92 Record., 23rd Annual IEEE. IEEE, 1992. doi: 10.1109/PESC.1992.254737
[2] Sang-Gil Lee, et al., The carrier-based PWM method for voltage balance of flying capacitor multilevel inverter, in: Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual. Vol. 1. IEEE, 2001. doi: 10.1109/PESC.2001.954006
[3] Patricio Cortes et al., Model predictive control of multilevel cascaded H-bridge inverters, IEEE Trans. Ind. Electron. 57 (8) (2010) 2691–2699, https://doi.org/10.1109/TIE.2010.2041733.
[4] Krishna Kumar Gupta et al., Multilevel inverter topologies with reduced device count: a review, IEEE Trans. Power Electron. 31 (1) (2016) 135–151, https://doi.org/10.1109/TPEL.2015.2405012.
[5] Bambang Sujanarko, Mochamad Ashari, Mauridhi Hery Purnomo, Article: Universal Algorithm Control for Asymmetric Cascaded Multilevel Inverter. Int. J. Comput. Appl. 10(6):38–44, November 2010. Published By Foundation of Computer Science. doi: 10.5120/1483-2000
[6] Shivam Prakash Gautam, Lalit Kumar Sahu, Shubhrata Gupta, Reduction in number of devices for symmetrical and asymmetrical multilevel inverters, IET Power Electron. 9 (4) (2016) 698–709, https://doi.org/10.1049/iet-pel.2015.0176.
[7] Ebrahim Babaei, Sara Laali, Zahra Bayat, A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches, IEEE Trans. Ind. Electron. 62 (2) (2015) 922–929, https://doi.org/10.1109/TIE.2014.2336601.
[8] Gnana Prakash, M. Balamurugan, S. Umashankar, A new multilevel inverter with reduced number of switches. Int. J. Power Electron. Drive Syst. 5.1 (2014) 63. pp 10.11591/ijpeds.v5i1.6089
[9] Ebrahim Babaei, Seyed Hossein Hosseini, New cascaded multilevel inverter topology with minimum number of switches., Energy Convers. Manage. 50 (11) (2009) 2761–2767, https://doi.org/10.1016/j.enconman.2009.06.032.
[10] Kannan Ramani, Mohd Ali Jagabar Sathik, Selvam Sivakumar, A new symmetric multilevel inverter topology using single and double source sub-multilevel inverters, J. Power Electron. 15 (1) (2015) 96–105, https://doi.org/10.6113/JPE.2015.15.1.96.
[11] Mohamad Reza Banaei, E. Salary, Single-source cascaded transformers multilevel inverter with reduced number of switches, IET Power Electron. 5 (9) (2012) 1748–1753, https://doi.org/10.1049/iet-pel.2011.0431.
[12] Kai-Ming Tsang, Wai-Lok Chan, Single DC source three-phase multilevel inverter using reduced number of switches, IET Power Electron. 7 (4) (2014) 775–783, https://doi.org/10.1049/iet-pel.2013.0319.
[13] Jian Cao, Nigel Schofield, Ali Emadi, Battery balancing methods: a comprehensive review. Vehicle Power and Propulsion Conference, 2008. VPPC'08. IEEE, IEEE (2008), https://doi.org/10.1109/VPPC.2008.4677669.
[14] Viju Nair et al., Novel Symmetric 6-Phase Induction Motor Drive Using Stacked Multilevel Inverters with a Single DC Link and Neutral Point Voltage Balancing, IEEE Trans. Ind. Electron. (2016), https://doi.org/10.1109/TIE.2016.2637884.
[15] Sung-Jun Park et al., A novel switching strategy for improving modularity and manufacturability of cascaded-transformer-based multilevel inverters, Electr. Power Syst. Res. 74 (3) (2005) 409–416, https://doi.org/10.12928/telkomnika.v8i2.613.
[16] Feel-soon Kang, A modified cascade transformer-based multilevel inverter and its efficient switching function, Electr. Power Syst. Res. 79 (12) (2009) 1648–1654, https://doi.org/10.1016/j.epsr.2009.07.001.
[17] Rajesh Gupta, Arindam Ghosh, Avinash Joshi, Control of cascaded transformer multilevel inverter based DSTATCOM, Electr. Power Syst. Res. 77 (8) (2007) 989–999, https://doi.org/10.1016/j.epsr.2006.08.015.
[18] Sung Geun Song, Feel Soon Kang, Sung-Jun Park, Cascaded multilevel inverter employing three-phase transformers and single dc input, IEEE Trans. Ind. Electron. 56 (6) (2009) 2005–2014, https://doi.org/10.1109/TIE.2009.2013846.
[19] Chihchiang Hua, Chihming Shen, Study of maximum power tracking techniques and control of DC/DC converters for photovoltaic power system. Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE. Vol. 1. IEEE, 1998. doi: 10.1109/PESC.1998.701883
[20] M.R. Banaei et al., Z-source-based multilevel inverter with reduction of switches, IET Power Electron. 5 (3) (2012) 385–392, https://doi.org/10.1049/iet-pel.2011.0198.
[21] Jing Zhao et al., Multilevel circuit topologies based on the switched-capacitor converter and diode-clamped converter, IEEE Trans. Power Electron. 26 (8) (2011) 2127–2136, https://doi.org/10.1109/TPEL.2010.2104330.
[22] Fang Zheng Peng, Z-source inverter, IEEE Trans. Ind. Appl. 39 (2) (2003) 504–510, https://doi.org/10.1109/IAS.2002.1042647.
[23] Poh Loh, Chiang, et al. Pulse-width modulation of Z-source inverters. Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE. Vol. 1. IEEE, 2004. doi: 10.1109/TPEL.2005.857543
[24] B.M. Manjunatha, D.V. Ashok Kumar, M. Vijay Kumar, Advanced pulse width modulation techniques for Z source multi level inverter, World Acad Sci Eng Technol Int Sci Index 99 (2015) 337–342
[25] Mohamad Reza Banaei et al., Switching algorithm for single Z-source boost multilevel inverter with ability of voltage control, IET Power Electron. 6 (7) (2013) 1350–1359, https://doi.org/10.1049/iet-pel.2012.0636. doi: 10.1049/iet-pel.2012.0636.
[26] RasoulShalchi Alishah et al., Reduction of power electronic elements in multilevel converters using a new cascade structure, IEEE Trans. Ind. Electron. 62 (1) (2015) 256–269.
[27] B. Verma Sapna, Rajni Rewatkar, Comparison Of Grid Connected 5-Level And 7-Level Inverters. Int. J. Electr. Electron. Data Commun. ISSN: 2320-2084, Special Issue, June-2015.