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A dual mode step-down switched-capacitor DC-DC converter with adaptive switch width modulation

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ABSTRACT

This paper proposes a step-down switched-capacitor (SC) DC-DC converter with pulse frequency modulation (PFM) and burst mode. This design proposes a novel dual mode control strategy to achieve high performance over a wide load range. PFM is adopted at heavy load to achieve the small output voltage ripple while burst mode is adopted at light load to improve transient response and power efficiency. To further improve the efficiency, an adaptive switch width modulation (ASWM) is proposed to reduce switching losses. The measured results show that the proposed four conversion ratios converter can operate with a 2.0–3.6 V input voltage range, load current from 0 to 2 mA at the output voltage of 1.2 V. The peak power efficiency is up to 84.2% from a 2.7 V input voltage supply at a load current of 2 mA. At a load of 60 μA, the burst mode achieves an 11% maximum efficiency improvement, and the average efficiency improvement of 6% is achieved with ASWM.

1. Introduction

Power supply should meet the needs of high power density, small area and low consumption for advanced devices [15,16]. Compared with traditional switched-inductor DC-DC converter [14], SC DC-DC converter can be easily integrated on a chip [1]. It also avoids electromagnetic interference (EMI). Both these advantages raise attentions of researcher to SC DC-DC converter.[4,5].

There are capacitance modulation and switching frequency modulation for output regulation at present [6,8], [9]. A digital capacitance modulation is proposed to regulate output voltage [6], but the lack of capacitance limits the simultaneous 100% capacitance utilization, so the power density of the converter decreases naturally. The switching frequency modulation can be divided into the digital modulation and the analog modulation. The digital switching frequency modulation achieves fast transient response, but it has the disadvantages of low precision and large output voltage ripple for output regulation [8]. An analog switching frequency control strategy is proposed to guarantee high precision and small output voltage ripple. [9], but due to the control losses, the power efficiency decreases rapidly at light load, the control strategy also has a problem that no detailed system stability analysis of the converter particularly the SC array is given. In order to solve the problem, this paper proposes an optimal dual mode controller instead of a single control strategy to regulate output voltage.

Another issue aims at reducing the switching losses to improve power efficiency. A conversion ratio only gains high power efficiency in a narrow input/output voltage range [2,3]. A reconfigurable SC array is implemented for a wide voltage range [10,11,13,17,20,21], however, the dominant switching losses becomes the main factor decreasing power efficiency. The switch width of SC array is usually determined by the maximum switching frequency, but the optimal switch width of the SC array varies with variation of the switching frequency, so the switching losses can be reduced by adjusting switch width at low switching frequency.

As is discussed above, this paper proposes a dual mode step-down SC DC-DC converter with four conversion ratios. PFM is adopted at heavy load while burst mode is adopted at light load. PFM achieves small output voltage ripple and high precision, a detailed system stability analysis is introduced. To overcome the problems of the lower power efficiency and the decreasing Gain bandwidth product (GBW) of PFM operation at light load, burst mode is adopted to reduce the control losses and implement fast transient response. To reduce switching losses over entire load range,

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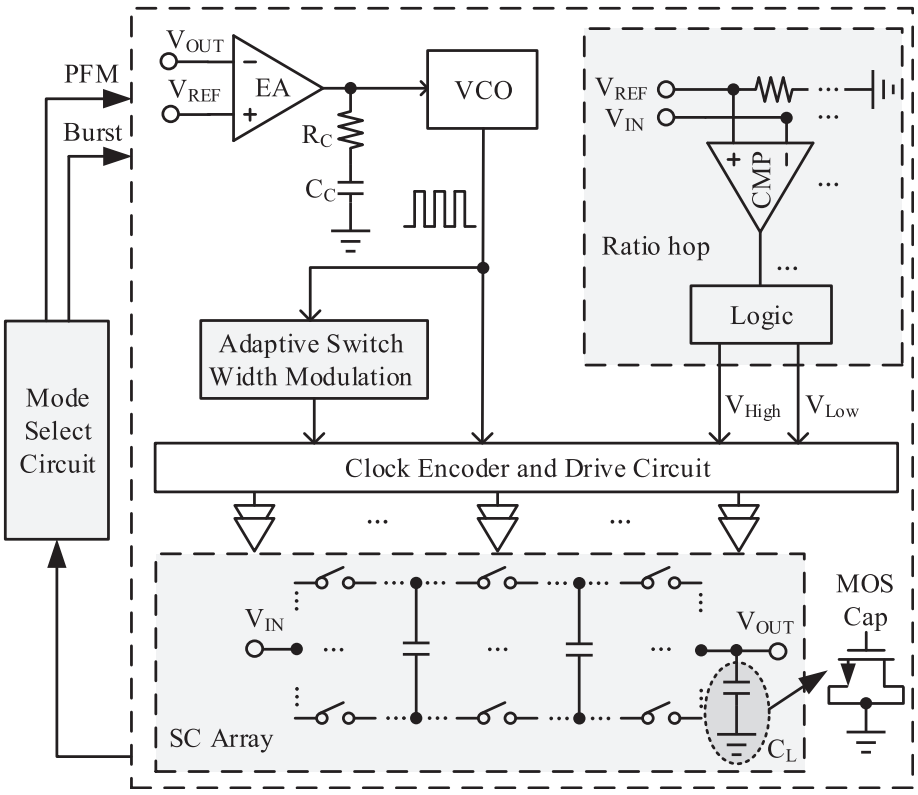

Fig. 1. Block diagram of the proposed SC DC-DC converter.

ASWM is proposed to optimize switch width with the variation of the switching frequency.

The rest of the paper is organized as follows. Section 2 is the detailed introduction of the proposed SC DC-DC converter, including operating principle of dual mode control strategy, and ASWM, a detailed system stability analysis is introduced at PFM operation. Section 3 describes the circuit implementation in detail. The measured results of the proposed converter in 0.18 μm CMOS technology are shown in section 4. Section 5 concludes the paper.

2. Proposed SC DC-DC converter

The proposed SC DC-DC converter consists of three main blocks as shown in Fig. 1, which are the ratio hop circuit, the SC power stage and the feedback controller. The SC power stage are four ratios SC array and output MOS capacitor. Dual mode control strategy and ASWM are realized in the feedback controller for output regulation.

When the system starts to work, the ratio hop circuit selects conversion ratio by input voltage. Four conversion ratios (2/3, 3/5, 1/2, 2/5) is selected by the ratio hop circuit for a 2.0V-3.6 V input voltage range, so the converter can achieve high efficiency for a wide input voltage range by these four conversion ratios. Then the mode select circuit determines the control mode of the SC DC-DC converter by detecting the load current. Dual mode control is adopted in the SC DC-DC converter, the SC DC-DC converter works in PFM for heavy load condition while in burst mode for light load condition. In PFM, the EA (error amplifier) compares the V_{OUT} with the reference voltage V_{REF}. The VCO (voltage controlled oscillator) generates CLK signal with different switching frequency by the output of EA, the switching frequency is adjusted with variation of the load condition. In the burst mode, the VCO turns off and turns on intermittently to get a stable output voltage V_{OUT}. The advantages of dual mode control strategy are achieved in the SC DC-DC converter. The converter gets smaller ripple, higher efficiency and faster load transient over the entire load current range. Besides, the CLK signal turns on the ASWM to adjust the switch width of the SC array, the optimal switch width of the SC array is achieved by the switching

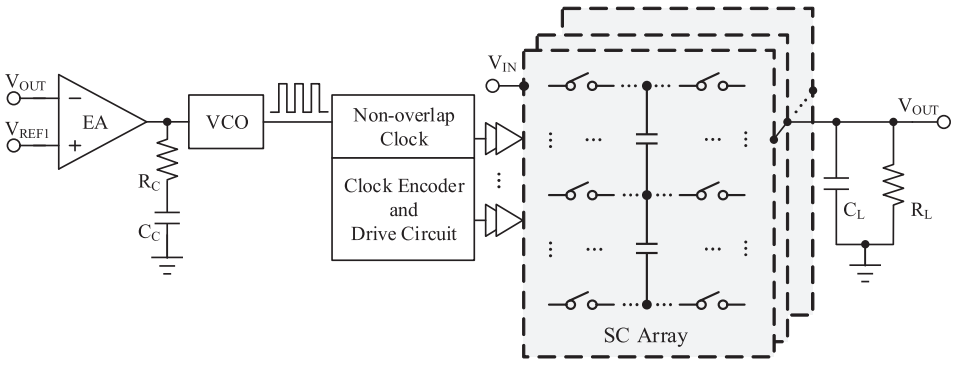

Fig. 2. Schematic of the proposed PFM control strategy.

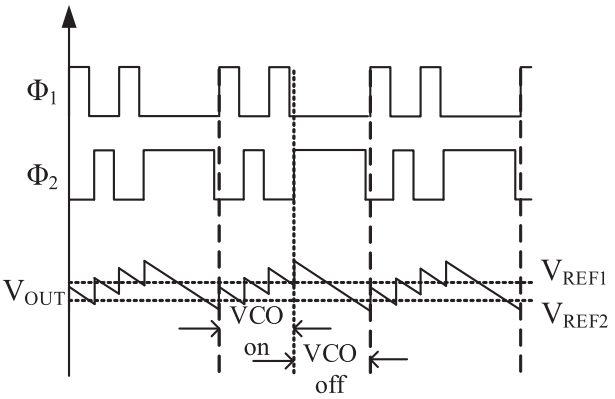

Fig. 3. Time diagram of the switching signal and output voltage at burst mode.

frequency of the VCO. Compared with the fixed switch width of the traditional SC DC-DC Converter, this technique improves power efficiency by reducing switching losses.

2.1. Dual mode control strategy

Dual mode control strategy aims at achieving high performance over the entire load range. PFM has the advantages of small output voltage ripple and high precision, but the transient response and power efficiency will decrease at light load. Burst mode detects output voltage with comparator, compared with PFM at light load, the transient response time can be improved; besides, the control circuit turns off intermittently, so the power efficiency can be improved at light load.

2.1.1. PFM control

PFM operation is adopted at heavy load. Fig. 2 shows schematic of the PFM control strategy. The variation of load current or output voltage V_{IN} can be detected by EA, the output voltage of EA controls the VCO to adjust switching frequency. The non-overlap clock, the clock encoder and the drive circuit are utilized to drive switch of the SC array. The VCO operates from 2 MHz to 20 MHz to maintain against input voltage and load current change.

The analog switching frequency modulation completes small output voltage ripple and high precision. However, the GBW of the PFM operation decreases at light load, so the slow transient response leads to large overshoot or undershoot of the output voltage V_{OUT}. PFM also has a problem of the system stability analysis, particularly, small signal mode of SC array is not given, it will be discussed in section 2.3.

2.1.2. Burst mode control

Burst mode is realized for improving transient response and power efficiency at light load in the proposed SC DC-DC converter. The operating principle can be introduced as follows: When switching frequency is smaller than 2 MHz VCO turns off and V_{OUT} decreases, when V_{OUT} is lower than reference voltage V_{REF2} ($V_{REF2}<V_{REF1}$), VCO turns on. Burst mode realizes output regulation with the discrete VCO operation, control losses decreases at light load.

Fig. 3 shows time diagram of the switching signal and output voltage at burst mode. Φ_1 and Φ_2 are non-overlap switching frequency. The output voltage is detected by comparator, so the fast transient response is achieved at light load. Control circuit turns off except comparator for V_{OUT} detection when VCO turns off, compared with PFM at light load, the control losses decreases at burst mode.

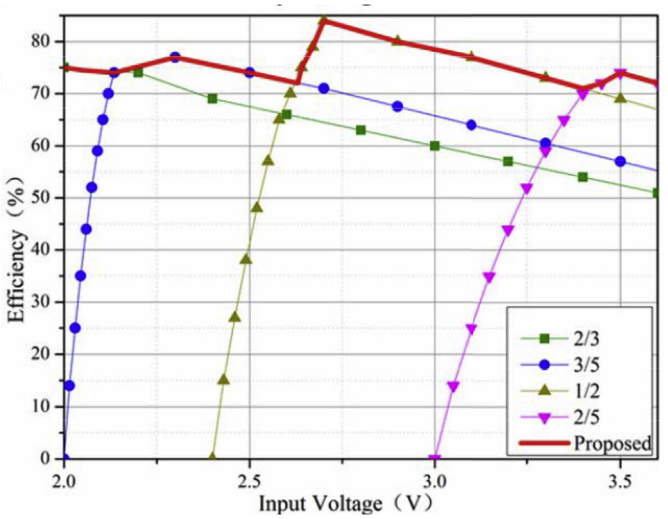

Fig. 5. Power efficiency of the proposed SC DC-DC converter at a 2 mA load current.

2.1.3. Performance analysis

There are mainly conduction losses, switching losses and bottom plate parasitic capacitance losses associated with the SC DC-DC converter at heavy load. All the power losses can be expressed by:

$$P_{Losses} = P_{Cond} + P_{Switch} + P_{Bottom} \quad (1)$$

where P_{Cond} is conduction losses, P_{Switch} is switching losses and P_{Bottom} is bottom plate parasitic capacitance losses. All the power losses at PFM operation is basically the same as that at burst mode, however, control losses becomes dominant at light load, so the power efficiency is improved by reducing control losses at burst mode.

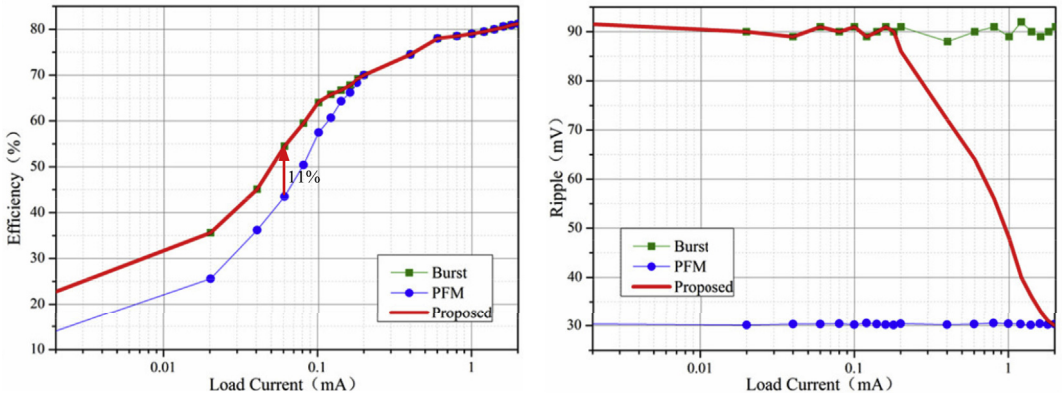

Fig. 4. Simulation results at dual mode (a) average power efficiency (b) average ripple.

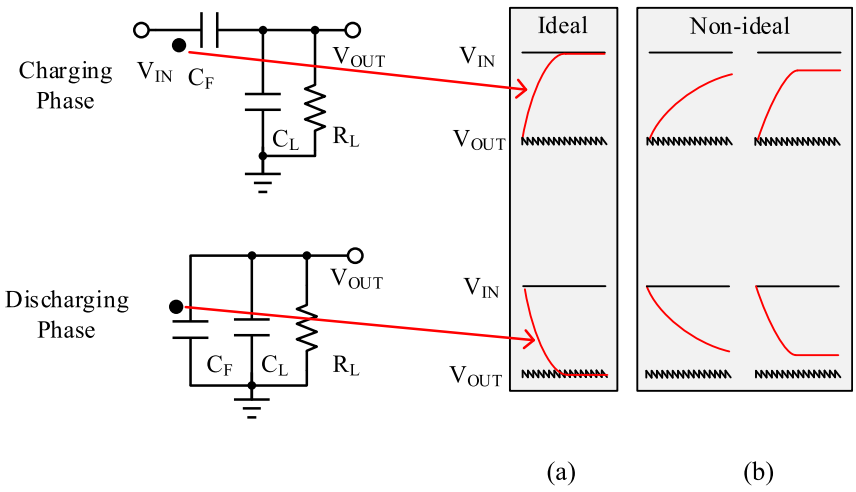

Fig. 6. Waveforms of the top plate of flying capacitor at ratio = 1/2. (a) Ideal. (b)Non-ideal.

For PFM operation, output voltage ripple is related to input voltage and output voltage at a given conversion ratio, it can be approximately expressed by:

$$V_{Ripple} = \frac{I_L T_S}{2C_L} = \frac{rC_F\left(\frac{n}{m}V_{IN} - V_{OUT}\right)}{2C_L} \quad (2)$$

where m/n is the conversion ratio.

Simulation results shows that the load current changes from 10 μA to 100 μA from a 2.7 V input supply, V_{OUT} gives a transient responses time of 113 μs and a dropout voltage of 350 mV at PFM operation, however, there is no dropout voltage of V_{OUT} for same load current changes and a fast transient response is achieved at burst mode operation. Fig. 4 (a) shows simulation results of average power efficiency at dual mode. Compared with PFM at light load, burst mode achieves an 11% maximum improvement of power efficiency at a 60 μA load current. Fig. 4 (b) shows simulation results of average ripple at dual mode. PFM achieves 30 mV average ripple at heavy load. Dual mode control strategy not only effectively helps delivering a wide load current range but also obtains a good performance.

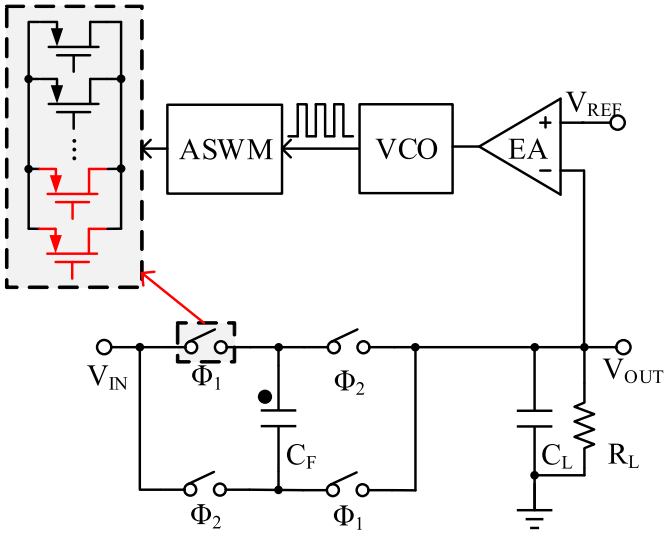

Fig. 7. Schematic of ASWM at ratio = 1/2.

Table 1
Interval division of the swith wdith of the SC array.

Frequency(MHz)	20–16	16–8	8–4	4–2	2
Width	10×	8×	4×	2×	1×

2.2. Reconfigurable SC array with adaptive switch width modulation (ASWM)

Fig. 5 shows the power efficiency of the proposed SC DC-DC converter at a 2 mA load current. The SC array has four ratios: 2/3, 3/5, 1/2 and 2/5, for a single conversion ratio, because switching losses and conduction losses are dominant, it is only efficient with a narrow input voltage range. To get high efficiency with a wide input voltage range, the proposed SC DC-DC converter utilizes series-parallel topology to complete a SC array of four ratios mentioned.

According to ideal model of the SC DC-DC converter [1], different switching frequency corresponds to different optimal switch width, but the switch width of the proposed SC array has been determined by the maximum switching frequency. ASWM is proposed to further optimize switch width for minimum switching losses tracking. Switching losses can be expressed by:

$$P_{Switch} = \frac{1}{2}C_{Gate}V_{IN}^2 f_S \quad (3)$$

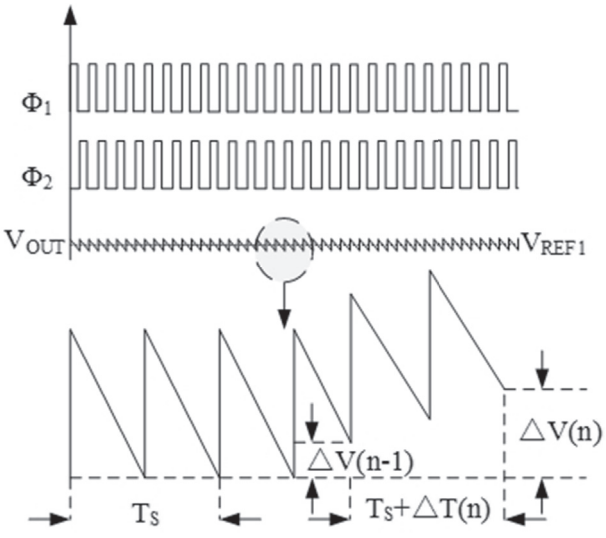

Fig. 8. Time diagram of the switching signal and output voltage at ratio = 1/2.

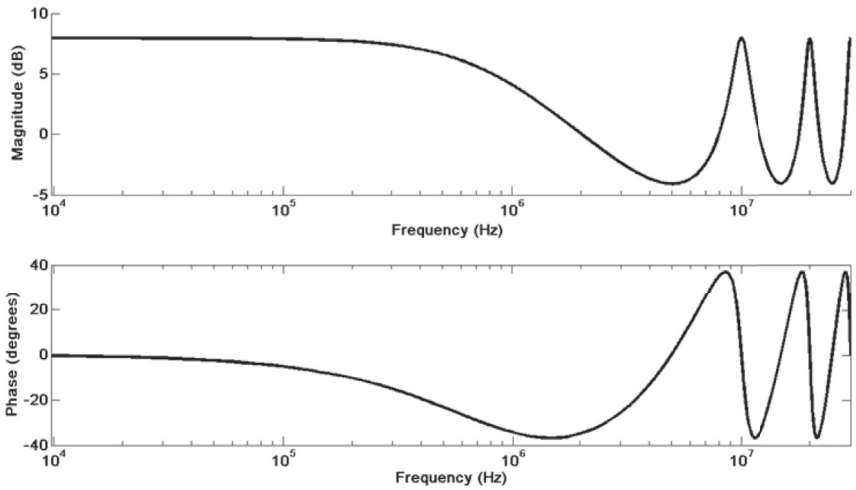

Fig. 9. Bode of the SC array at ratio = 1/2.

where C_{Gate} is gate-capacitance of the switch, V_{IN} is input voltage and fs is the switching frequency. C_{Gate} is proportional to switch width. When the load current decreases, the switching frequency decreases and switch width can be optimized to reduce switching losses.

The optimal switch width can be determined by whether it is completely charged and discharged. Fig. 6(a) shows ideal waveforms of the top plate of flying capacitor in the charging phase and the discharging phase at ratio = 1/2. Non-ideal waveforms are shown in Fig. 6(b), due to large on-state resistance of the switch, the charging and the discharging is insufficient. It is the basis of optimal switch width selection.

Fig. 7 shows the schematic of ASWM at ratio = 1/2. The variation of load current is tested by the EA, the EA controls the VCO to adjust the switching frequency, ASWM selects switch width of the SC array according to the switching frequency of the VCO. Minimum switching losses tracking is implemented with ASWM.

According to the switching frequency of the dual mode control strategy, the switch width can be divided into five parts (4×, 2×, 2×, 1× and 1×), it can be adjusted with the variation of the switching frequency. Table 1 shows the interval division of the switch width of the SC array. Simulation results shows that an 8% improvement of power efficiency is achieved from a 2.7 V input voltage supply at a load current of 2 mA.

2.3. System stability analysis at PFM operation

2.3.1. Small signal model of the SC array

Fig. 8 shows time diagram of the switching signal and output voltage at ratio = 1/2, the time constant of charging and discharging is much smaller than period of switching frequency. ΔV(n-1) and ΔV(n) are the variation of output voltage on n-1st and nth period respectively. ΔT(n) is the variation of time on nth period. The variation of output voltage can be expressed by:

$$\Delta V(n) - \Delta V(n-1) = V_{Charging} - V_{Discharging} \tag{4}$$

where $V_{Charging}$ is the increase of output voltage due to charge transfer from input to output, $V_{Discharging}$ is the decrease of output voltage due to power consumption. According to charge conservation, $V_{Charging}$ can be expressed by:

$$V_{Charging} = \frac{2(V_{IN} - 2(V_{OUT} + \Delta V(n-1)))C_F}{C_L} \tag{5}$$

where C_F is all flying capacitor, C_L is output capacitor. $V_{Discharging}$ can be expressed by:

Table 2
The pole of the four ratios of the SC array at $f = f_S$.

Ratio	2/3	3/5	1/2	2/5
ω_{sc}	$0.16f_S$	$0.13f_S$	$0.15f_S$	$0.1f_S$

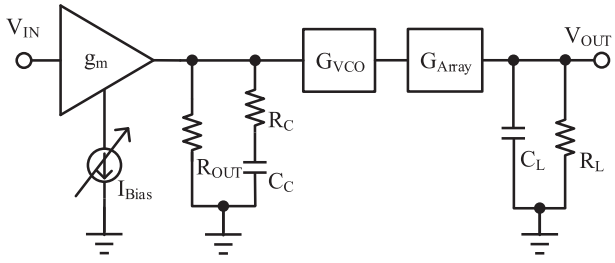

Fig. 10. Small signal modeling of the proposed SC DC-DC converter.

$$V_{Discharging} = \frac{\left(V_{OUT} + \frac{1}{2}(\Delta V(n) + \Delta V(n-1))\right)(T_S + \Delta T(n))}{R_L C_L} \tag{6}$$

where R_L is load resistor, T_S is switching period.

Combining (3), (4) and (5), consider the first order of the equation, it can be expressed by:

$$\Delta V(n)\left(1 + \frac{T_S}{2R_L C_L}\right) + \Delta V(n-1)\left(1 - \frac{4C_F}{C_L} - \frac{T_S}{2R_L C_L}\right) = -\Delta T(n)\frac{V_{OUT}}{R_L C_L} \tag{7}$$

From s-transform of equation (7), the transfer function of the SC array can be obtained by:

$$\frac{\Delta V(s)}{\Delta T(s)} = -\frac{\frac{V_{OUT}}{R_L C_L}}{1 + \frac{T_S}{2R_L C_L} + e^{-sT}\left(1 - \frac{4C_F}{C_L} - \frac{T_S}{2R_L C_L}\right)} \cdot \frac{1 - e^{-sT}}{sT} \tag{8}$$

Here the capacitance is 500 pF and 5 nF for C_F and C_L respectively. Fig. 9 shows bode of equation (8). Further, equation (8) can be expressed by:

$$\frac{\Delta V(s)}{\Delta T(s)} = -\frac{V_{OUT} f_S}{25} \cdot \frac{1 - e^{-sT}}{\left(1 - \frac{3}{5}e^{-sT}\right)sT} \tag{9}$$

where f_S is the switching frequency. Therefore, the transfer function of the SC array can be approximately expressed by:

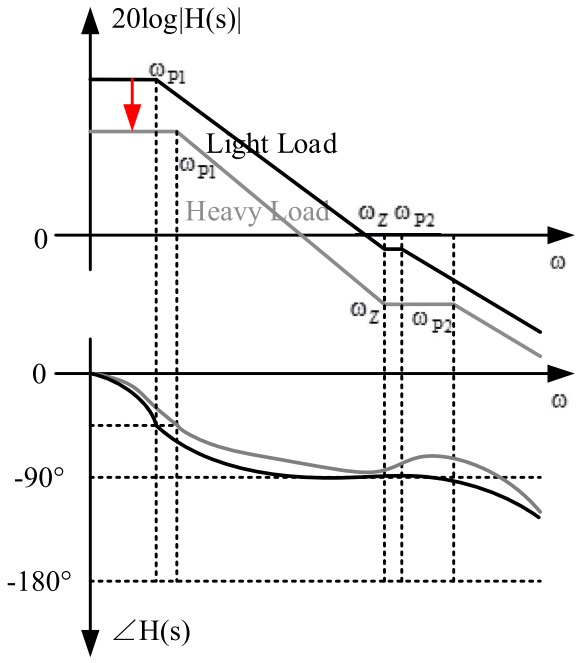

Fig. 11. Loop gain of the proposed SC DC-DC converter.

$$\frac{\Delta V(s)}{\Delta f(s)} = \frac{V_{OUT}}{25 f_S} \cdot \frac{1}{1+\frac{s}{\omega_{SC}}} \tag{10}$$

where ω_{sc} is equal to $0.15 f_S$.

Table 2 shows the poles of the four ratios of the SC array at $f = f_S$. ω_{sc} obtains minimum at ratio = 2/5. The transfer function of the SC array has completed with linear model, system stability analysis of the proposed SC DC-DC converter discussed as follows.

2.3.2. System stability analysis of the proposed SC DC-DC converter at PFM operation

Fig. 10 shows small signal model of the proposed SC DC-DC converter with compensation. R_{OUT} is output impedance of EA, the compensation consists of R_C and C_C. G_{VCO} is the gain of VCO and G_{Array} is the gain of SC array. The transfer function of the SC DC-DC converter can be expressed in:

$$H(s) = \frac{A_{DC}(1+sR_CC_C)}{(1+sR_{OUT}C_C)\left(1+\frac{s}{\omega_{SC}}\right)} \tag{11}$$

where A_{DC} is the low frequency gain, it can be expressed by:

$$A_{DC} = g_m R_{OUT} G_{VCO} G_{Array} \tag{12}$$

the dominant pole is given as:

$$\omega_{P1} = \frac{1}{R_{OUT}C_C} \tag{13}$$

Hence, the GBW can be expressed by:

$$GBW = \frac{G_{VCO}G_{Array}g_m}{C_C} \tag{14}$$

and the non-dominant pole located at the SC array and the zero can be expressed by:

$$\omega_{P2} = \omega_{SC} \tag{15}$$

$$\omega_Z = \frac{1}{R_CC_C} \tag{16}$$

Fig. 11 shows loop gain of the SC DC-DC converter. The relative position of poles and zero can be observed. The bias current of EA is controlled by load current. Therefore, the GBW can be increased by the adaptive bias current. It can be observed that non-dominant pole and

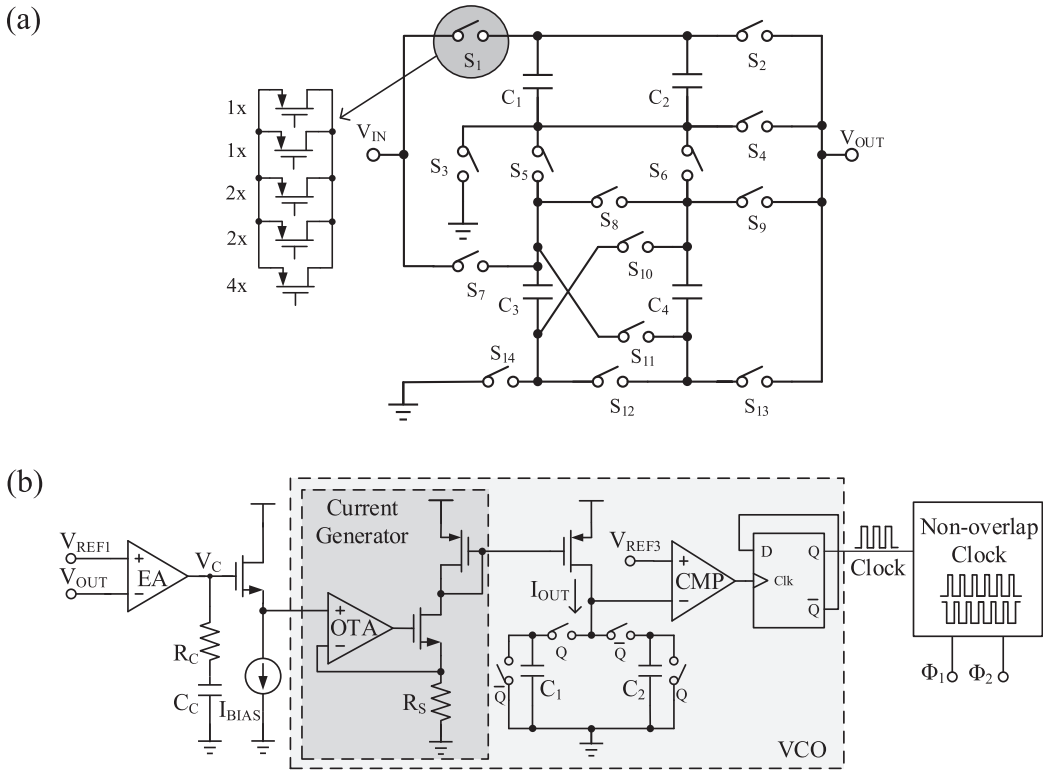

Fig. 12. (a) Reconfigurable SC array of proposed SC DC-DC converter. (b) PFM control circuit.

Table 3
Switching signals of the proposed SC array.

Ratio	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}
2/3	Φ_1	Φ_2	Φ_2	off	Φ_1	Φ_1	off	off	Φ_2	off	Φ_2	Φ_1	Φ_1	Φ_2
3/5	Φ_1	Φ_2	Φ_2	Φ_1	off	off	Φ_1	on	Φ_2	off	off	on	Φ_1	Φ_2
1/2	Φ_1	Φ_2	off	Φ_1	Φ_2	Φ_2	Φ_1	off	off	Φ_1	off	Φ_2	Φ_1	Φ_2
2/5	Φ_1	Φ_2	off	Φ_1	Φ_2	Φ_2	Φ_1	Φ_1	off	off	off	on	Φ_1	Φ_2

Table 4
GBW, ω_{p2} and ω_z location at a 2–20 MHz switching frequency.

Parameter	Range
GBW	14.3 KHz-45.6 KHz
ω_{p2}	31.8 KHz-509.5 KHz
ω_z	27.2 KHz

zero cancel each other at light load. When load current increases, the loop gain decreases and the zero is much smaller than non-dominant pole at heavy load, the phase margin is enhanced. The non-dominant ω_{P2} is always higher than 2.2 GBW to ensure the stability of the SC DC-DC converter.

3. Circuit implementation

3.1. Reconfigurable SC array

Fig. 12 (a) shows the reconfigurable SC array of the proposed SC DC-DC converter. There are four same capacitors and fourteen transistors of power switch, the optimization of power switch width has completed according to ideal model [1]. Four conversion ratios (2/3, 3/5, 1/2, 2/5) are realized for a 2–3.6 V input voltage range, conversion ratio is controlled by 2-bit signal V_{High} and V_{Low} which are generated from ratio hop circuit. Every switch width is divided into five parts for ASWM. (1×, 1×, 2×, 2× and 4×).

Table 3 shows switching signals of the SC array, where Φ_1 and Φ_2 are charging and discharging switching signals of flying capacitors respectively. On and off represent power switch turn on and turn off respectively.

3.2. Pulse frequency modulation (PFM) control circuit

Fig. 12 (b) shows the implementation of PFM control circuit, it contains EA, VCO and non-overlap clock circuit. V_C controls VCO to generate the switching frequency for SC array to transfer charge. According to system stability analysis at PFM operation in section 2, Table 4 summaries the GBW, ω_{p2} and ω_z location at a 2–20 MHz switching frequency.

VCO is the core control circuit at PFM operation. It is composed of current generator, CMP and D flip-flop. In one half cycle, Q = 1, C_1 is charged to V_{C1} and C_2 is connected to ground, D flip-flop reverses at $V_{C1}>V_{REF3}$. In another half cycle, Q = 0, C_2 is charged to V_{C2} and C_1 is connected to ground, D flip-flop reverses at $V_{C2}>V_{REF3}$. The switching frequency f_S can be expressed by:

$$f_S = \frac{I_{OUT}}{2CV_{REF3}} \tag{17}$$

where I_{OUT} is the charging current to C_1 or C_2.

Fig. 13 shows the implementation of EA. The transistors M_{P3}, M_{P4}, M_{P5} and M_{P6} are switches. The transistors M_{N9} and M_{N10} are connected to input voltage. When RST = 1, V_{REF1} is connected to the gate of the M_{N10}, the M_{P3} and the M_{P4} turn on, the M_{P5} and the M_{P6} turn off, the amplifier works as the error amplifier at PFM operation. When RST = 0, V_{REF2} is connected to the gate of the M_{N10}, the M_{P5} and the M_{P6} turn on, the M_{P3} and the M_{P4} turn off, the amplifier works as the comparator at burst mode

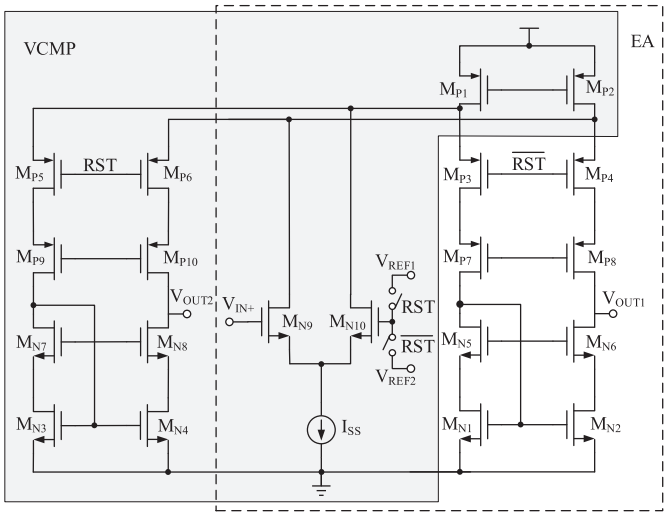

Fig. 13. Proposed error amplifier.

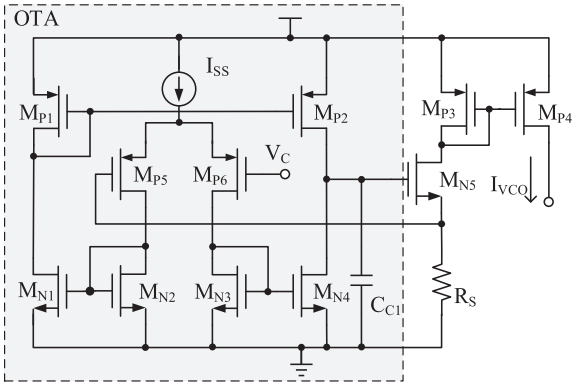

Fig. 14. Proposed current generator.

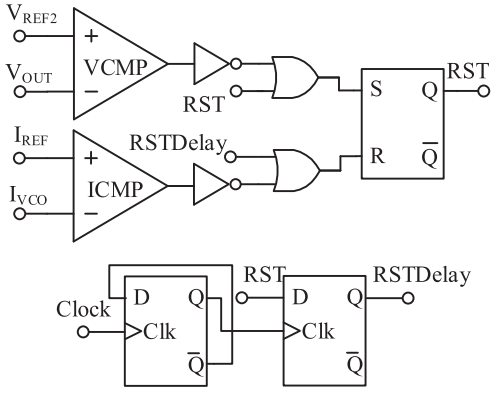

Fig. 15. Burst mode control circuit.

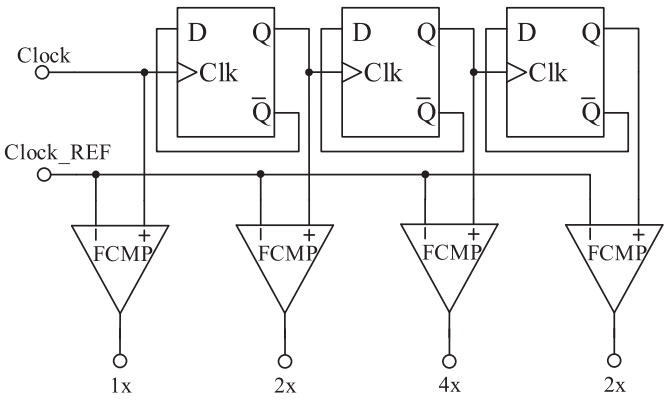

Fig. 16. Switching frequency detection circuit.

operation. The same offset voltage guarantees operating stability for mode selection.

The current generator circuit is shown in Fig. 14. V_C is connected to the gate of M_{P6}, the top of the resistor R_S is connected to the gate of the M_{P5}, the bottom of the R_S is connected to ground. System stability analysis is achieved with compensation C_{C1}, the current I_{VCO} can be expressed by:

$$I_{VCO} = \frac{V_C}{R_S} \tag{18}$$

3.3. Burst mode control circuit

Fig. 15 shows burst control circuit at light load. It consists of the ICMP, the VCMP, the RS flip-flop and the 2-bit divider. The ICMP is the current comparator. The VCMP is the amplifier shown in Fig. 13 at RST = 0. When $I_{VCO} < I_{REF}$, RST = 0, the control circuit turns off, the output voltage begins to decrease. When $V_{OUT} < V_{REF2}$, RST = 1, the VCO starts up, the output voltage begins to increase, the reference voltage V_{REF1} and V_{REF2} are 1.2 V and 1.15 V respectively.

The signal RST Delay avoids stopping converter. When $V_{OUT} < V_{REF2}$, VCO starts up and the I_{VCO} is still smaller than the I_{REF}, VCO need enough time to initialize before the ICMP starts up. The delay time can be expressed by:

$$T_{Delay} = \frac{1}{f_S} \tag{19}$$

3.4. Adaptive switch width modulation (ASWM) circuit

The switch width is controlled through comparing reference switching frequency Clock_REF with switching frequency Clock and its

Table 5
Interval division of the input voltage range.

Ratio	2/3	3/5	1/2	2/5
V_{IN}(V)	(2.0, 2.2)	(2.2, 2.5)	(2.5,3.3)	(3.3, 3.6)

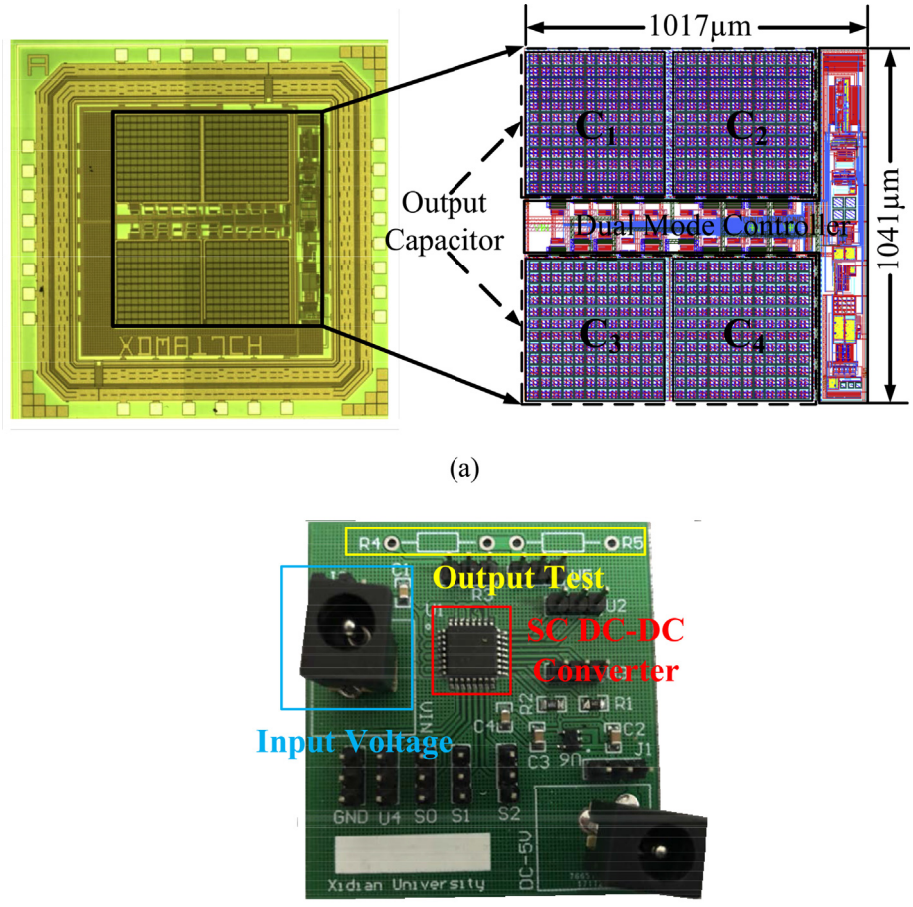

Fig. 17. (a) The die photo of the proposed SC DC-DC converter (b) The test PCB board.

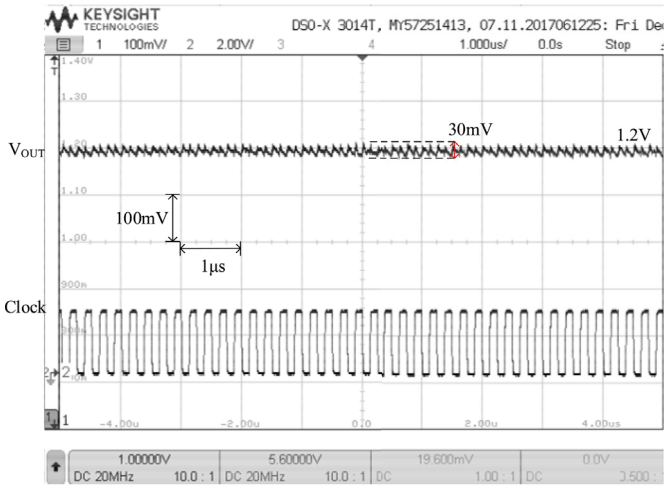

Fig. 18. Measured performance at PFM operation.

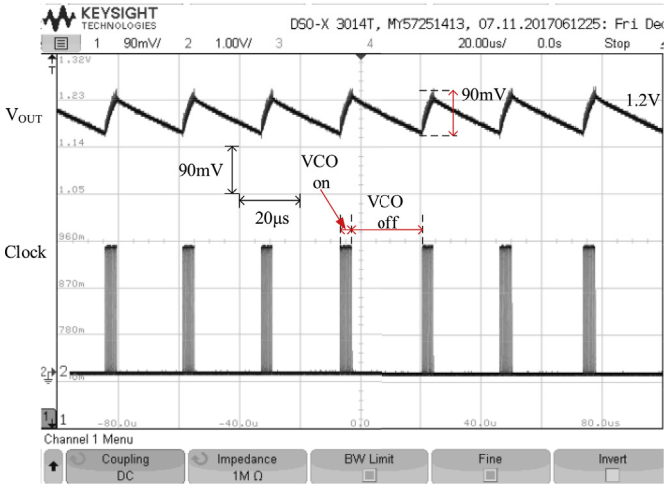

Fig. 19. Measured performance at burst mode operation.

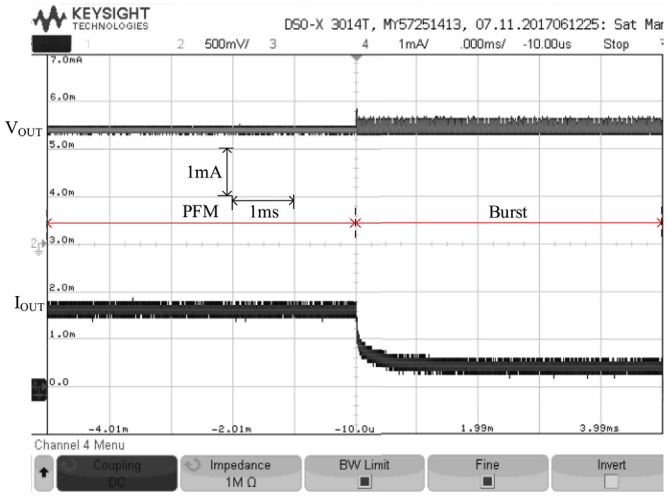

Fig. 20. Measured load transient waveform at dual mode operation.

fractional signals respectively. The FCMP is the switching frequency comparator, the Clock_REF is 2 MHz. Fig. 16 shows switching frequency detection circuit for adaptive switch width modulation.

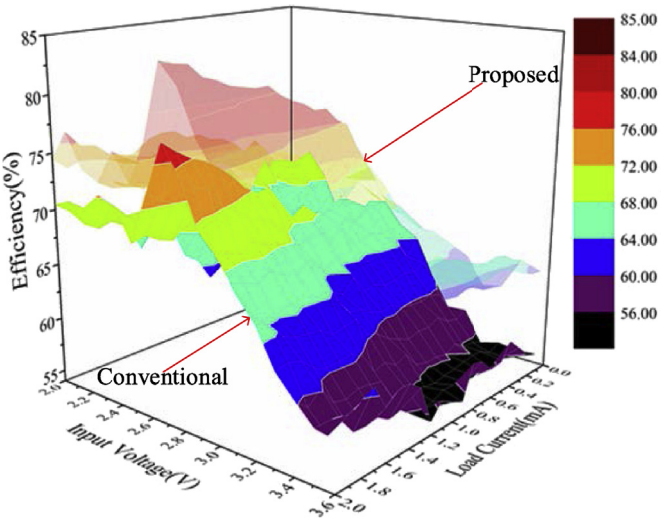

Fig. 21. Measured power efficiency of the proposed SC DC-DC converter.

Table 6
Comparison with recently published SC DC-DC converter.

Work	2016 [7]	2016 [12]	2016 [18]	2012 [19]	2011 [22]	This work
Technology	65 nm	180 nm	65 nm	90 nm	130 nm	180 nm
Topology	1/1,3/4 2/3	4/1	1/1,3/4 2/3,1/2	2/3,1/3	1/1,2/3 1/3	2/3,3/5 1/2,2/5
V_{IN} (V)	0.6–1.2	0.39–0.43	1.2	1.2	1.2/ 0.3–1.1	2.0–3.6
V_{OUT}(V)	0.6,0.8,1	1	0.6–1	0.755, 0.32	0.3–1.1	1.2
f_S(Hz)	13 M	17M-23 M	12 M	NR	500K-6.9 M	2M-20 M
C_F	675 pF	NR	675 pF	5 nF	350 pF	500 pF
$P_{OUT,Max}$	800 µW	1.1 mW	1 mW	1 mW	230 µW	2.4 mW
Peak efficiency	80%	70%	83%	75.3%	80%	84.2%
Output capacitor	off-chip	Off-chip	off-chip	off-chip	off-chip	on-chip

4. Measured results

The proposed SC DC-DC converter has been fabricated in 0.18 µm CMOS process. The die photo of the proposed SC DC-DC converter with active area of 1017µm × 1041 µm and the test PCB board are shown in Fig. 17. Flying capacitance (C_1, C_2, C_3 and C_4) is 500 pF MIM and output capacitance is 5 nF MOS (shown in Fig. 17 dotted box).

The output voltage of the proposed SC DC-DC converter is fixed at 1.2 V. According to conversion ratios, the interval division of the input voltage range is shown in Table 5. A 50 mV hysteretic interval between two ratios is introduced to ensure stability of output voltage.

Fig. 18 shows the measured transient waveform at PFM operation. A 2 mA load current is given at a fixed 2.7 V input voltage. The output ripple is approximately 30 mV. The bias current of EA depends on switching frequency, the measured results show that the fast response time is achieved when load current changes. The load current range is 1.8–2 mA for a 2.0–3.6 V input voltage range at PFM operation.

Fig. 19 shows the measured transient waveform at burst mode operation. The load current is 200 µA and switching frequency is about 2 MHz when VCO turns on, output ripple is close to 90 mV. Burst mode realizes output regulation with discrete VCO operation. Improvement of the power efficiency and transient response are achieved at light load.

Fig. 20 shows measured load transient waveform at dual mode

operation. The load current I_{OUT} changes from 1.7 mA to 400 μA, VCO operating condition can be detected by test signal RST. The measured results show that the converter operates normally from PFM to burst mode, and vice versa. The load current range is effectively extended at dual mode operation.

The switching losses and the conduction losses are dominant in the conventional SC DC-DC converter, the optimal power efficiency should consider both of them. Control losses seriously impacts power efficiency at light load. Fig. 21 shows measured power efficiency of the proposed SC DC-DC converter. The peak efficiency is as high as 84.2% from a 2.7 V input supply and 2 mA load current at ratio = 1/2. Burst mode not only effectively enlarges load current range, but also reduces control losses for improving power efficiency. Improvements of 6% for the average power efficiency is achieved with adaptive switch width modulation.

Table 6 shows a comparison with recently published SC DC-DC converter. Reconfigurable SC array is inevitable for a wide input/output voltage range. The proposed SC DC-DC converter achieves a 0–2 mA current range for a 2.0–3.6 V input voltage range, the power density is 2.4 mW/mm^2 for 84.2% peak power efficiency.

5. Conclusion

This paper presented the detailed design, the circuit implementation and the measured results for a step-down SC DC-DC converter. Firstly, a reconfigurable SC array has four conversion ratios for a 2.0–3.6 V input voltage range. Secondly, a dual mode control strategy is proposed for output regulation, PFM is adopted to complete small output voltage ripple at heavy load while burst mode is adopted to improve load transient and power efficiency at light load. Thirdly, ASWM is proposed to further improve power efficiency over the entire load range. The peak efficiency of the proposed SC DC-DC converter is 84.2% from a 2.7 V input voltage supply at a load current of 2 mA. In conclusion, this paper proposed a high performance SC DC-DC converter for ultra-low power portable devices.

Acknowledgments

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