Thermal Optimization of Electronic Devices on PCB Based on the Ant Colony Algorithm

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***Abstract*—With the integration of the electronic devices on the printed circuit board, the heat flux density in narrow spaces is increasing rapidly. The placement of electronic devices can affect the temperature of the overall circuit board. In addition, some special devices usually need to meet many location requirements. For example, the devices such as FPGAs, ARMs and MCUs need to be placed in the central position of the PCB for the use of multiple peripheral circuits. In order to optimize the temperature of devices with a priori layout requirement, this paper uses the micro-element thermal equilibrium method to establish the temperature field model and then the ant colony algorithm with classified compensation is used to search optimized position of all components. Simulation experiment results show that the proposed algorithm can effectively reduce the maximum temperature of devices in the case of the electronic devices meet the needs of the circuit function.**

Keywords-heat flux density; priori; micro-element thermal equilibrium; ant colony algorithm

I. INTRODUCTION

The thermal stress of the system will be enlarged with the increase of heat flux in the circuit board [1], resulting in a significant increase of the circuit failure rate. However, electronic engineers usually neglect the steady-state temperature variety caused by the placement of components or just simply separate the chips with high power consumption. In addition, we can also use computer simulation software to calculate the temperature, such as Flotherm [2]. However, it's difficult to deal with the overlapping region when the number of components is significant and the range of optimization are relatively large.

In order to overcome these questions, many layout optimization algorithms have been researched which can be divided into optimization algorithm and heuristic algorithm. The optimization algorithms take advantage of operational research knowledge and can get the optimal solution of the layout accurately. However, when the PCB area is large, the time complexity is also high. The heuristic algorithm can discover the sub optimal solution of the feasible solution space by guiding rules under the acceptable cost of the system. In a complex scene, heuristic algorithms are more suitable for engineering applications such as genetic algorithms [3, 4], simulated annealing algorithms [5] and ant colony algorithms [6, 7].

Based on the principle of heuristic optimization, many PCB layout optimization methods have been proposed. Bogula, Chermoshencev and Suzdaltsev [8] is devoted to the development and study of evolutionary algorithms for solving multi-objective problems of high-speed digital electronic PCB design. Ismail and Yusof [9, 10] choose the Weighted-sum approach to consider the temperature and the inter-connection between each component, but perhaps some devices not only have high power consume but also should be put the central position. Alexandridis, Paizis, Chondrodima and Stogiannos [11] developed an approach dealing with the continuous nature placement in PCB thermal design based on the particle swarm optimization. The above algorithms can solve the device layout problem in a certain scene, but does not consider the existence of a priori layout constraints between the devices on the printed circuit board.

In this paper, we propose a new partial grid model method and use the ant colony algorithm to optimize the layout of devices. For the actual requirements of the component, we place them in the designated area. Some components have a "package" relationship, which need to be placed in the adjacent area. Other components without specific location restrictions can be placed over a large area. In addition, in order to avoid the local optimal solution, this paper use the ant colony method with classified compensation. Finally, the Flotherm simulation experiments show that the optimized device placement can effectively reduce the maximum temperature and average temperature on the printed circuit board, which proves the validity of our algorithm.

II. ANT COLONY ALGORITHM

This paper uses ant colony algorithm to heuristically search the placement of electronic devices. In the work [12] Ant colony algorithm was proposed to solve optimal problem because of the good positive feedback, parallel computing and robustness. It has obvious advantages over other heuristic methods in solving combinatorial optimization problems with more nodes.

In ant colony system, all n nodes are regarded as n different cities. Each ant starts from the first city to the nth city. We can consider that different routes serve as a different combination program. When ants walk through a city, they will leave some pheromones τ in their place. The pheromones on each city are the pheromones left by all

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passing ants and will volatilize over time. The visibility η of next city for ants depends on the distance between different cities. Each ant will select the next city by the pheromone and visibility of cities. The transition probability between city i and city j is as follow:

$$P_{ij}(t) = \frac{[\tau_{ij}(t)]^{\alpha} \cdot [\eta_{ij}(t)]^{\beta}}{\sum_{s \in allcity} [\tau_{is}(t)]^{\alpha} [\eta_{is}(t)]^{\beta}} \tag{1}$$

After all ants have traveled all cities, we choose a better path based on the objective optimization function. And then the path of pheromone can be adjusted as follow:

$$\tau_{ij}(t+1) = (1-\rho)\tau_{ij}(t) + \Delta\tau_{ij}(t) \tag{2}$$

where the ρ is the volatility, $\Delta\tau(t)$ is determined by the better path. Then we only need to iterate through the loop until the final solution can meet some conditions to terminate the iteration.

III. Devices Layout Algorithm With Priori Constraints

In this section, considering that the component on the PCB have priori layout requirements, we propose a new partial grid model method where every component have their own optimizing regions as the diverse circumstances may require.

A. *The Principle of PCB Modeling*

Under normal circumstances the device placement model makes the number of PCB grid equal to the number of devices[13]. As shown in Fig. 1(a), each device is placed on a grid. In this case, we can optimize the device order to reduce the temperature of devices.

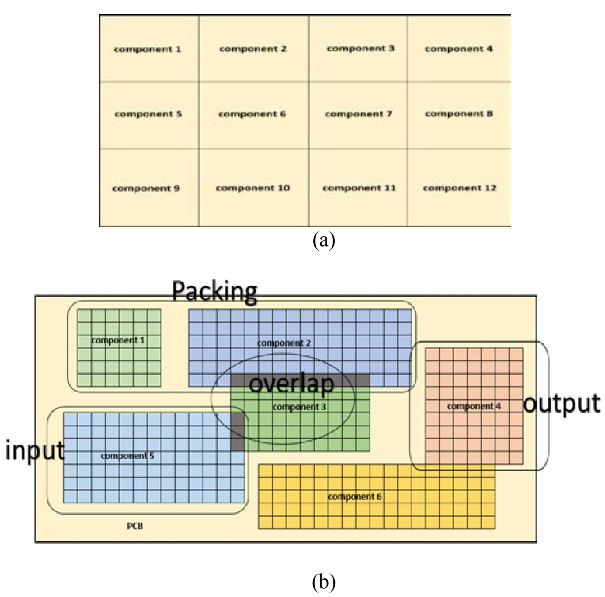


Figure 1. Examples of two PCB models: (a) the device placement model under normal circumstances. (b) the device placement model with priori layout requirements.

In this paper, we place each device into a designated corresponding optimization area based on the actual requirements of the engineers. As shown in Fig. 1(b), some devices are the nuclear part of the control circuit, which need to be placed in the center of the PCB. Some devices have a "package" relationship, which need to be placed in the vicinity. And then some devices, which have to connect the input and output interfaces, need to be placed in the edge position. Devices without special position constraints can specify a larger area. Each region of component can cover the entire or a small part of other areas. In the meantime, every region can be divided into smaller grids, which are used to get the specific location.

B. *The Temperature Calculation for Devices on PCB*

In order to optimize layout by ant colony algorithm, we need to build an objective function such as the maximum temperature, the minimum temperature or the average temperature of components on the PCB. As a result, we need to establish a temperature model for a PCB.

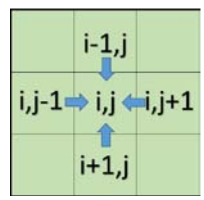


Figure 2. Heat transfer between each grid and the surrounding grid.

we use micro-element thermal equilibrium method[13] to compute the temperature of the PCB.As shown in Fig. 2, the heat flowing into the node equals to the heat flowing out of the node in the steady state. There are five heat exchange paths between a grid and the surrounding grids. In addition, each device has different power consumption according to the chip manual. In summary, each small square can list the energy balance equation under steady-state conditions as:

$$Q_{i+1,j} + Q_{i-1,j} + Q_{i,j+1} + Q_{i,j-1} + Q_{air\_i,j} + S_{i,j} = 0 \tag{3}$$

where the heat transfer from $(i+1, j)$ to (i, j) can be expressed as:

$$Q_{i+1,j} = \frac{\Delta T}{R_{i+1,j}} \tag{4}$$

where ΔT is the temperature difference between two grids, $R_{i+1,j}$ is the heat resistance between the two grids.

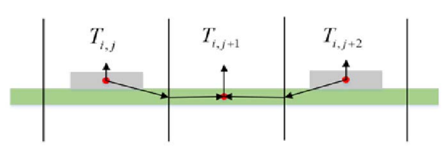


Figure 3. Thermal conduction path between the grids.

As shown in Fig. 3, in our PCB grid model, some grids have components and other grids don't have components. Therefore, the thermal resistance between adjacent grids is related to the specific placement of the components. The calculation point of the grid with a component is set to the component center therefore we need to consider the thermal resistance between component and PCB. The calculation point of the grid with no component is in the middle of the PCB. The thermal resistance between the grid in the x direction is:

$$R_{i,j+1} = R_{p_{i,j}} + \frac{L_{grid\_x}}{\lambda_p \cdot L_{grid\_y} \cdot h_p} + R_{p_{i,j+1}} \quad (5)$$

where $R_{p_{i,j}}$ and $R_{p_{i,j+1}}$ is the thermal resistance between the component and the PCB located in the grid (i, j) and $(i, j+1)$. They will be set to 0 if there is no component on the grid. L_{grid_x} and L_{grid_y} are the length of grid in x and y directions. λ_p and h_p is the thermal conductivity and the height of the PCB board. Similarly, we can calculate the heat transfer in other directions. In addition, the convection heat flow between the grid and the air can be expressed as follows:

$$Q_{air\_i,j} = \begin{cases} \dfrac{T_{air} - T_{i,j}}{R_{top}} & \text{an component} \\ a_p \cdot L_{grid\_x} \cdot L_{grid\_y} \cdot (T_{air} - T_{i,j}) & \text{no component} \end{cases} \quad (6)$$

where R_{top} is the thermal resistance between component and air. a_p is the convection exchange coefficient of the air.

According to the equations (3)-(6), we can deduce the temperature equation similarly for each grid as follows:

$$\begin{aligned} &\left(\frac{T_{i,j+1}}{R_{i,j+1}} + \frac{T_{i,j-1}}{R_{i,j-1}} + \frac{T_{i-1,j}}{R_{i-1,j}} + \frac{T_{i+1,j}}{R_{i+1,j}}\right) \\ &= \left(\frac{1}{R_{i,j+1}} + \frac{1}{R_{i,j-1}} + \frac{1}{R_{i-1,j}} + \frac{1}{R_{i+1,j}} + \frac{1}{R_{air}}\right) \times T_{i,j} - \frac{T_{air}}{R_{air}} - S_{i,j} \end{aligned} \quad (7)$$

Finally, we can get the temperature data for each grid through computing a linear system of equations.

C. Devices Layout Optimization Based Ant Colony Method under P riori Layout Restriction

Through the above sections, we have completed PCB modeling and temperature calculation under the priori layout constraint. After that, we use ant colony algorithm to heuristically optimize the device placement.

Firstly, we put each component in its own optimizing region. Then we stipulate that each ant walks in the order of region 1, region 2, region 3, etc. Initially, we put m ants randomly on the small grid of region 1. The moving probability that the ant travels to the small grid in next region can be show as follow:

$$P_{ij}^{k}(t) = \begin{cases} \dfrac{[\tau_{ij}^{k}(t)]^{\alpha} \cdot [\eta_{ij}(t)]^{\beta}}{\sum_{s \in C} [\tau_{is}^{k}(t)]^{\alpha} [\eta_{is}(t)]^{\beta}} & (C \in \text{next region}) \\ 0 & (\text{occupied}) \end{cases} \quad (8)$$

where i and j is respectively grid location in current and next region. τ_{ij} is pheromone between grid i and j. η is a visibility variable which can be set to the distance of two small grids. The larger the linear distance, the smaller the heat transfer between two components. S is the index of small grids in the next region. α and β represents the relative importance of residual pheromones and visibility information. k represents the transition probability of the kth region and there are a total of $n-1$ moving probabilities which need to be established when ants travel all the regions.

If the ants happen to be in overlapping positions of two or more regions, the moving probability of the occupied position should be set to 0 in the next region. According to the practical request of electronic engineers, we can choose average temperature, maximum temperature, minimum temperature of the devices or multi-objective optimization fitness function as an optimization indicator.

There are two temperature distribution conditions that we primarily concerned about. One is that the devices under this path are less than the maximum tolerable temperature. The other requirement is that the path is the best solution according to the objective function. In order to avoid the algorithm from getting caught in local optimization prematurely, we update the pheromone with classification compensation strategy. We divide the grid positions into three cases:

- A are the placements that satisfy the first condition.
- B is the placement that satisfies the second condition.
- C are the placements around B.

The pheromone in each small grid is correspondingly reduced according to a certain volatilization rate ρ. We can deduce the different pheromone compensation for three cases as follows:

$$\tau_{ij}^{k}(t+1) = \begin{cases} (1-\rho)\tau_{ij}^{k}(t) & (i,j,k \notin A,B,C) \\ (1-\rho)\tau_{ij}^{k}(t) + a\Delta\tau_{best} & (i,j,k \in A) \\ (1-\rho)\tau_{ij}^{k}(t) + b\Delta\tau_{best} & (i,j,k \in B) \\ (1-\rho)\tau_{ij}^{k}(t) + c\Delta\tau_{best} & (i,j,k \in C) \end{cases} (k \in [1, n-1]) \quad (9)$$

where in general, $b > c > a$ .Then we update the ansition probability based on the updated pheromone and iterate the process.

The ant colony algorithm under priori layout restriction is shown in Table I.

TABLE I. THE DETAILED STEPS FOR OUR ALGORITHM

Our method
● **Initialization** 1)Set the number of ants m , devices n and region partition. 2)Choose the objective function $F(r)$. 3)Set initialization parameters for ant colony: τ^0 , η , ρ , α , β . 4)Set initialization parameters for PCB: a_p , λ_p , R and let t =0.

- **While** $t+1<t_{\max}$ **do**
  1) Choose location $\mathbf{i}^t=\{i_1^1,i_2^1,\ldots,i_m^1\}$ on region 1 randomly.
  2) Let $p,q=1$.
  3) **While** $p \le n-1$ **do**
     i) **While** $q \le m$ **do**
        a)Calculate transition probability $P_{ij}^{p,t}$, **for** j in region $p+1$.
        b)Choose one grid randomly in next region by $P_{ij}^{p,t}$.
  3)Calculate temperature $\mathbf{T}_q^t$, **for** $q=1,\ldots,m$.
  4)Choose the best Route r^t from all ants according to $F(r)$.
  5)Update pheromones $\boldsymbol{\tau}^t$.
  6)Update the best layout for devices $r^{\mathbf{best}}$, **if** $F(r^t)\le F(r^{\mathbf{best}})$.
- **Final answer:** $r^{\mathbf{best}}$

IV. EXPERIMENT

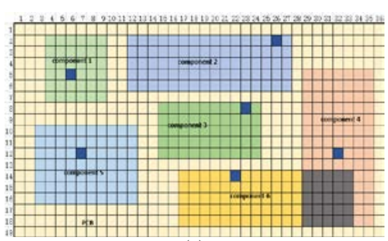
A. Parameters Setup

In this experiment, we choose six components with various power to test our algorithm. Their powers are set to 0.2W, 0.8W, 0.5W, 0.4W, 0.3W, 0.6W. The PCB board size is $18\text{cm}\times 9.5\text{cm}\times 0.08\text{cm}$ and the length of each grid is 0.5cm. We use MATLAB software to calculate the PCB temperature distribution and then use ant colony algorithm to optimize the placement of the components. At the same time, the Flotherm experiments are conducted to verify the results of mathematical model calculation.

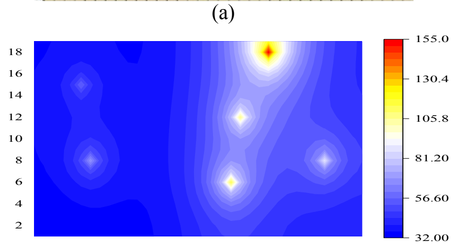
B. Experiments Results

We partition area for each device and randomly place electronic components on an initial location. Then we use ant colony algorithm under priori layout restrictions to get the optimized layout of devices.

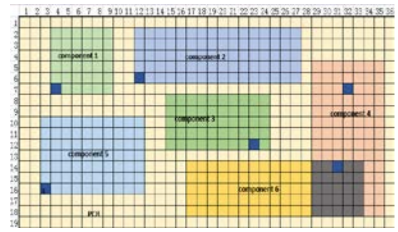
Fig. 5(a) and (c) show the layout of devices in the case of not optimized PCB and optimized PCB. The not optimized and optimized temperature map calculated by MATLAB are presented in Fig. 5(b) and (d) respectively.



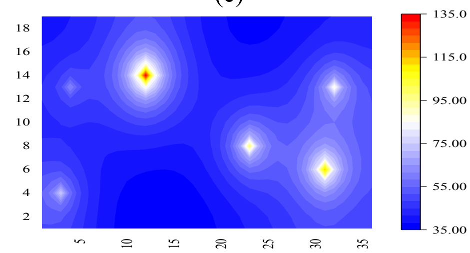
(a)



(b)



(c)

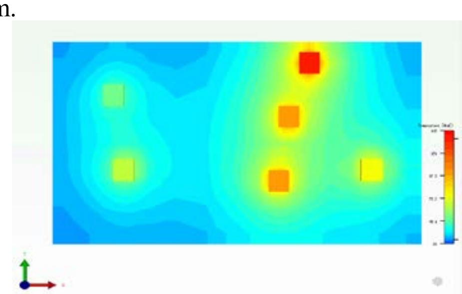


(d)

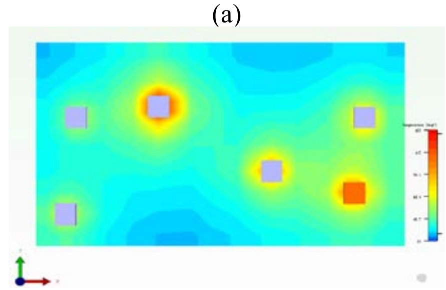
Figure 5. (a) not optimized layout. (b) not optimized PCB temperature by MATLAB. (c).optimized layout. (d) optimized PCB temperature by MATLAB.

It is easy to find that the not optimized placement of components is not ideal. The component 2 with higher power consumption is put to the edge of the PCB. And after 100 times iterations, the PCB board has a significant decline in the maximum temperature.

Fig. 6 shows the heat map of not optimized and optimized placements by the Flotherm software. We can see that the temperature trend in MATLAB is similar to Flotherm.



(a)



(b)

Figure 6. (a) not optimized PCB temperature map by Flotherm. (b) optimized PCB temperature map by Flotherm.

Table II and Table III show the temperature of devices by MATLAB and Flotherm respectively. We can see that after optimizing the layout, the maximum temperature of the components calculated by the Flotherm is reduced by $12\,°C$, the minimum temperature is increased by $2.73\,°C$ and the average temperature is decreased by 1.29 °C . The temperature calculated by Flotherm is lower than the mathematical model, but the relative temperature between the devices is essentially same. This is because that the mathematical model has made some simplification and ideal assumptions. In this paper, the optimization goal is to balance the temperature of all components. our algorithm has achieved the expected results.

TABLE II. TEMPERATURE OF DEVICES BY MATLAB AND FLOTHERM

Temperature of the component(°C)							
		one	two	there	four	five	six
Not optimized	**MATLAB**	56.78	154.79	107.01	87.33	68.43	113.51
	Flotherm	54.74	145.50	104.20	82.60	67.80	107.40
	difference	2.04	9.29	2.81	4.73	0.63	6.11
optimized	**MATLAB**	61.90	134.84	98.05	87.91	74.84	113.91
	Flotherm	57.47	133.50	104.40	81.25	69.15	108.70
	difference	4.43	1.34	-6.35	6.66	5.69	5.21

TABLE III. TEMPERATURE COMPARISON

Statistics temperature (°C)				
		max	min	average
Not optimized	**MATLAB**	154.79	56.78	97.97
	Flotherm	145.50	54.74	93.70
	difference	9.29	2.04	4.27
optimized	**MATLAB**	134.87	61.90	95.24
	Flotherm	133.50	57.47	92.41
	difference	1.37	4.43	2.83

V. CONCLUSION

In this paper, we propose a layout optimization algorithm for devices on PCB with prior constraints of devices' position. We introduce a refined PCB model method and use heuristic algorithm - ant colony algorithm with classification compensation strategy to optimize the device layout. After mathematical modeling and Flotherm software simulation experiments, we can see that the algorithm can effectively reduce the maximum temperature and average temperature of the electronic devices on the PCB.

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