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New SOI lateral power devices with trench oxide

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Abstract

We describe new SOI lateral power devices which have a trench oxide to improve the device performance. High-voltage super-junction (SJ) SOI-LDMOSFETs have a trench oxide in the drift region. It allows to reduce the drift length without degrading the breakdown voltage. With the proposed device structure a reduction of the on-resistance of the *n*-drift layer can be achieved. The breakdown voltage and the specific on-resistance of the suggested devices as a function of the trench oxide depth, the *p*-column width, and the doping are studied. Shorted-anode lateral insulated-gate bipolar transistors (SA-LIGBTs) on SOI have a trench oxide at the drain/anode region. It suppresses effectively the snap-back voltage inherent in conventional SA-LIGBTs without increasing the anode length of the device. Using the two-dimensional numerical simulator *Minimos-NT*, we confirm that the drift length of the proposed SJ SOI-LDMOSFETs is reduced to 65% compared to conventional devices, and a weak negative differential resistance region is observed with the proposed SOI SA-LIGBT.

1. Introduction

Lateral power devices on SOI (silicon on insulator) have attracted much attention in a wide variety of applications such as automotive electronics, consumer electronics, telecommunications, and industrial electronics [1]. Advantages of SOI technology are superior isolation, reduced parasitic capacitances and leakage currents, and superior high temperature performance compared to traditional junction isolation. These advantages allow efficient monolithic integration of multiple power devices and low-voltage control circuitry on a single chip. The main issues in the development of these devices are to obtain the best trade-off between the specific on-resistance (R_{SP}) and the breakdown voltage (BV) [2], and to shrink the feature size without degrading device characteristics. In order to fulfill these requirements new structures such as super-junctions [3], buried gate oxide devices [4], LUDMOSFETs [5], trench lateral power MOSFETs with a trench bottom source contact (TLPM/S) [6], the multi-channel approach [7], and hybrid SOI LDMOS-IGBT [8] have been proposed. Vertical SJ devices such as COOLMOS [9] and MDmesh [10] assume complete charge balance of the depletion layer. This can be achieved by introducing alternating *n*- and *p*-columns in the drift region, which allow to drastically increase the doping in this region. This results in a significant reduction in R_{SP} of the devices. Recently a lateral SJ SOI-LDMOSFET [11] which has a channel on the side wall of the device was proposed to improve on-state characteristics. The channel can be made by a lateral trench gate, which increases the channel area.

To obtain the best trade-off between R_{SP} and BV, we suggest a SJ SOI-LDMOSFET which has an extra *p*-column and a trench oxide in the drift region. The extra *p*-column is doped to achieve a balanced charge condition which means that the net depletion layer charge is zero. The trench oxide in the *p*-column helps to reduce the drift length without further decreasing the conduction area (only the *n*-column contributes to the current conduction). The R_{SP} of the proposed structure is

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effectively reduced by the SJ concept together with the trench oxide.

In order to reduce the chip size of the high-voltage ICs it is important to increase the current density of the output power devices. Lateral IGBTs on SOI have attracted much attention for high-voltage ICs and smart power applications, because they simultaneously handle high voltage and large current [12]. By means of dielectric isolation high-voltage LIGBTs on SOI allow to increase the operating current density due to minority carrier injection. However, this causes a slow turn-off time and a potential parasitic thyristor latch-up of the devices. One of the efficient methods to achieve fast switching is to introduce a shorted-anode structure to the LIGBT. The SA-LIGBT (shorted-anode LIGBT) offers design flexibility with respect to the trade-off between switching speed and on-resistance. The n^+ anode short provides an electron extraction path during turn-off. The major drawback of the SA-LIGBT is its negative differential resistance (NDR) region caused by the two different conduction mechanisms responsible for the current flow in the SA-LIGBT [13]. To suppress the NDR one needs to increase the p^+ anode length [14], but this results in a larger chip size. We propose a new SA-LIGBT which has a trench oxide at the drain/anode region. With this structure it is possible to reduce the snap-back voltage, and a similar turn-off time as that of the LDMOSFET can be obtained. Even the reverse characteristics of the proposed structure are similar to that of the conventional device. Two-dimensional numerical simulations with *Minimos-NT* [15] have been performed to investigate the influence of device parameters on the on-state characteristics, BV, and switching performance.

2. Device structures

Fig. 1 shows the schematic structure of the proposed SJ SOI-LDMOSFET which has a trench oxide in the drift region. With the structure proposed it is possible to reduce the drift length drastically without degrading the maximum BV by increasing the surface path of the drift layer. This buried *p*-column can be connected to the *p*-body directly or indirectly. The optimum *p*-column doping concentration is determined by the width of the *p*-column and the net charge of the *n*-column.

Our device is designed to achieve a BV of 300 V with an SOI thickness t_{soi} of 7.0 μm and with a buried oxide thickness t_{ox} of 2.0 μm. With these parameters the maximum BV of conventional SOI-LDMOSFETs is 300 V at the minimum allowable drift length of 20.0 μm. The trench oxide depth affects the BV, and it must be designed to ensure a long enough surface path of the device. It is important to minimize the *p*-column width, because it shrinks the conduction area of the device. The optimal *n*- and *p*-column doping concentrations depend on the column width. The *n*-column doping must be increased to lower the on-resistance of the SJ devices. Simulations are performed to find optimum device parameters with a trench oxide depth from 2.0 to 3.0 μm and a *p*-column width from 0.3 to 1.3 μm. With an *n*-column width W_N of 4.0 μm, a *p*-column width W_P of 0.3 μm and a drift length L_d of 13.0 μm the doping concentration of the *n*-column can be raised up to 6.0×10^{15} cm^{-3}. As shown in Fig. 2, the current of the proposed structure flows through the *n*-column and therefore shows clearly that only the *n*-column contributes to the current conduction.

Fig. 3 shows the schematic structure of the proposed SOI SA-LIGBT. The n^+ layer is introduced to the p^+ anode region to achieve a shorted-anode structure. As can be seen in the figure, the n^+ and p^+ are separated by the trench oxide. The device is designed to achieve a BV of 120 V with an SOI thickness t_{soi} of 2.0 μm and with a buried oxide thickness t_{ox} of 1.0 μm. The design parameters used for the simulations are listed in Table 1.

As shown in the table the *n*-drift length is 8.5 μm, the doping amounts to 1.0×10^{16} cm^{-3}, and the trench oxide

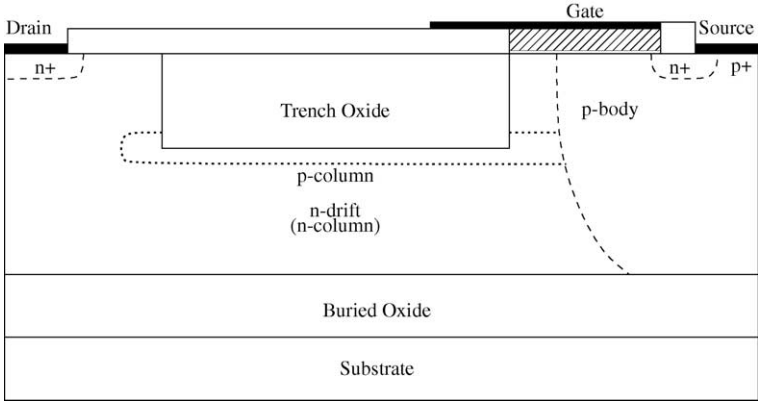

Fig. 1. Schematics of the SJ SOI-LDMOSFET with a trench oxide in the drift region.

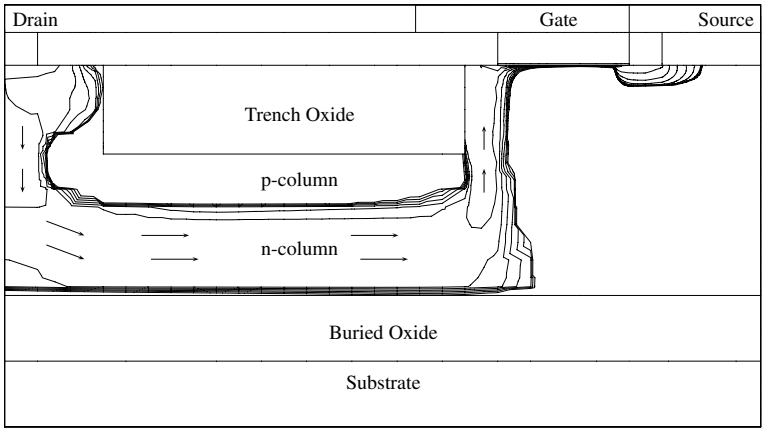

Fig. 2. Current distribution of a SJ SOI-LDMOSFET with a trench oxide at $V_{GS} = 15$ V and $V_{DS} = 20$ V. The arrows show the current flow in the drift region.

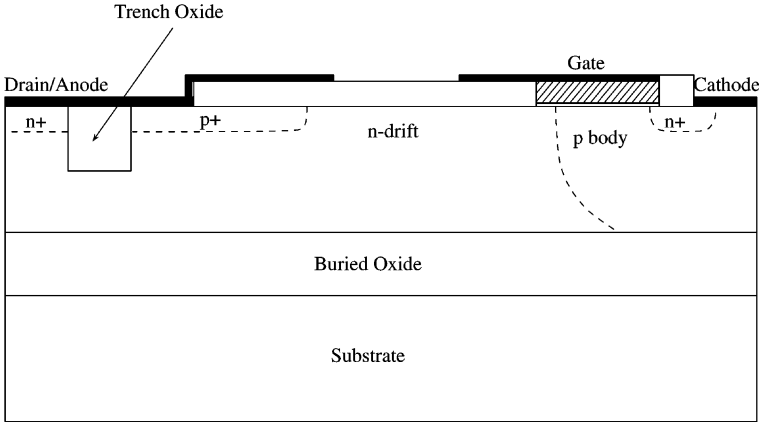

Fig. 3. Schematic structure of the proposed SOI SA-LIGBT with a trench oxide at the drain/anode.

Table 1
The technological and geometrical parameters of the SOI SA-LIGBT.

Parameter	Value
N-drift doping N_D	1.0×10^{16} cm^{-3}
N-drift length L_d	8.5 μm
SOI thickness t_{soi}	2.0 μm
N-substrate doping	5.0×10^{18} cm^{-3}
Buried oxide thickness t_{ox}	1.0 μm
n^+ drain length	2.0 μm
p^+ anode length	6.0 μm
Trench oxide depth	0.5–1.5 μm

depth is 1.0 μm. A highly doped n-buffer is added at the drain/anode region which helps to prevent punch through at this region [16]. An n^+ drain length of 2.0 μm and a p^+ anode length of 6.0 μm are used through out all the simulations in the paper. With the structure proposed it is possible to suppress the NDR without increasing the p^+ anode length. The device has a hybrid LDMOSFET-LIGBT structure with a common drift region. The p^+ anode provides conductivity modulation of the n-drift region. The n^+ drain defines a lateral DMOS structure and an electron extraction path during turn-off of the device. As a result two different modes of on-state operation can be seen, which depend on the bias conditions. At low anode voltages the device exhibits MOSFET operation. Only the n^+ region at the drain/anode contributes to current conduction in the on-state, and significant conductivity modulation of the n-drift region cannot be seen. As the anode voltage increases, the potential underneath the p^+ anode starts to fall and makes the p^+ anode and n-drift junction forward biased. Considerable injection of holes from the p^+ anode to the n-drift takes place, resulting in lower forward voltage

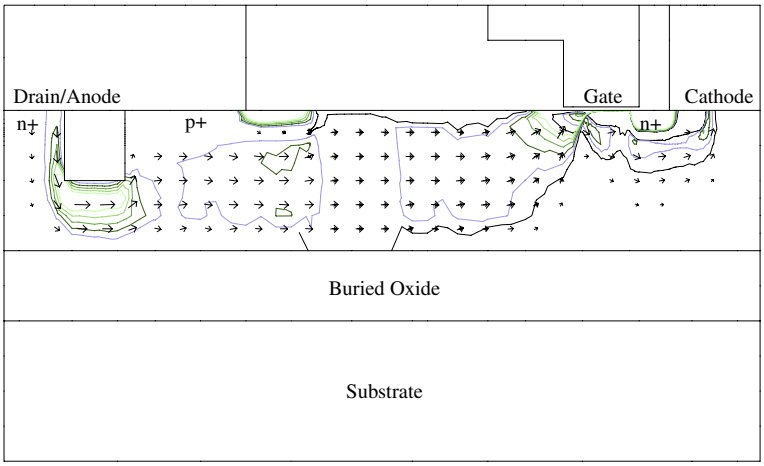

Fig. 4. Current flow in the proposed SA-LIGBT at $V_G = 12$ V and $V_A = 10$ V.

drop compared to the SOI-LDMOSFET. Fig. 4 shows the current flows of the proposed SA-LIGBT at $V_G = 12$ V and $V_A = 10$ V. The electron current at the n^+ drain region, and the hole current at the p^+ anode and under the cathode (p-body region) can be seen simultaneously.

3. Simulation results

3.1. SJ SOI-LDMOSFET

The drift doping of conventional SOI-LDMOSFETs is restricted by the RESURF (reduced surface field) effect [17,18]. To increase the BV the drift length must be increased and the doping decreased. This results in an increase in the on-resistance. With the SJ structure it is possible to increase the doping concentration of the drift layer drastically, and R_{SP} can be reduced effectively. The on-resistance of the SJ devices has a linear voltage dependence instead of the square-law dependence of standard power MOSFETs [19]. The BV of the SJ depends on the critical electric field E_c of the device and the length of the n- and p-columns. With the SJ concept the n-column charge Q_n, the p-column charge Q_p, and the charge Q_{db} of the p-body depletion region should be balanced in this structure. Assuming that all columns are completely depleted before breakdown, the charges and BV are given by [11]

$$Q_n = Q_p + Q_{db} < 2\frac{\varepsilon_s E_c}{q} \tag{1}$$

$$Q_n = N_D W_N; \quad Q_p = N_A W_P \tag{2}$$

$$BV = E_c t_{N,P} \tag{3}$$

where $t_{N,P}$ is the length of the n and p-columns, respectively. From (3) it follows that the BV depends both on the critical electric field E_c and the column length. To reduce the column length of the SJ SOI-LDMOSFET we propose a trench oxide in the drift region.

Fig. 5 shows the comparison of the BV of conventional SOI-LDMOSFETs which have an n-drift length $L_d = 20.0$ μm and 13.0 μm, respectively, and the SJ SOI-LDMOSFET with a trench oxide and $L_d = 13.0$ μm. As shown in the figure the BV of the conventional devices strongly depends on the drift length. If the n-drift length is reduced to 13.0 μm in this structure, a BV of 245 V (the dotted line) is obtained at $N_D = 3.5\times10^{15}$ cm^{-3}. The

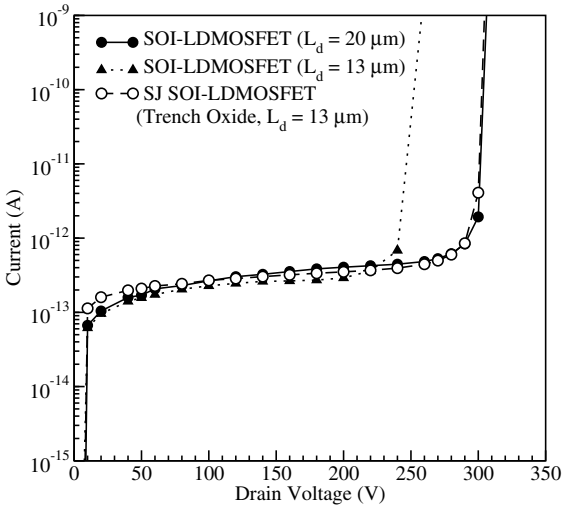

Fig. 5. Comparison of the BV of the conventional SOI-LDMOSFETs ($L_d = 20.0$ μm and 13.0 μm) and the SJ SOI-LDMOSFET with trench oxide ($L_d = 13.0$ μm). N_D of conventional devices are 2.3×10^{15} cm^{-3} (at $L_d = 20.0$ μm) and 3.5×10^{15} cm^{-3} (at $L_d = 13.0$ μm), respectively, and 6.0×10^{15} cm^{-3} of the SJ SOI-LDMOSFET.

dashed line in the figure shows the BV of the SJ SOI-LDMOSFET with trench oxide. Because of the increased surface path of the device, the BV increases with the trench oxide in the drift region. A BV of 300 V is obtained with $L_d = 13.0$ μm in this structure. Note that this is the same BV as that of the conventional SOI-LDMOSFET with $L_d = 20.0$ μm. Fig. 6 shows the electric field distribution of the suggested device at $V_{DS} = 300$ V, in particular a higher electric field can be observed at the trench oxide edges. We can see clearly several peaks of the electric field. The SJ SOI-LDMOSFET with a trench oxide has an additional peak in the middle of the SOI below the gate.

Fig. 7 shows a comparison of the electric field strength at the bottom of the trench oxide between the SOI-LDMOSFET and the SJ SOI-LDMOSFET. L_d of both structures is 13.0 μm. At the *n*-drift and *p*-body junction both devices show similar trends compared to the conventional device, but the abrupt peak can be seen at the trench oxide edge. Generally, in the middle of the device (along the lateral direction of the device) the conventional SOI-LDMOSFET has a broad range of higher electric field near the *n*-drift and *p*-body junction, and no abrupt peak can be found. The SJ SOI-LDMOSFET with a trench oxide with $L_d = 13.0$ μm and $N_D = 6.0\times10^{15}$ cm^{-3}, the optimum electric field strength distribution is obtained with N_A of 1.5×10^{16} cm^{-3} (with $W_P = 0.8$ μm).

The solid line of Fig. 8 shows the BV versus *n*-drift doping of the conventional SOI-LDMOSFET with an optimum $L_d = 20.0$ μm. If the *n*-drift doping is reduced below the optimum value (2.3×10^{15} cm^{-3}), the maximum electric field is moved towards the drain edge. If it exceeds the optimum value, a high electric field is moved towards the gate edge. Both cases cause lower BV. With the trench oxide in the drift region it is possible to increase the surface path of the depletion region and L_d can be reduced drastically without degrading the BV.

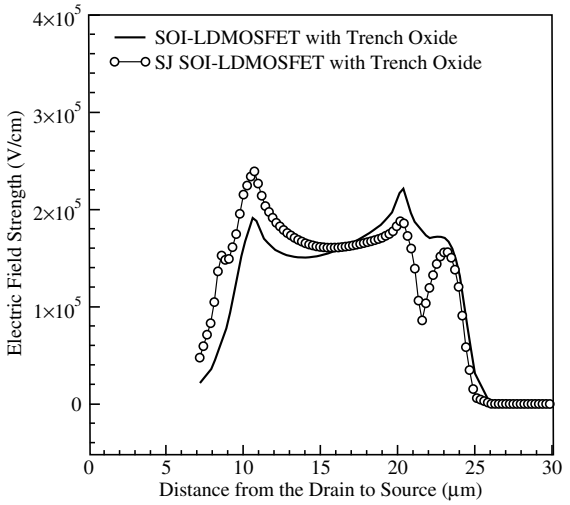

Fig. 7. Comparison of the electric field strength at the bottom of the trench oxide between the SOI-LDMOSFET and the SJ SOI-LDMOSFET. Both structures have a trench oxide in the drift region with $L_d = 13.0$ μm.

The dashed line shows the BV of the SOI-LDMOSFET which has a trench oxide in the drift region, a maximum BV of 300 V is obtained at $L_d = 13.0$ μm. Because the reduced *n*-drift area cause affects the charge balance condition, the optimum doping N_D is slightly increased compared to the conventional device.

The reduced conduction area caused by the trench oxide increases the R_{SP} of the device. To solve this problem we propose the SJ SOI-LDMOSFET by introducing the buried *p*-column in the *n*-drift region together with a trench oxide. With this structure R_{SP} can be lowered effectively. Fig. 9 shows the BV versus *p*-column doping of the proposed devices with various trench depths. L_d and N_D are fixed to 13.0 μm and

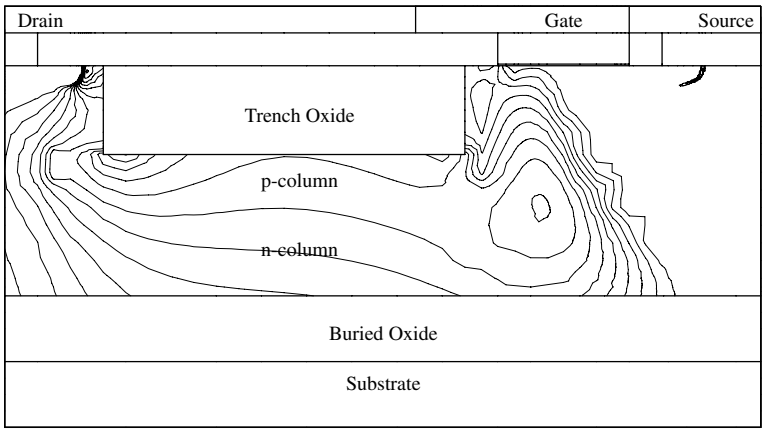

Fig. 6. Electric field distribution of a SJ SOI-LDMOSFET which has a trench oxide in the drift region at $V_{DS} = 300$ V.

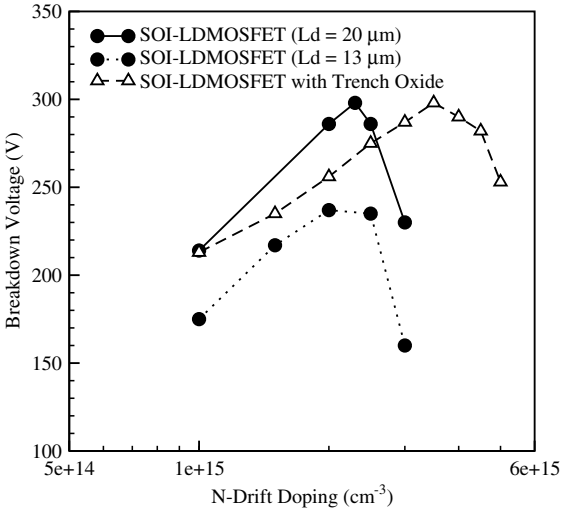

Fig. 8. BV versus *n*-drift doping of the conventional SOI-LDMOSFETs and SOI-LDMOSFET with trench oxide (trench depth = 2.7 μm and L_d = 13.0 μm).

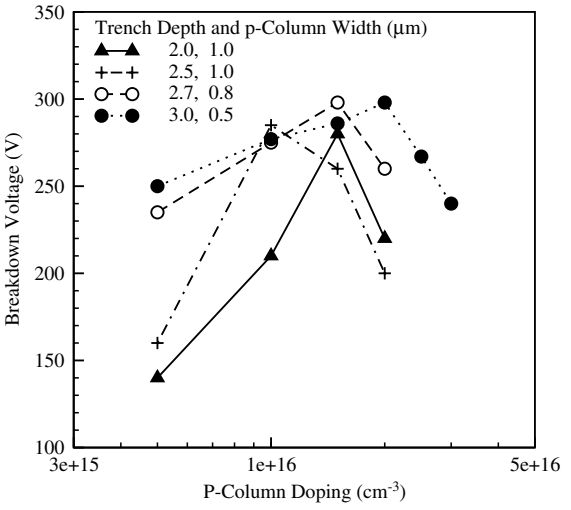

Fig. 9. BV versus *p*-column doping of the SJ SOI-LDMOSFETs with trench oxide which have L_d = 13.0 μm and $N_D = 6.0\times10^{15}$ cm^{-3}.

6.0×10^{15} cm^{-3}, respectively. The trench depth determines the length of the surface path of the device. If it is below 2.5 μm (solid and dot-dashed lines) the BV is lower than that of conventional devices. With a trench depth over 2.7 μm the same BV is reached as the maximum value of conventional SOI-LDMOSFETs.

To obtain the maximum BV, the charges Q_n, Q_p, and Q_{db} in the SJ SOI-LDMOSFET must be balanced for complete depletion of the drift region at breakdown. If the *p*-column width is larger, the doping of this layer should be reduced to fulfill the charge balance. To make

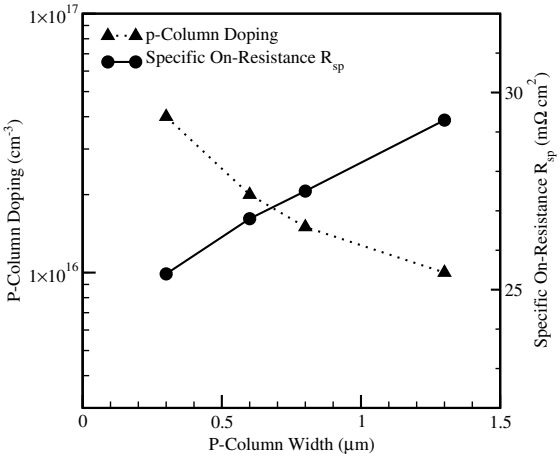

Fig. 10. *p*-column doping and R_{SP} versus *p*-column width of the SJ SOI-LDMOSFET which has a trench oxide.

it larger the conduction area is also important to minimize the *p*-column width. Fig. 10 shows the *p*-column doping and R_{SP} versus *p*-column width of the proposed SJ SOI-LDMOSFET which has a trench oxide. The *p*-column doping concentration at each point in the figure is optimized to have the maximum BV of 300 V. Other device parameters such as the trench oxide depth, the drift length L_d, and the *n*-column doping N_D are 2.7, 13.0 μm, and 6.0×10^{15} cm^{-3}, respectively. The doping of the *p*-column is reduced with the increased *p*-column width.

Eq. (3) shows this relationship, and the dotted line of Fig. 10 clearly follows this dependence. With $W_P = 0.3$ μm and 1.3 μm, the optimum N_A is 4.0 cm^{-3} and 1.0×10^{15} cm^{-3}, respectively. $Q_p = N_A \times W_P$ of both cases remains approximately constant. The solid line shows the relationship between W_P and R_{SP}. With reduced *p*-column width R_{SP} of the proposed device is improved by the increased conduction area. With lower W_P of 0.3 μm it is possible to achieve a minimum R_{SP} of 25.4 mΩ cm^2. If W_P of the structure is increased to 1.3 μm, R_{SP} is increased to 29.3 mΩ cm^2.

Table 2 shows a DC performance comparison of the simulation results between the conventional SOI-LDMOSFET and the SJ SOI-LDMOSFET which has a

Table 2
DC performance comparison between the conventional SOI-LDMOSFET and the proposed device

	Conventional SOI-LDMOSFET	SJ SOI-LDMOSFET with a trench oxide
N_D	2.3×10^{15} cm^{-3}	6.0×10^{15} cm^{-3}
L_d	20.0 μm	13.0 μm
R_{SP}	33.4 mΩ cm^2	25.4 mΩ cm^2
BV	300 V	300 V

trench oxide in the drift region. For the proposed device with an n-column doping N_D of 6.0×10^{15} cm^{-3} and a drift length L_d of 13.0 μm, a maximum BV of 300 V is obtained with a p-column doping $N_A = 4.0\times10^{16}$ cm^{-3} and a p-column width $W_P = 0.3$ μm. These results demonstrate that the drift length can be reduced with a trench oxide in the drift region. The on-state characteristics depend on the p-column width and the drift doping. The R_{SP} of the proposed device is 25.4 mΩ cm^2. It is about 76% of the corresponding R_{SP} of the conventional 300 V SOI-LDMOSFET. Even the width of the drift region is reduced by the p-column and R_{SP} is lower than that of the conventional device by the reduced L_d and the increased N_D of the proposed device.

3.2. SOI SA-LIGBT

Fig. 11 shows a comparison of the BV of the conventional SOI-LIGBT which has an n-drift length $L_d = 8.5$ μm, and the SOI SA-LIGBT with a trench oxide at the drain/anode. In the forward blocking state the leakage current of the conventional SOI-LIGBT depends both on the space charge carrier generation and the common base current gain of the pnp transistor, as a result a larger leakage current can be seen (dotted-dashed line in Fig. 11). The BV of the proposed SOI SA-LIGBT is much higher compared to that of the conventional SOI-LIGBT, it is the same BV as that of the conventional SA-LIGBT. A similar high blocking capability to that of a conventional SOI-LDMOSFET is obtained.

The on-state performance of the proposed SA-LIGBT has been simulated and compared with the conventional device. Fig. 12 shows the comparison of the I–V characteristics of a conventional SOI LIGBT, a conventional SOI SA-LIGBT, and the proposed SOI SA-LIGBT which has a trench oxide at the drain/anode region. As can be seen in the figure SA-LIGBTs have a NDR region which cannot be found in the conventional LIGBT. This is due to the two different conduction mechanisms responsible for the current flow. The NDR corresponds to the snap-back regions in the I–V curves in Fig. 12. With the proposed structure the snap-back voltage is reduced effectively compared to the conventional SA-LIGBT with the same p^+ anode length. The snap-back voltage of the proposed SOI SA-LIGBT is 1.95 V, it is reduced by about 20% compared to the conventional SA-LIGBT (about 2.45 V) which has the same device parameters. This demonstrates that the trench oxide at the drain/anode can suppress the NDR effectively without increasing the p^+ anode length.

Fig. 13 shows the on-state characteristics of the proposed SOI SA-LIGBT. Because of the weak injection of the pnp bipolar structure compared to the conventional LIGBT, the current density of the proposed SA-LIGBT is lower than that of the conventional LIGBT. However, the forward biased safe operating area (FBSOA) limited by the latch-up parasitic thyristor inherent in its structure is increased compared to the conventional SOI-LIGBT. I–V curves in the figure show that the SA-LIGBT has good saturation currents up to the $V_G = 30$ V and $V_A = 80$ V without latch-up.

The switching performance of conventional IGBTs is limited by the excess carrier recombination process producing tail current. Additionally, hole injection is not stopped instantly leading to increased switching time.

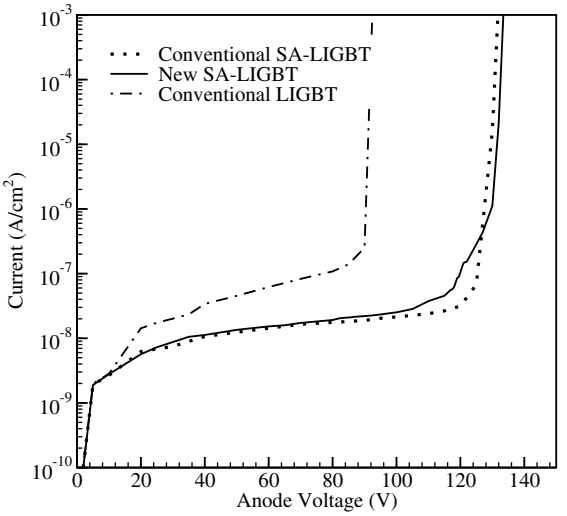

Fig. 11. BV comparison of the conventional SOI-LIGBT, and the conventional and proposed SOI SA-LIGBTs. Lower leakage currents can be seen at the SA-LIGBTs.

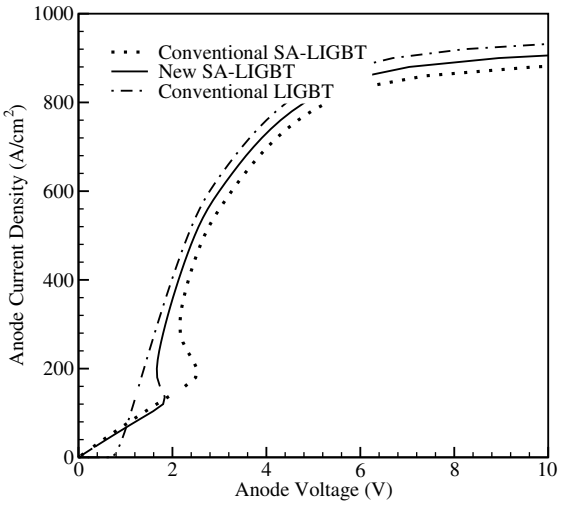

Fig. 12. I–V comparison of the conventional SOI-LIGBT and the conventional and proposed SOI SA-LIGBTs. A reduced snap-back voltage of the proposed device can be seen.

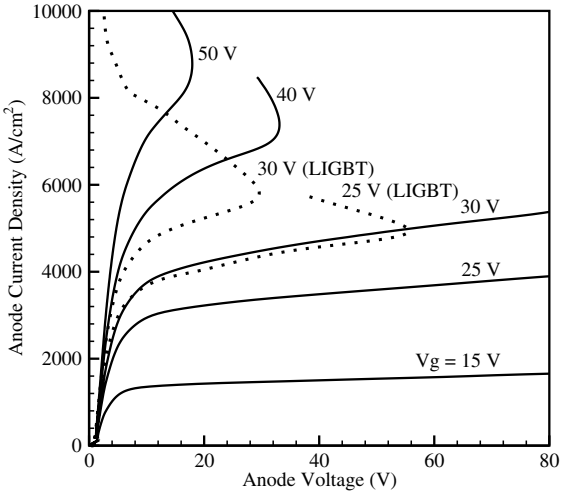

Fig. 13. On-state characteristics of the proposed SOI SA-LIGBT and a conventional SOI-LIGBT. The considerable improvement of the latch-up can be seen.

There are two distinct phases in the turn-off waveform of the conventional LIGBT. The first phase is characterized by a rapid fall in anode current, corresponding to the electron current flowing through the MOSFET, which is reduced to zero when the gate voltage drops below its threshold voltage. The second phase is dominated by the slowly decaying tail of the anode current. During the second phase, minority carriers (holes) stored in the drift region are removed by the recombination processes, and the decay of this stored charge is mainly determined by the minority carrier lifetime in the drift region. The reduction of the carrier lifetime in the drift region causes to increase the on-resistance of the devices. The n^+ anode short of the SA-LIGBT provides an electron extraction path during turn-off. It aids fast decaying of excess carriers (holes) in the n-drift region and reduces switching speed compared to the conventional LIGBT. Fig. 14 shows the turn-off characteristics of the proposed SOI SA-LIGBT and a conventional SOI LIGBT. Turn-off simulations were performed at an anode current density of 190 A/cm^2, $V_A = 50$ V, and $V_G = 12$ V. The devices were turned off by ramping down the gate voltage from 12 V to 0 V in 10 ns. A carrier lifetime of 10 μs for both electrons and holes were used in the simulation. As can be seen in the figure the turn-off tail of the proposed SA-LIGBT is extremely small in comparison to the conventional SOI-LIGBT. It gives similar characteristics as that of the SOI-LDMOSFET, thus reducing considerably the turn-off time and the transient power losses.

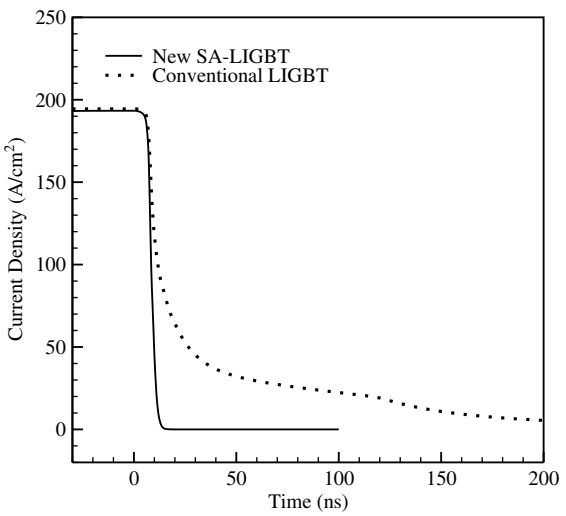

Fig. 14. Turn-off characteristics of the proposed SOI SA-LIGBT and a conventional SOI-LIGBT at the anode current density 190 A/cm^2, $V_A = 50$ V, and $V_G = 12$ V. The tail current dose not exist for the SOI SA-LIGBT.

4. Conclusions

The proposed high-voltage SJ SOI-LDMOSFET transistor with a trench oxide in the drift region exhibits a reduced R_{SP}. For the device, which has a drift length $L_d = 13.0$ μm, a p-column doping $N_A = 4.0 \times 10^{16}$ cm^{-3}, and a p-column width $W_P = 0.3$ μm, R_{SP} is 25.4 mΩ cm^2. At $L_d = 13.0$ μm, the BV is the same as that of a conventional SOI-LDMOSFET with $L_d = 20.0$ μm. The R_{SP} of the proposed device is about 76% and the n-drift length is about 65% of that of a conventional SOI-LDMOSFET, respectively. With this new device concept it is possible to reduce the device size and R_{SP} without degrading the BV.

In addition, we propose a SOI SA-LIGBT which has a trench oxide at the drain/anode region. The n^+ drain and p^+ anode of this device are separated by the trench oxide, which results in a higher pinchoff resistance under the p^+ anode. With this structure it is possible to suppress the NDR effectively without increasing the p^+ anode length. The snap-back voltage inherently present in the SA-LIGBT is about 20% lower than that of a conventional SA-LIGBT. Additionally, significant improvements in the turn-off time are achieved by the shorted-anode structure.

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